REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change boilerplate to allow for class V criteria. Add class V devices to this SMD. Editorial changes throughout.	97-01-27	Monica L. Poelking
B	Correct figure 5. Update boilerplate. - jak	00-10-24	Thomas M. Hess
C	Add case outline Z. Update the boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - TVN	02-08-16	Thomas M. Hess

REV																			
SHEET																			
REV																			
SHEET																			
REV	C	C	C																
SHEET	15	16	17																

REV STATUS OF SHEETS																
REV	C	B	C	C	C	B	B	B	C	C	C	B	B	B		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
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Michael A. Frye

DRAWING APPROVAL DATE
89-11-06

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89847**

SHEET 1 OF 17

DSCC FORM 2233
APR 97

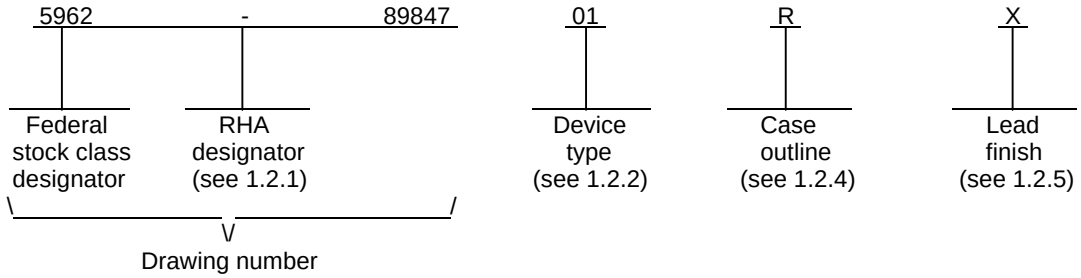
5962-E533-02

1. SCOPE

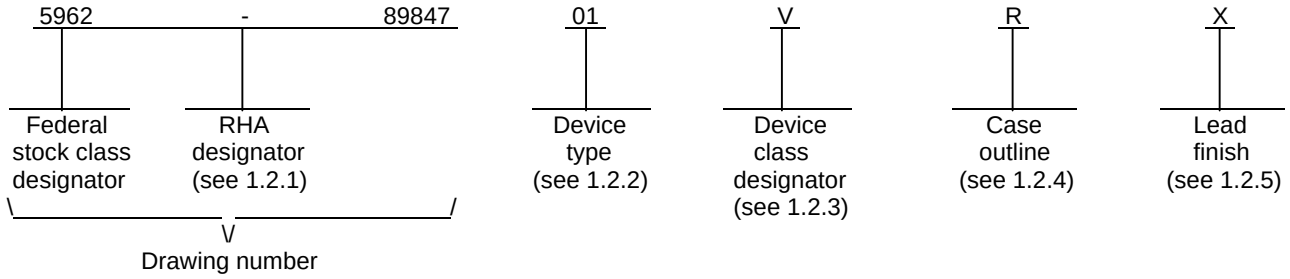
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT241	Octal buffer/line driver with three-state outputs, TTL compatible inputs
02	54ACT11241	Octal buffer/line driver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.
Q or V	Certification and qualification to MIL-PRF-38535.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
Z	GDFP1-G20	20	Flat pack with gullwing
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Input clamp diode current (I_{IK})	±20 mA
Output clamp diode current (I_{OK})	±20 mA
DC output current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±100 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 3/

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Maximum high level input voltage (V_{IH})	2.0 V
Case operating temperature range (T_C)	-55°C to +125°C
Input rise and fall rate ($\Delta t/\Delta V$)	8 ns/V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+24 mA

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

EIA/JEDEC Standard No. 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage 3006	V_{OH}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND, I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.4		V
				5.5 V		5.4		
		For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND, I_{OH} = -24 mA		4.5 V		3.7		
				5.5 V		4.7		
		For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND, I_{OH} = -50 mA 4/		5.5 V		3.85		
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND, I_{OL} = 50 µA	All All	4.5 V	1, 2, 3		0.1	V
				5.5 V			0.1	
		For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 24 mA	All V	4.5 V	1, 3		0.4	
					2		0.5	
			All M, Q		1		0.4	
					2, 3		0.5	
			All V	5.5 V	1, 3		0.4	
					2		0.5	
			All M, Q		1		0.4	
					2, 3		0.5	
		For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 mA 4/	All All	5.5 V	1, 2, 3		1.65	
Three-state output leakage current high 3021	I_{OZH} 5/	$\overline{OE1}$ or OE2 = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = 5.5 V	All V	5.5 V	1		0.5	µA
					2		10.0	
			All M, Q		1		0.5	
					2, 3		10.0	
Three-state output leakage current low 3020	I_{OZL} 5/	$\overline{OE1}$ or OE2 = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = GND	All V	5.5 V	1		-0.5	
					2		-10.0	
			All M, Q		1		-0.5	
					2, 3		-10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, $I_{IN} = 1.0$ mA	All V	0.0 V	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, $I_{IN} = -1.0$ mA	All V	Open	1	-0.4	-1.5	V
Input current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All V	5.5 V	1		0.1	µA
					2		1.0	
			All M, Q		1		0.1	
					2, 3		1.0	
Input current low 3009	I_{IL}	For input under test, $V_{IN} = GND$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All V	5.5 V	1		-0.1	µA
					2		-1.0	
			All M, Q		1		-0.1	
					2, 3		-1.0	
Input capacitance 3012	C_{IN}	See 4.4.1c $T_C = +25°C$	All All	GND	4		8.0	pF
Output capacitance 3012	C_{OUT}	See 4.4.1c $T_C = +25°C$	All V	5.5 V	4		15.0	
Power dissipation capacitance	C_{PD} 6/	See 4.4.1c $T_C = +25°C$	All All	5.0 V	4		70	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 7/	For input under test, $V_{IN} = V_{CC} - 2.1$ V For all other inputs, $V_{IN} = V_{CC}$ or GND	All V	5.5 V	3		1.6	mA
					1, 2		1.0	
			All M, Q		1, 2, 3		1.6	
Quiescent supply current, outputs high 3005	I_{CCH}	$\overline{OE1}$ = GND and OE2 = V_{CC} For all inputs, $V_{IN} = V_{CC}$	All V	5.5 V	1		2.0	µA
					2		40.0	
			All M, Q		1, 2, 3		160.0	
Quiescent supply current, outputs low 3005	I_{CCL}	$\overline{OE1}$ = GND and OE2 = V_{CC} For all inputs, $V_{IN} = GND$	All V	5.5 V	1		2.0	µA
					2		40.0	
			All M, Q		1, 2, 3		160.0	
Quiescent supply current, outputs three-state 3005	I_{CCZ}	$\overline{OE1}$ = V_{CC} and OE2 = GND For all inputs, $V_{IN} = V_{CC}$ or GND	All V	5.5 V	1		2.0	µA
					2		40.0	
			All M, Q		1, 2, 3		160.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Low level ground bounce noise	V_{GBL} 8/ 9/	V_{LD} = 2.5 V I_{OL} = +24 mA See figure 5, See 4.4.1d	All V	4.5 V	4		2000	mV
High level ground bounce noise	V_{GBH} 8/ 9/	V_{LD} = 2.5 V I_{OH} = -24 mA See figure 5 , See 4.4.1d	All V	4.5 V	4		2000	mV
Latch-up input/output over-voltage	I_{CC} (O/V1) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ V_{test} = 6.0 V, V_{CCQ} = 5.5 V V_{over} = 10.5 V, See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output positive over-current	I_{CC} (O/I1+) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ V_{test} = 6.0 V, V_{CCQ} = 5.5 V $I_{trigger}$ = +120 mA , See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I_{CC} (O/I1-) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ V_{test} = 6.0 V, V_{CCQ} = 5.5 V $I_{trigger}$ = -120 mA, See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$, $5\ \mu s \le t_f \le 5\ ms$ V_{test} = 6.0 V, V_{CCQ} = 5.5 V V_{over} = 9.0 V, See 4.4.1d	All V	5.5 V	2		100	mA
Functional tests 3014	11/	V_{IL} = 0.40 V, V_{IH} = 2.40 V Verify output V_{OUT} See 4.4.1b	All All	4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Propagation delay time, data to output, mAn to mYn 3003	t_{PHL} 12/	C_L = 50 pF R_L = 500Ω See figure 5	All V	4.5 V	9, 11	1.0	9.0	ns
					10	1.0	10.0	
			01 M, Q		9	1.0	9.0	
					10, 11	1.0	10.0	
			02 M, Q		9	1.5	8.5	
					10, 11	1.5	9.5	
	t_{PLH} 12/	C_L = 50 pF R_L = 500Ω See figure 5	All V	4.5 V	9, 11	1.0	9.0	ns
					10	1.0	10.0	
			01 M, Q		9	1.0	9.0	
					10, 11	1.0	10.0	
			02 M, Q		9	1.5	9.0	
					10, 11	1.5	10.7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable, $\overline{OE1}$ and OE2 to mYn 3003	t_{PZH} 12/	$C_L = 50$ pF $R_L = 500\Omega$ See figure 5	All V	4.5 V	9, 11	1.0	9.0	ns
					10	1.0	11.5	
			01 M, Q		9	1.0	9.0	
					10, 11	1.0	11.5	
			02 M, Q		9	1.5	11.3	
					10, 11	1.5	13.0	
	t_{PZL} 12/	$C_L = 50$ pF $R_L = 500\Omega$ See figure 5	All V	4.5 V	9, 11	1.0	10.0	ns
					10	1.0	12.5	
			01 M, Q		9	1.0	10.0	
					10, 11	1.0	12.5	
			02 M, Q		9	1.5	11.5	
					10, 11	1.5	11.9	
Propagation delay time, output disable, $\overline{OE1}$ and OE2 to mYn 3003	t_{PHZ} 12/	$C_L = 50$ pF $R_L = 500\Omega$ See figure 5	All V	4.5 V	9, 11	1.0	10.5	ns
					10	1.0	12.5	
			01 M, Q		9	1.0	10.5	
					10, 11	1.0	12.5	
			02 M, Q		9	1.5	10.6	
					10, 11	1.5	11.4	
	t_{PLZ} 12/	$C_L = 50$ pF $R_L = 500\Omega$ See figure 5	All V	4.5 V	9, 11	1.0	10.5	ns
					10	1.0	12.5	
			01 M, Q		9	1.0	10.5	
					10, 11	1.0	12.5	
			02 M, Q		9	1.5	11.2	
					10, 11	1.5	12.0	

1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25°C$.
b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25°C$.
c. All ΔI_{CC} and I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

TABLE I. Electrical performance characteristics - Continued.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at 4.5 V $\leq V_{CC} \leq$ 5.5 V.

4/ Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

5/ For the I_{OZH} and I_{OZL} tests, three-state outputs are required.

6/ Power dissipation capacitance (C_{PD}) determines the no load power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC}) f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$. For both P_D and I_S, n is the number of device inputs at TTL levels; f is the frequency of the input signal; d is the duty cycle of the input signal; and C_L is the external output load capacitance.

7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Class V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

8/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = i.e, ±24 mA) and 50 pF of load capacitance (see figure 4). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f$ = 3.5 ±1.5ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (see figure 4). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

9/ When used in asynchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2,000 mV can be a possible problem.

10/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$, and V_{over}, are to be accurate within ±5 percent.

11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated.

12/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum AC limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

Device type	01	02	
Case outlines	R, S, Z, 2	L	3
Terminal number	Terminal symbol		
1	$\overline{OE1}$	1Y1	NC
2	1A1	2Y1	V_{CC}
3	4Y2	3Y1	4A1
4	2A1	4Y1	3A1
5	3Y2	GND	2A1
6	3A1	GND	1A1
7	2Y2	GND	$\overline{OE1}$
8	4A1	GND	NC
9	1Y2	1Y2	1Y1
10	GND	2Y2	2Y1
11	1A2	3Y2	3Y1
12	4Y1	4Y2	4Y1
13	2A2	OE2	GND
14	3Y1	4A2	GND

Device type	01	02	
Case outlines	R, S, Z, 2	L	3
Terminal number	Terminal symbol		
15	3A2	3A2	NC
16	2Y1	2A2	GND
17	4A2	1A2	GND
18	1Y1	V_{CC}	1Y2
19	OE2	V_{CC}	2Y2
20	V_{CC}	4A1	3Y2
21	---	3A1	4Y2
22	---	2A1	NC
23	---	1A1	OE2
24	---	$\overline{OE1}$	4A2
25	---	---	3A2
26	---	---	2A2
27	---	---	1A2
28	---	---	V_{CC}

Pin description	
Terminal symbol	Description
mAn (m = 1 to 4, n = 1 to 2)	Data inputs
mYn (m = 1 to 4, n = 1 to 2)	Data outputs
$\overline{OE1}$	Output enable control inputs (active low)
OE2	Output enable control inputs (active high)

FIGURE 1. Terminal connections.

Device types 01 and 02			
Inputs			Outputs
$\overline{OE1}$	OE2	mAn	mYn
L L H	H H L	L H X	L H Z

H = High voltage level.
L = Low voltage level.
X = Irrelevant
Z = High impedance

FIGURE 2. Truth table.

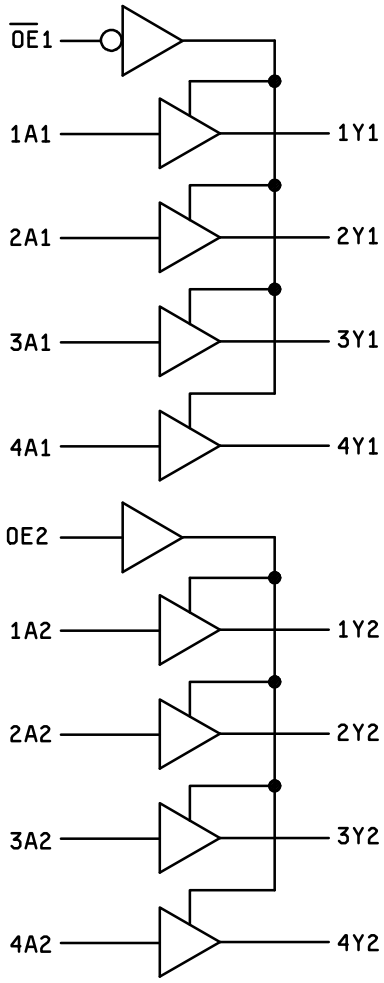
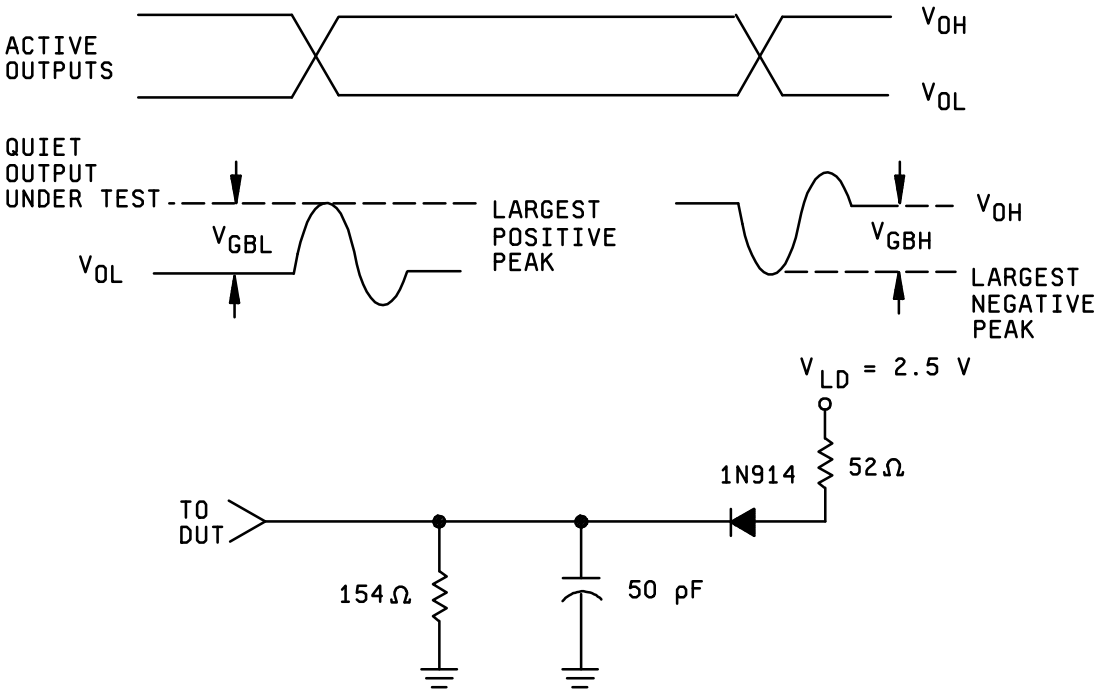
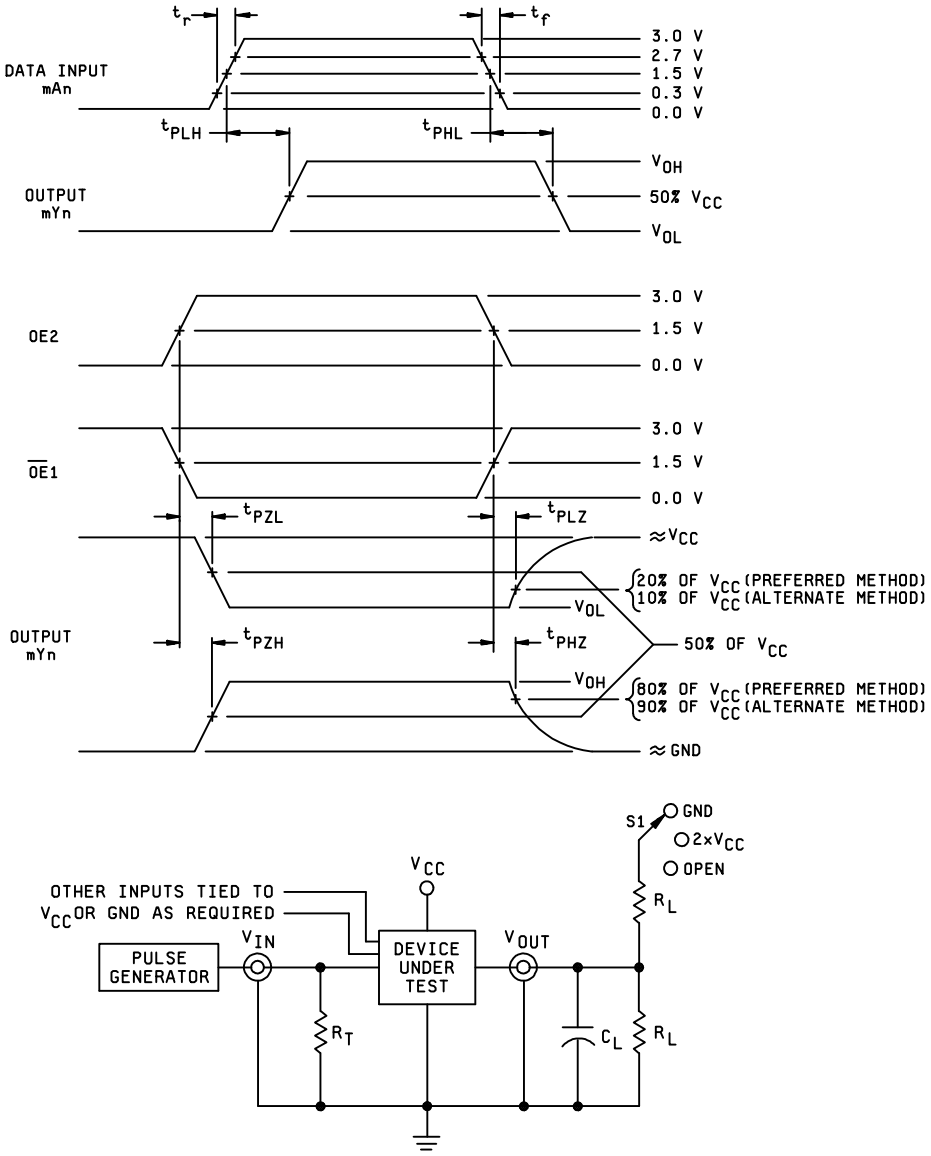


FIGURE 3. Logic diagram.



NOTE: Resistance and capacitance tolerances = ±10 %.

FIGURE 4. Ground bounce load circuit and waveforms.



NOTES:

1. Preferred method – used for device type 02:
   When measuring t_{PLH} and t_{PHL}: S1 = open.
   When measuring t_{PLZ} and t_{PZL}: S1 = 2 x V_{CC}.
   When measuring t_{PHZ} and t_{PZH}: S1 = GND.
2. Alternate method – used for device type 01:
   When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: S1 = open.
   When measuring t_{PLZ} and t_{PZL}: S1 = 2 x V_{CC}.
3. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
4. R_L = 500Ω or equivalent, R_T = 50Ω or equivalent.
5. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
6. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
7. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein.. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

d. Latch-up and ground bounce tests are required for device class V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground bounce tests, test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 02-08-16

Approved sources of supply for SMD 5962-89847 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE Number	Vendor Similar PIN 2/
5962-8984701RA	27014 01295	54ACT241DMQB SNJ54ACT241J
5962-8984701SA	27014 01295	54ACT241FMQB SNJ54ACT241W
5962-89847012A	27014 01295	54ACT241LMQB SNJ54ACT241FK
5962-8984701VRA	27014	54ACT241J-QMLV
5962-8984701VSA	27014	54ACT241W-QMLV
5962-8984701VZA	27014	54ACT241WG-QMLV
5962-8984701V2A	27014	54ACT241E-QMLV
5962-8984702LA	3/	SNJ54ACT11241J
5962-89847023A	3/	SNJ54ACT11241FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493