REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02, generic 1847. Add two packages, F-5 and C-2. Make changes to paragraphs 1.2.1, 1.2.2, 6.4, table I, and figures 1 and 2. Change drawing CAGE code to 67268.	89-03-22	M. A. FRYE
B	Changes in accordance with NOR 5962-R080-94.	94-06-24	M. A. FRYE
C	Make changes to latching and nonlatching current test in table I. Update boilerplate. Add class V for vendor CAGE 01295. -rrp	00-12-01	R. MONNIN
D	Drawing updated to reflect current requirements. - ro	03-03-04	R. MONNIN

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
DONALD R. OSBORNE

CHECKED BY
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APPROVED BY
N. A. HAUCK

DRAWING APPROVAL DATE
87-03-10

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, CURRENT MODE PULSE WIDTH MODULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86806**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

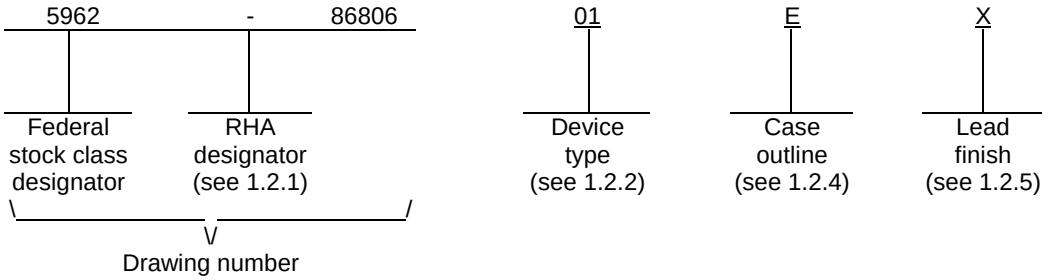
5962-E238-03

1. SCOPE

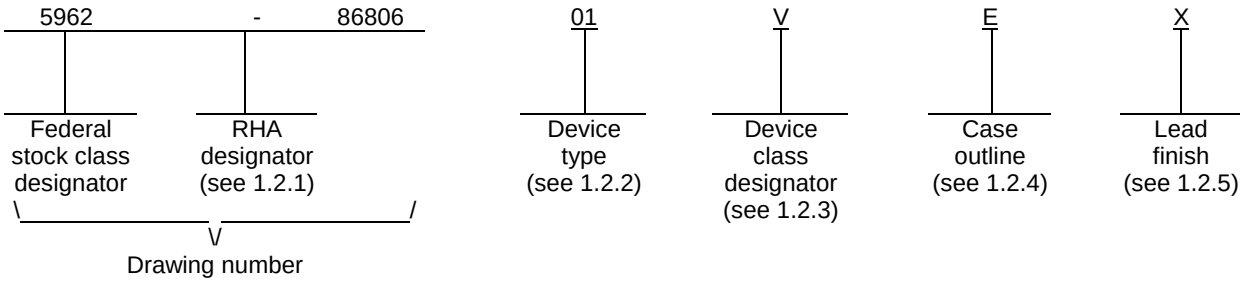
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	1846	Controller, pulse-width modulator
02	1847	Controller, pulse-width modulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{IN})	+40 V dc
Collector supply voltage (V_C)	+40 V dc
Output current, source or sink	500 mA dc
Analog inputs	-0.3 V to +V_{IN}
Reference output current	-30 mA dc
Sync output current	-5 mA dc
Error amplifier output current	-5 mA dc
Soft start sink current	50 mA dc
Oscillator charging current	5 mA dc
Power dissipation at T_A = +25°C	1000 mW 2/
Power dissipation at T_C = +25°C	2000 mW 3/
Junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	100°C/W
Case F	115°C/W
Case 2	88°C/W

1.4 Recommended operating conditions.

Supply voltage range	+8 V dc to +40 V dc
Collector supply voltage range	+4.5 V dc to +40 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate at 10 mW/°C for T_A above +50°C.
3/ Derate at 16 mW/°C for T_C above +25°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference section							
Output voltage	V_O	T_A = +25°C, I_O = 1 mA	1	All	5.05	5.15	V dc
Line regulation	R_{LINE}	8 V ≤ V_{IN} ≤ 40 V	1,2,3	All	-20	20	mV dc
Load regulation	R_{LOAD}	-10 mA ≤ I_L ≤ -1 mA	1,2,3	All	-15	15	mV dc
Total output variation 2/	----	Line, load, and temperature	1,2,3	All	5.00	5.20	V dc
Short circuit output	I_{OS}	V_{REF} = 0 V, Both negative and positive currents are considered to decrease towards 0.	1,2,3	All	-10		mA dc
Oscillator section							
Initial accuracy	---	T_A = +25°C, R_T = 10 kΩ , C_T = 4700 pF	4	All	39	47	kHz
Frequency change with voltage	Δf_{OSC}	8 V ≤ V_{IN} ≤ 40 V	4,5,6	All	-2.0	2.0	%
Sync output voltage high level	V_{SOH}		1,2,3	All	3.9		V dc
Sync output voltage low level	V_{SOL}					2.7	
Sync input voltage high level	V_{SIH}	C_T = 0 V	1,2,3	All	3.9		V dc
Sync input voltage low level	V_{SIL}					2.5	
Sync input current	I_{SYNC}	Sync voltage = 5.25 V, C_T = 0 V	1,2,3	All		1.5	mA dc

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error amplifier section							
Input offset voltage	V_{IO}		1,2,3	All		5.0	mV dc
Input bias current	I_{IB}		1,2,3	All	-1.0		µA dc
Input offset current	I_{IO}		1,2,3	All	-250	250	nA dc
Open loop voltage gain	A_{VS}	V_O = 1.2 V to 3 V, V_{CM} = 2 V	4,5,6	All	80		dB
Unity gain bandwidth 2/	GBW	T_A = +25°C	4	All	0.7		MHz
Common mode rejection ratio	CMRR	0 V ≤ V_{CM} ≤ 38 V, V_{IN} = 40 V	4,5,6	All	75		dB
Power supply rejection ratio	PSRR	8 V ≤ V_{IN} ≤ 40 V	4,5,6	All	80		dB
Output sink current (COMPENSATION pin)	I_{SINK}	-15 mV ≤ V_{ID} ≤ -5 V, V_{COMP} pin = 1.2 V	1,2,3	All	2.0		mA dc
Output source current (COMPENSATION pin)	I_{SOURCE}	15 mV ≤ V_{ID} ≤ 5 V, V_{COMP} pin = 2.5 V	1,2,3	All		-0.4	mA dc
High level output voltage	V_{OH}	R_L = (COMP) 15 kΩ	1,2,3	All	4.3		V dc
Low level output voltage	V_{OL}	R_L = (COMP) 15 kΩ	1,2,3	All		1.0	V dc
Current sense amplifier section							
Amplifier gain 3/ 4/	A_V	$V_{(-CUR\ SENSE)}$ pin = 0 V, $V_{(CUR\ LIM/SS)}$ pin open	4,5,6	All	2.5	3.15	V dc
Maximum differential input signal (pos and neg current sense pin voltages)	V_{IDIFF}	$V_{(CUR\ LIM/SS)}$ pin open, 3/ R_L = (COMP pin) = 15 kΩ	1,2,3	All	1.1		V dc
Input offset voltage	V_{IO}	$V_{(CUR\ LIM/SS)}$ pin = 0.5 V, COMP pin open 3/	1,2,3	All	-25	25	mV dc
Common mode rejection ratio	CMRR	1 V ≤ V_{CM} ≤ 12 V	4,5,6	All	60		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current sense amplifier section - continued							
Power supply rejection ratio	PSRR	$8 V \le V_{IN} \le 40 V$	4,5,6	All	60		dB
Input bias current	I_{IB}	$V_{(CUR LIM/SS)}$ pin = 0.5 V, 3/ COMP pin open	1,2,3	All	-10		µA dc
Input offset current	I_{IO}	$V_{(CUR LIM/SS)}$ pin = 0.5 V, 3/ COMP pin open	1,2,3	All	-1.0	1.0	µA dc
Delay to outputs 2/	----	T_A = +25°C	9	All		500	ns
Current limit adjust section							
Current limit offset	---	$V_{(-CUR LIM/SS)}$ pin = 0 V, 3/ $V_{(+CUR LIM/SS)}$ pin = 0 V, COMP pin open	1,2,3	All	0.40	0.55	V dc
Input bias current	I_{IB}	$V_{(+ERROR AMP)}$ pin = V_{REF}, $V_{(+ERROR AMP)}$ pin = 0 V	1,2,3	All	-30		µA dc
Shutdown terminal section							
Threshold voltage	---	$R_{L(CUR LIM/SS)}$ pin = 15 kΩ at 2 V or equivalent.	1,2,3	All	250	400	mV dc
Latching current	---	Current into CUR LIM/SS 5/	1,2,3	All	3		mA
Nonlatching current	---	Current into CUR LIM/SS 6/	1,2,3	All		0.8	mA
Delay to outputs 2/	---	T_A = +25°C	1	All		600	ns
Output section							
Collector-emitter voltage	---		1,2,3	All	40		V dc
Collector leakage current	---	V_C = 40 V	1,2,3	01		200	µA dc

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output section - continued							
Output low level	V_{OL}	I_{SINK} = 20 mA	1,2,3	All		0.4	V dc
		I_{SINK} = 100 mA				2.1	
Output high level	V_{OL}	I_{SOURCE} = 20 mA	1,2,3	All	13		V dc
		I_{SOURCE} = 100 mA			12		
Rise time 2/	t_R	C_L = 1,000 pF, T_A = +25°C	9	All		300	ns
Fall time 2/	t_F	C_L = 1,000 pF, T_A = +25°C	9	All		300	ns
Under-voltage lockout section							
Start-up threshold	---		1,2,3	All		8.0	V dc
Total standby current section							
Supply current	I_{CC}		1,2,3	All		21	mA dc
Cold start/PWM latch reset	L_{RESET}	T_J = -55°C, R_T = 10 kΩ, C_T = 4700 pF, SYNC I_{OUT} = -1 mA	3	All	7/		kHz

1/ Standard test conditions (unless otherwise specified): $+V_{IN}$ = 15 V dc, R_T = 10 kΩ, C_T = 4,700 pF.

2/ If not tested, shall be guaranteed to specified limits.

3/ Parameter measured at trip point of latch with $V_{+ERROR\ AMP} = V_{REF}$; $V_{-ERROR\ AMP}$ = 0 V.

4/ Amplifier gain defined as:

$$G = (\Delta V_{COMP\ pin} / \Delta V_{+CURRENT\ SENSE\ pin}) ; \quad \Delta V_{+CURRENT\ SENSE\ pin} = 0 \text{ to } 1.0 \text{ V}$$

5/ Current into CUR LIM/SS pin guaranteed to latch circuit in shutdown state.

6/ Current into CUR LIM/SS pin guaranteed not to latch circuit in shutdown state.

7/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWN latch Set command. To minimize the effects of self heating, the test must be completed within the first 50 milliseconds of applied power. The minimum limit shall be equal to 0.49 x the oscillator frequency.

Device types	01 and 02	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	CUR. LIMIT/SOFTSTART	NC
2	V_{REF}	CUR. LIMIT/SOFTSTART
3	(-) CUR. SENSE	V_{REF}
4	(+) CUR. SENSE	(-) CUR. SENSE
5	(+) ERROR AMP	(+) CUR. SENSE
6	(-) ERROR AMP	NC
7	COMPENSATION	(+) ERROR AMP
8	C_T	(-) ERROR AMP
9	R_T	COMPENSATION
10	SYNC	C_T
11	OUTPUT A	NC
12	GROUND	R_T
13	V_C	SYNC
14	OUTPUT B	OUTPUT A
15	V_{IN}	GROUND
16	SHUTDOWN	NC
17	----	V_C
18	----	OUTPUT B
19	----	V_{IN}
20	----	SHUTDOWN

NC = No connection

FIGURE 2. Terminal connections.

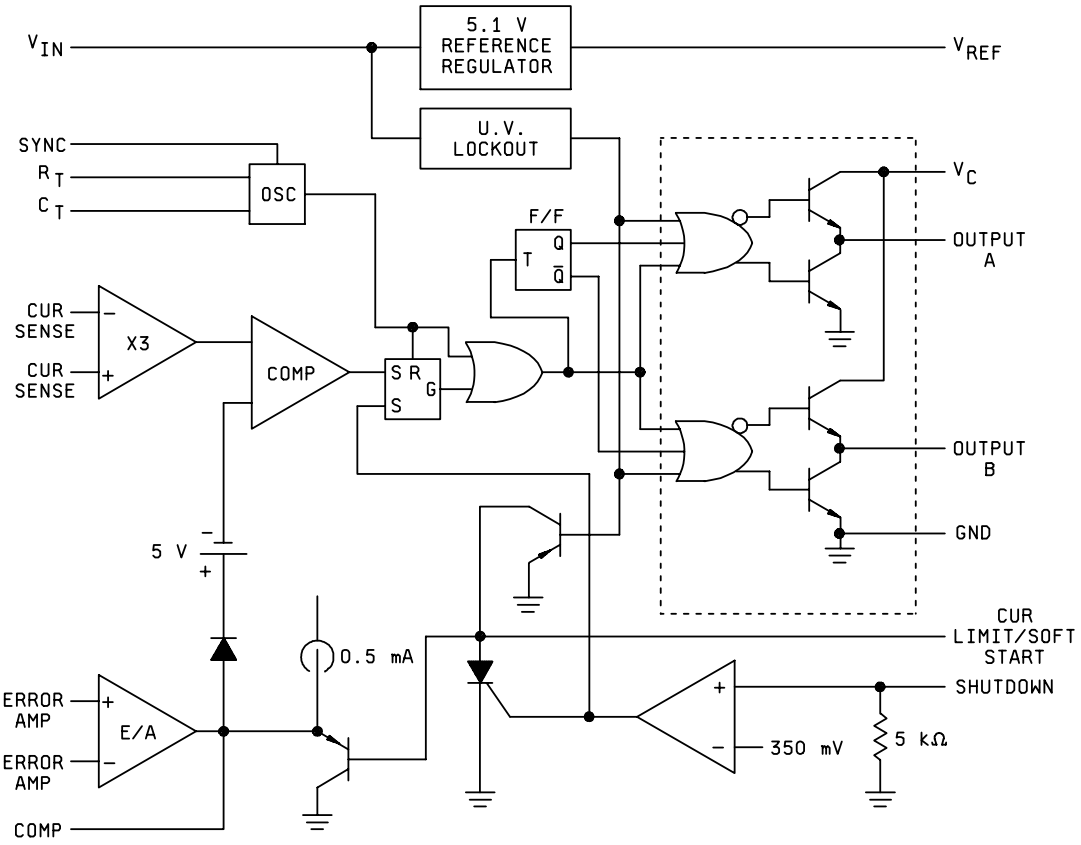


FIGURE 2. Block diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4,9 1/	1,2,3,4,9 1/	1,2,3,4,9 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6,9	1,2,3,4,5,6,9	1,2,3,4,5,6,9
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-03-04

Approved sources of supply for SMD 5962-86806 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8680601EA	01295	UC1846J/883B
	34333	SG1846J/883B
	3/	LT1846J/883B
5962-8680601FA	34333	SG1846F/883B
5962-86806012A	01295	UC1846L/883B
	34333	SG1846L/883B
5962-8680601VEA	01295	UC1846JQMLV
5962-8680601V2A	01295	UC1846LQMLV
5962-8680602EA	3/	UC1847J/883B
	3/	LT1847J/883B
	3/	SG1847J/883
5962-8680602FA	3/	SG1847F/883B
5962-86806022A	3/	UC1847L/883B
	3/	SG1847L/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
34333	Microsemi Integrated Products 11861 Western Avenue Garden Grove, CA 92641-1816