| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Change to one part one part number format. Add characterization for device classes B, S, Q, and V. Add ground bounce and latch-up immunity characterization. Add appendix for substitution data. Changes to table I. Editorial changes throughout. – jak | 92-12-22 | Monica L. Poelking |
| B | Add radiation hardness assurance limits. Editorial changes throughout. - jak | 98-05-06 | Monica L. Poelking |
| C | Add vendor CAGE F8859. Add device type device type 02. Add case outline X. Add radiation features in section 1.5. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - LTG | 04-12-01 | Thomas M. Hess |

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | C | B | C | C | C | C | C | C | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | | | | | | | | | | | | |

| REV STATUS OF SHEETS | REV | C | C | C | C | C | C | C | C | C | C | C | C | C | C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
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**DEFENSE SUPPLY CENTER COLUMBUS**
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**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89-02-07

REVISION LEVEL
C

MICROCIRCUITS, DIGITAL, ADVANCED CMOS, 8-INPUT MULTIPLEXER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

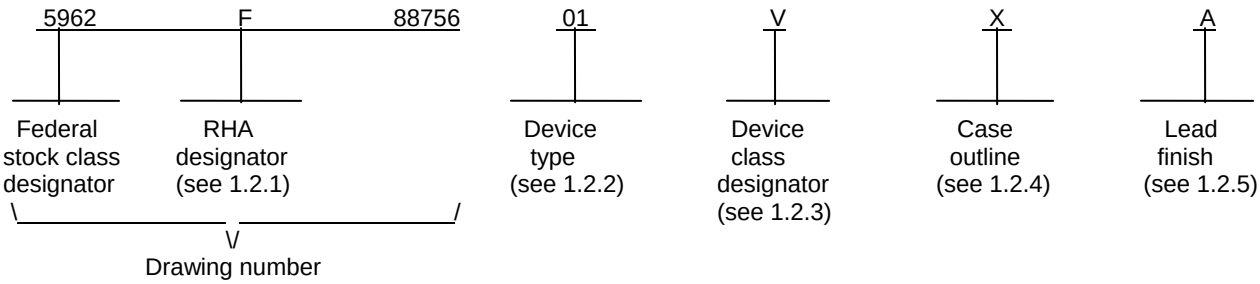
| SIZE | CAGE CODE | |
|---|---|---|
| **A** | **67268** | **5962-88756** |

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes M, B, and Q), and space application (device classes S and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN

1.2 PIN. The PIN is as shown in the following example.




1.2.1 RHA designator. Device classes B, S, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ACT151 | 8-input multiplexer, TTL compatible inputs |
| 02 | 54ACT151 | 8-input multiplexer, TTL compatible inputs |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| B, S, Q, or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| X | CDFP4-F16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +6.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC input diode current ($I_{IK}$) ($V_{IN}$ = -0.5 V, $V_{IN}$ = $V_{CC}$ + 0.5 V) | ±20 mA |
| DC output diode current ($I_{OK}$) ($V_{OUT}$ = -0.5 V, $V_{OUT}$ = $V_{CC}$ + 0.5 V) | ±20 mA |
| DC output current ($I_{OUT}$) | ±50 mA |
| DC $V_{CC}$ or GND current ($I_{CC}$, $I_{GND}$) | ±100 mA |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Maximum power dissipation ($P_D$) | 500 mW |
| Lead temperature (soldering, 10 seconds): | |
| Case outline X | +260°C |
| Other case outlines except case X | +300°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +175°C 4/ |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1.4 Recommended operating conditions. 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Input voltage range ($V_{IN}$) | +0.0 V dc to $V_{CC}$ |
| Output voltage range ($V_{OUT}$) | +0.0 V dc to $V_{CC}$ |
| Maximum low level input voltage ($V_{IL}$) | 0.8 V dc |
| Minimum high level input voltage ($V_{IH}$) | 2.0 V dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Input edge rate ($\Delta V/\Delta t$) minimum: | |
| (from $V_{IN}$ = 0.8 V to 2.0 V, 2.0 V to 0.8 V) | 125 mV/ns |
| Maximum high level output current ($I_{OH}$) | -24 mA |
| Maximum low level output current ($I_{OL}$) | 24 mA |

1.5 Radiation features.

| | |
|---|---|
| Device type 01: | |
| Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) | 100 krads (Si) |
| Single Event Latch-up (SEL) | ≥ 100 MeV–cm$^2$/mg |
| Device type 02: | |
| Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) | 300 krads (Si) |
| Single Event Latch-up (SEL) | ≥ 93 MeV–cm$^2$/mg |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

EIA/JEDEC Standard No. 78 - IC Latch-up Test.

(Copies of these documents are available online at http://www.jedec.org or from Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device classes M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes B, S, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes B, S, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes B, S, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes B, S, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes B, S, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device classes M. For device classes M notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M. Device class M devices covered by this drawing shall be in microcircuit group number 39 (see MIL-PRF-38535, appendix A).

3.11 Substitution. Substitution data shall be as indicated in the appendix herein.

4. VERIFICATION

4.1 Sampling and inspection. For device classes B, S, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes B, S, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute the first 7 test requirements of table II herein.

(4) For device class M, unless otherwise specified, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

(5) Unless otherwise specified in the QM plan for static burn-in, device classes B and S, test condition A, method 1015 of MIL-STD-883, the test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

(a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on both inputs and open outputs, and required on outputs when it is connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ.

(b) For static burn-in II, all inputs shall be connected through the R1 resistors to $V_{CC}$. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on open outputs, and required on outputs when it is connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ.

(c) $V_{CC}$ = 5.5 V +0.5 V, -0.0 V.

(6) Unless otherwise specified in the QM plan for dynamic burn-in, device classes B and S, test condition D, method 1015 of MIL-STD-883, the following shall apply:

(a) Input resistors = 220Ω to 2 kΩ ±20 percent.

(b) Output resistors = 220Ω ±20 percent.

(c) $V_{CC}$ = 5.5 V + 0.5 V, -0.0 V.

(d) The $\overline{E}$ pin shall be connected through a resistor to a clock pulse (CP1). Other inputs shall be connected to $V_{CC}$. Outputs shall be connected through the resistors to $V_{CC}/2$ ±0.5 V.

(e) CP1 = 25 kHz to 1 MHz square wave; duty cycle = 50 percent ±15 percent; $V_{IH}$ = 4.5 V to $V_{CC}$, $V_{IL}$ = 0 V ±0.5 V; $t_r$, $t_f$ ≤ 100 ns.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes B, S, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class S or V beyond the requirements of device class B or Q shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S or V devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B or Q devices shall be in accordance with MIL-PRF-38535 for static burn-in. Dynamic burn-in is not required.

d. The PDA for class M devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in and dynamic burn-in.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the specified PDA.

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ -55°C ≤ $T_C$ ≤ +125°C 4.5 V ≤ $V_{CC}$ ≤ 5.5 V unless otherwise specified | | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| High level output voltage 3006 | $V_{OH1}$ 5/ | For all inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V<br>For all other inputs<br>$V_{IN}$ = $V_{CC}$ or GND<br>$I_{OH}$ = -50µA | | All<br>All | 4.5 V | 1, 2, 3 | 4.4 | | V |
| | $V_{OH2}$ | For all inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V<br>For all other inputs<br>$V_{IN}$ = $V_{CC}$ or GND<br>$I_{OH}$ = -50µA | | All<br>All | 5.5 V | 1, 2, 3 | 5.4 | | |
| | | | M, D, P, L, R | 01<br>B, S, Q, V | | 1 | 5.4 | | |
| | $V_{OH3}$ | For all inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V<br>For all other inputs<br>$V_{IN}$ = $V_{CC}$ or GND<br>$I_{OH}$ = -24mA | | All<br>All | 4.5 V | 1, 2, 3 | 3.7 | | |
| | | | M, D, P, L, R | 01<br>B, S, Q, V | | 1 | 3.7 | | |
| | $V_{OH4}$ 5/ | For all inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V<br>For all other inputs<br>$V_{IN}$ = $V_{CC}$ or GND<br>$I_{OH}$ = -24 mA | | All<br>All | 5.5 V | 1, 2, 3 | 4.7 | | |
| | $V_{OH5}$ 6/ | For all inputs affecting output under test, $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V<br>For all other inputs<br>$V_{IN}$ = $V_{CC}$ or GND<br>$I_{OH}$ = -50mA | | All<br>All | 5.5 V | 1, 2, 3 | 3.85 | | |
| | | | M, D, P, L, R | 01<br>B, S, Q, V | | 1 | 3.85 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| Low level output voltage 3007 | $V_{OL1}$ 5/ | For all inputs affecting output under test, $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND<br>$I_{OL} = 50\ \mu A$ | | All<br>All | 4.5 V | 1, 2, 3 | | 0.1 | V |
| | $V_{OL2}$ | For all inputs affecting output under test, $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND<br>$I_{OL} = 50\ \mu A$ | | All<br>All | 5.5 V | 1, 2, 3 | | 0.1 | |
| | | | M, D, P, L, R | 01<br>B, S, Q, V | | 1 | | 0.1 | |
| | $V_{OL3}$ | For all inputs affecting output under test, $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND<br>$I_{OL} = 24\ mA$ | | All<br>B, S, Q, V | 4.5 V | 1, 3 | | 0.4 | |
| | | | | | | 2 | | 0.5 | |
| | | | | All | | 1 | | 0.4 | |
| | | | | M | | 2, 3 | | 0.5 | |
| | | | M, D, P, L, R | 01<br>B, S, Q, V | | 1 | | 0.4 | |
| | $V_{OL4}$ 5/ | For all inputs affecting output under test, $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND<br>$I_{OL} = 24\ mA$ | | All<br>B, S, Q, V | 5.5 V | 1, 3 | | 0.4 | |
| | | | | | | 2 | | 0.5 | |
| | | | | All<br>M | | 1 | | 0.4 | |
| | | | | | | 2, 3 | | 0.5 | |
| | $V_{OL5}$ 6/ | For all inputs affecting output under test, $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND<br>$I_{OL} = 50\ mA$ | | All<br>All | 5.5 V | 1, 2, 3 | | 1.65 | |
| | | | M, D, P, L, R | 01<br>B, S, Q, V | | 1 | | 1.65 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| Positive input clamp voltage 3022 | $V_{IC+}$ | For input under test | | All B, S, Q, V | 0.0 V | 1 | 0.4 | 1.5 | V |
| | | $I_{IN}$ = 1.0 mA | M, D, P, L, R | 01 B, S, Q, V | | | 0.4 | 1.5 | |
| Negative input clamp voltage 3022 | $V_{IC-}$ | For input under test | | All B, S, Q, V | Open | 1 | -0.4 | -1.5 | V |
| | | $I_{IN}$ = -1.0 mA | M, D, P, L, R | 01 B, S, Q, V | | | -0.4 | -1.5 | |
| Input current high 3010 | $I_{IH}$ | For input under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND | | All | 5.5 V | 1 | | 0.1 | µA |
| | | | | B, S, Q, V | | 2 | | 1.0 | |
| | | | | All | | 1 | | 0.1 | |
| | | | | M | | 2, 3 | | 1.0 | |
| | | | M, D, P, L, R | 01 B, S, Q, V | | 1 | | 0.1 | |
| Input current low 3009 | $I_{IL}$ | For input under test $V_{IN}$ = GND For all other inputs $V_{IN} = V_{CC}$ or GND | | All | 5.5 V | 1 | | -0.1 | µA |
| | | | | B, S, Q, V | | 2 | | -1.0 | |
| | | | | All | | 1 | | -0.1 | |
| | | | | M | | 2, 3 | | -1.0 | |
| | | | M, D, P, L, R | 01 B, S, Q, V | | 1 | | -0.1 | |
| Quiescent supply current output high 3005 | $I_{CCH}$ | For all inputs $V_{IN} = V_{CC}$ or GND | | 01 | 5.5 V | 1 | | 2.0 | µA |
| | | | | B, S, Q, V | | 2 | | 40.0 | |
| | | | | 01 M | | 1 | | 8.0 | |
| | | | | | | 2, 3 | | 160.0 | |
| | | | | 02 All | | 1 | | 2.0 | |
| | | | | | | 2, 3 | | 40.0 | |
| | | | M | | | | | 100.0 | µA |
| | | | D | 01 | | 1 | | 1.0 | mA |
| | | | P, L, R | B, S, Q, V | | | | 3.5 | |
| | | | M, D, P, L, R, F 7/ | 02 Q, V | | 1 | | 50 | µA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Quiescent supply current output low 3005 | $I_{CCL}$ | For all inputs $V_{IN} = V_{CC}$ or GND | 01 B, S, Q, V | 5.5 V | 1 | | 2.0 | µA |
| | | | | | 2 | | 40.0 | |
| | | | 01 M | | 1 | | 8.0 | |
| | | | | | 2, 3 | | 160.0 | |
| | | | 02 All | | 1 | | 2.0 | |
| | | | | | 2, 3 | | 40 | |
| | | M | 01 B, S, Q, V | | 1 | | 100.0 | µA |
| | | D | | | | | 1.0 | mA |
| | | P, L, R | | | | | 3.5 | |
| | | M, D, P, L, R, F 7/ | 02 Q, V | | 1 | | 50 | µA |
| Quiescent supply Current delta, TTL input levels 3005 | $\Delta I_{CC}$ 8/ | For input under test $V_{IN} = V_{CC} - 2.1\ V$ For all inputs $V_{IN} = V_{CC}$ or GND | 01 B, S, Q, V | 5.5 V | 3 | | 1.6 | mA |
| | | | | | 1, 2 | | 1.0 | |
| | | | 01 M | | 1, 2, 3 | | 1.6 | |
| | | | 02 All | | 1, 2, 3 | | 1.6 | |
| | | M, D | 01 B, S, Q, V | | 1 | | 1.6 | |
| | | P, L, R | | | | | 3.5 | |
| Input capacitance 3012 | $C_{IN}$ | See 4.4.1c $T_C = +25°C$ | All All | GND | 4 | | 10.0 | pF |
| Power dissipation capacitance | $C_{PD}$ 9/ | See 4.4.1c $T_C = +25°C$, f = 1 MHz | All All | 5.0 V | 4 | | 110.0 | pF |
| Latch-up input/output over-voltage | $I_{CC}$ (O/V1) 10/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $V_{over} = 10.5\ V$ See 4.4.1b | All B, S, Q, V | 5.5 V | 2 | | 200 | mA |
| Latch-up input/output positive over-current | $I_{CC}$ (O/I1+) 10/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$ See 4.4.1b | All B, S, Q, V | 5.5 V | 2 | | 200 | mA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Latch-up input/output negative over-current | $I_{CC}$ (O/I1-) 10/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$<br>$5\ \mu s \le t_r \le 5\ ms$<br>$5\ \mu s \le t_f \le 5\ ms$<br>$V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$<br>$I_{trigger} = -120\ mA$<br>See 4.4.1b | All<br>B, S, Q, V | 5.5 V | 2 | | 200 | mA |
| Latch-up supply over-voltage | $I_{CC}$ (O/V2) 10/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$<br>$5\ \mu s \le t_r \le 5\ ms$<br>$5\ \mu s \le t_f \le 5\ ms$<br>$V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$<br>$V_{over} = 9.0\ V$<br>See 4.4.1b | All<br>B, S, Q, V | 5.5 V | 2 | | 100 | mA |
| Functional tests 3014 | 11/ | $V_{IL} = 0.40\ V$<br>$V_{IH} = 2.40\ V$<br>Verify output $V_{OUT}$<br>See 4.4.1e | All<br>All | 4.5 V | 7, 8 | L | H | |
| | | | M, D, P, L, R<br>01<br>B, S, Q, V | | 7 | L | H | |
| | | $V_{IL} = 0.40\ V$<br>$V_{IH} = 2.40\ V$<br>Verify output $V_{OUT}$<br>See 4.4.1e | All<br>M | 5.5 V | 7, 8 | L | H | |
| Propagation delay time, select to output, Sn to Z or $\overline{Z}$ 3003 | $t_{PHL1}$, $t_{PLH1}$ 12/ 13/ | $C_L = 50\ pF$ minimum<br>$R_L = 500\Omega$<br>See figure 4 | All<br>B, S, Q, V | 4.5 V | 9, 11 | 1.0 | 16.0 | ns |
| | | | | | 10 | 1.0 | 20.0 | |
| | | | All<br>M | | 9 | 1.0 | 16.0 | |
| | | | | | 10, 11 | 1.0 | 20.0 | |
| | | | M, D, P, L, R<br>01<br>B, S, Q, V | 4.5 V | 9 | 1.0 | 16.0 | |
| Propagation delay time, data to output, Im to Z or $\overline{Z}$ 3003 | $t_{PHL2}$, $t_{PLH2}$ 12/ 13/ | $C_L = 50\ pF$ minimum<br>$R_L = 500\Omega$<br>See figure 4 | All<br>B, S, Q, V | 4.5 V | 9, 11 | 1.0 | 13.0 | ns |
| | | | | | 10 | 1.0 | 16.0 | |
| | | | All<br>M | | 9 | 1.0 | 13.0 | |
| | | | | | 10, 11 | 1.0 | 16.0 | |
| | | | M, D, P, L, R<br>01<br>B, S, Q, V | | 9 | 1.0 | 13.0 | |
| Propagation delay time, enable to output, $\overline{E}$ to Z or $\overline{Z}$ 3003 | $t_{PHL3}$, $t_{PLH3}$ 12/ 13/ | $C_L = 50\ pF$ minimum<br>$R_L = 500\Omega$<br>See figure 4 | All<br>B, S, Q, V | 4.5 V | 9, 11 | 1.0 | 10.5 | ns |
| | | | | | 10 | 1.0 | 12.5 | |
| | | | All<br>M | | 9 | 1.0 | 10.5 | |
| | | | | | 10, 11 | 1.0 | 12.5 | |
| | | | M, D, P, L, R<br>01<br>B, S, Q, V | | 9 | 1.0 | 10.5 | |

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in MIL-STD-883 [e.g. $I_{CC}$(O/V1)], utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. $V_{IC}$ (pos) tests, the GND terminal can be open. $T_C$ = +25°C.
b. $V_{IC}$ (neg) tests, the $V_{CC}$ terminal shall be open. $T_C$ = +25°C.
c. All $I_{CC}$ and $\Delta I_{CC}$ tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 are tested at all levels M, D, P, L, and R of irradiation. Pre and post irradiation values are identical unless otherwise specified in table I.

RHA parts for device type 02 meet all levels M, D, P, L, R, and F of irradiation. Pre and post irradiation values are identical unless otherwise specified in table I.

When performing post irradiation electrical measurements for any RHA level for any device, $T_A$ = +25 °C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

5/ For device classes B, S, Q, and V, this test is guaranteed, if not tested, to the limits specified in table I.

6/ Transmission driving tests are performed at $V_{CC}$ = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN}$ = 2.0 V or 0.8 V.

7/ The maximum limit for this parameter at 100 krads (Si) is 2 μA.

8/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0.0 V or $V_{CC}$. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits is equal to the number of inputs at a high TTL input level times $\Delta I_{CC}$ maximum limit; and the preferred method and limits are guaranteed.

9/ Power dissipation capacitance ($C_{PD}$) determines the no load dynamic power consumption ($P_D$) and the dynamic current consumption ($I_S$), where:

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$

f is the frequency of the input signal; n is the number of device inputs at TTL levels; d is the duty cycle of the input signal; and $C_L$ is the external output load capacitance.

10/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and $V_{over}$ are to be accurate within ±5 percent.

11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated.

12/ Device classes B, S, Q, and V are tested at $V_{CC}$ = 4.5 V at $T_C$ = +125°C for sample testing and at $V_{CC}$ = 4.5 V at $T_C$ = +25°C for screening. Other voltages of $V_{CC}$ and temperatures are guaranteed, if not tested to the limits specified in table I (see 4.4.1d).

TABLE I. Electrical performance characteristics - Continued.

13/ AC limits at $V_{CC}$ = 5.5 V are equal to the limits at $V_{CC}$ = 4.5 V and guaranteed by testing at $V_{CC}$ = 4.5 V. Minimum ac limits for $V_{CC}$ = 5.5 V are 1.0 ns and guaranteed by guardbanding the $V_{CC}$ = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

| Device types | 01 and 02 | |
|---|---|---|
| Case outlines | E, F, and X | 2 |
| Terminal number | Terminal symbol | |
| 1 | I3 | NC |
| 2 | I2 | I3 |
| 3 | I1 | I2 |
| 4 | I0 | I1 |
| 5 | Z | I0 |
| 6 | $\overline{Z}$ | NC |
| 7 | $\overline{E}$ | Z |
| 8 | GND | $\overline{Z}$ |
| 9 | S2 | $\overline{E}$ |
| 10 | S1 | GND |
| 11 | S0 | NC |
| 12 | I7 | S2 |
| 13 | I6 | S1 |
| 14 | I5 | S0 |
| 15 | I4 | I7 |
| 16 | $V_{CC}$ | NC |
| 17 | - - - | I6 |
| 18 | - - - | I5 |
| 19 | - - - | I4 |
| 20 | - - - | $V_{CC}$ |

NC = No connection.

| Terminal description | |
|---|---|
| Terminal symbol | Description |
| Im (m = 0 to 7) | Data inputs |
| Sn (n = 0 to 2) | Asynchronous select control inputs |
| $\overline{E}$ | Enable control input (active low) |
| Z, $\overline{Z}$ | Outputs (noninverting, inverting) |

FIGURE 1. Terminal connections.

| Device types 01 and 02 | | | | | |
|---|---|---|---|---|---|
| Inputs | | | | Outputs | |
| $\overline{E}$ | S2 | S1 | S0 | $\overline{Z}$ | Z |
| H | X | X | X | H | L |
| L | L | L | L | I0 | I0 |
| L | L | L | H | I1 | I1 |
| L | L | H | L | I2 | I2 |
| L | L | H | H | I3 | I3 |
| L | H | L | L | I4 | I4 |
| L | H | L | H | I5 | I5 |
| L | H | H | L | I6 | I6 |
| L | H | H | H | I7 | I7 |

H - High level voltage
L = Low level voltage
X = Irrelevant

FIGURE 2. Truth Table.

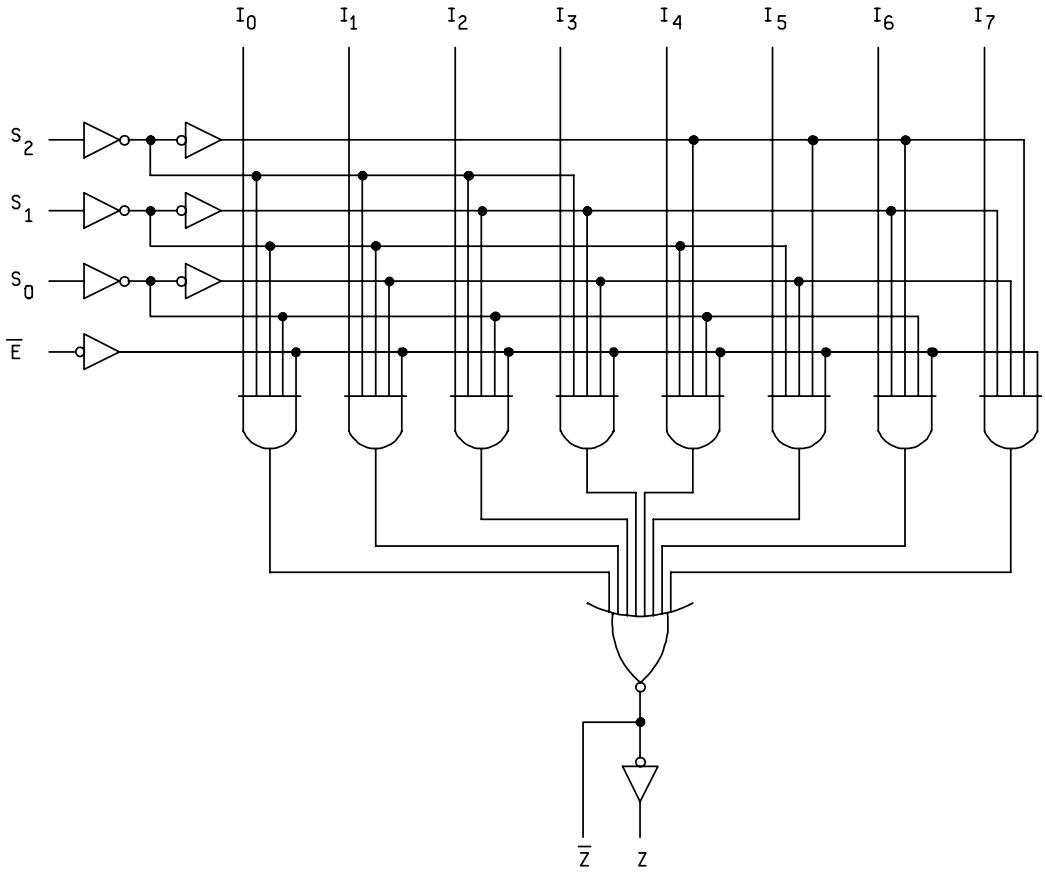



FIGURE 3. Logic diagram.

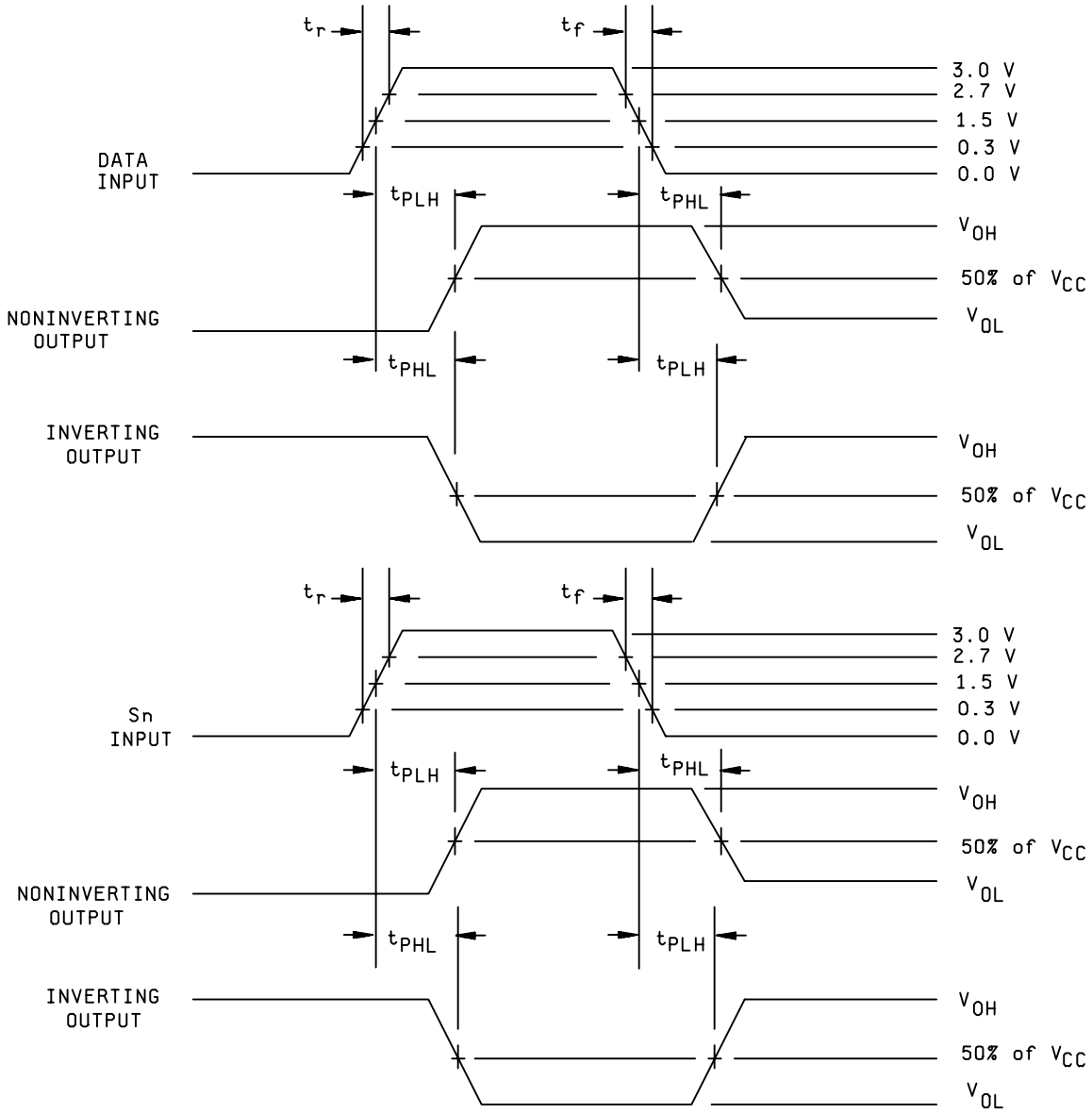
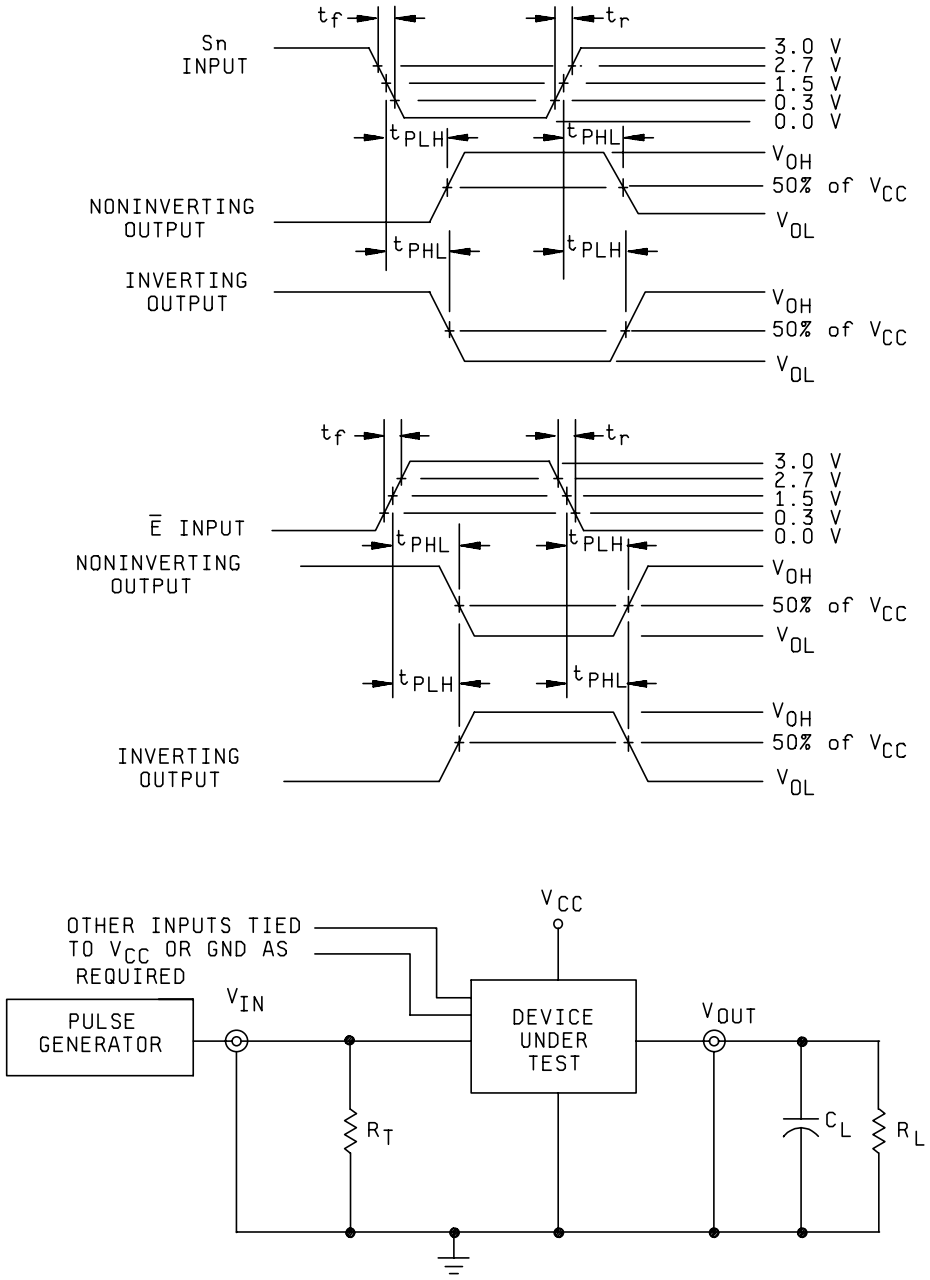



FIGURE 4. Switching waveforms and test circuit .




NOTES:
1. $C_L$ = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. $R_T$ = 50Ω or equivalent, $R_L$ = 500Ω or equivalent.
3. Input signal from pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r$ ≤ 3.0 ns; $t_f$ ≤ 3.0 ns; $t_r$ and $t_f$ shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit - Continued.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups 1/ (in accordance with MIL-STD-883, method 5005, table I) | Subgroups 1/ (in accordance with MIL-PRF-38535, table III) | | | |
|---|---|---|---|---|---|
| | Device class M | Device 2/ class B | Device 2/ class S | Device class Q | Device class V |
| Interim electrical parameters, method 5004 | | 1 | 1 | 1 | 1 |
| Static burn-in I, method 1015 (see 4.2.1a) | 3/ | Not required | Required 4/ | Not required | Required 4/ |
| Interim electrical parameters, method 5004 (see 4.2.1b) | | | 1 5/ | | 1 5/ |
| Static burn-in II, method 1015 (see 4.2.1a) | 3/ | Required 6/ | Required 4/ | Required 6/ | Required 4/ |
| Interim electrical parameters, method 5004 (see 4.2.1b) | | 1 2/ 5/ | 1 2/ 5/ | 1 2/ 5/ | 1 2/ 5/ |
| Dynamic burn-in I, method 1015 (see 4.2.1a) | 3/ | Not required | Required 4/ | Not required | Required 4/ |
| Interim electrical parameters, method 5004 (see 4.2.1b) | | | 1 5/ | | 1 5/ |
| Final electrical parameters, method 5004 | 2/ 1,2,3, 7,8,9 | 2/ 6/ 1,2, 7,9 | 1,2,7,9 2/ | 2/ 6/ 1,2,3, 7,8,9,10,11 | 2/ 1,2,3 7,8,9,10,11 |
| Group A test requirements method 5005 (see 4.4.1) | 1,2,3,4,7, 8,9,10,11 | 1,2,3,4,7, 8,9,10,11 | 1,2,3,4,7, 8,9,10,11 | 1,2,3,4,7, 8,9,10,11 | 1,2,3,4,7, 8,9,10,11 |
| Group B end point electrical parameters, method 5005 (see 4.4.2) | | | 5/ 1,2,3,7, 8,9,10,11 | | |
| Group C end-point electrical parameters, method 5005 (see 4.4.3) | 1,2,3 | 1,2 5/ | | 1,2,3 5/ | 5/ 1,2,3,7, 8,9,10,11 |
| Group D end-point electrical parameters, method 5005 (see 4.4.4) | 1,2,3 | 1,2 | 1,2,3 | 1,2,3 | 1,2,3 |
| Group E end-point electrical parameters, method 5005 (see 4.4.5) | 1,7,9 | 1,7,9 | 1,7,9 | 1,7,9 | 1,7,9 |

1/ Blank spaces indicate tests are not applicable.
2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).
3/ The burn-in shall meet the requirements of 4.2.1a herein.
4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.
5/ Delta limits shall be required only on table I, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table III.
6/ The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias) or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table II).

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

| Parameter 1/ | Symbol | Device types | Delta limits |
|---|---|---|---|
| Supply current | $I_{CCH}$, $I_{CCL}$ | 01 | ±100 nA 2/ |
| | | 02 | ±300 nA |
| Supply current delta | $\Delta I_{CC}$ | 02 | ±0.4 mA |
| Input current low level | $I_{IL}$ | 02 | ±20 nA |
| Input current high level | $I_{IH}$ | 02 | ±20 nA |
| Output voltage low level $V_{CC}$ = 5.5 V, $I_{OL}$ = 24 mA | $V_{OL}$ | 02 | ±0.04 V |
| Output voltage high level $V_{CC}$ = 5.5 V, $I_{OH}$ = -24 mA | $V_{OH}$ | 02 | ±0.20 V |

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ Guaranteed, if not tested.

4.3 Qualification inspection for device classes B, S, Q, and V. Qualification inspection for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

c. $C_{IN}$ and $C_{PD}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. $C_{PD}$ shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For $C_{IN}$ and $C_{PD}$, test all applicable pins on five devices with zero failures.

d. For device classes B, S, Q, and V, subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table on figure 2 herein. The test vectors used to verify the truth table shall test all possible input to output logic patterns. For device classes B, S, Q and V, subgroups 7 and 8 tests shall include verifying the functionality of the device

4.4.2 Group B inspection. When applicable, the group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes B, S, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes B, S, Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, B, S, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Device type 01:

(1) Inputs tested high, $V_{CC}$ = 5.5 V dc +5%, $R_{CC}$ = 10Ω ±20%, $V_{IN}$ = 5.0 V dc +5%, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested low, $V_{CC}$ = 5.5 V dc +5%, $R_{CC}$ = 10Ω ±20%, $V_{IN}$ = 0.0 V dc, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

b. Device type 02:

(1) Inputs tested high, $V_{CC}$ = 5.5 V dc ±5%, $V_{IN}$ = 5.0 V dc +10%, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested low, $V_{CC}$ = 5.5 V dc ±5%, $V_{IN}$ = 0.0 V dc, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

4.4.5.1.1 Accelerated aging test. Accelerated aging shall be performed on class M, B, S, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes B, S, Q, and V. Sources of supply for device classes B, S, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A

A.1 SCOPE

A.1.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. For new designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing designs prior to the date of this document, the new PIN can be used in lieu of the old PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 SUBSTITUTION DATA

| New PIN | Old PIN |
|---|---|
| 5962-8875601MEA | 5962-8875601EA |
| 5962-8875601MFA | 5962-8875601FA |
| 5962-8875601M2A | 5962-88756012A |

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-12-01

Approved sources of supply for SMD 5962-88756 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/SMCR/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8875601EA | 3/ | 54ACT151DMQB |
| 5962-8875601FA | 3/ | 54ACT151FMQB |
| 5962-88756012A | 3/ | 54ACT151LMQB |
| 5962-8875601MEA | 27014 | 54ACT151DMQB |
| 5962-8875601MFA | 27014 | 54ACT151FMQB |
| 5962-8875601M2A | 27014 | 54ACT151LMQB |
| 5962-8875601BEA | 3/ | JM54ACT151BEA |
| 5962-8875601BFA | 3/ | JM54ACT151BFA |
| 5962-8875601B2A | 3/ | JM54ACT151B2A |
| 5962-8875601SEA | 3/ | JM54ACT151SEA |
| 5962-8875601SFA | 3/ | JM54ACT151SFA |
| 5962-8875601S2A | 3/ | JM54ACT151S2A |
| 5962R8875601BEA | 27014 | JM54ACT151BEA-R |
| 5962R8875601BFA | 27014 | JM54ACT151BFA-R |
| 5962R8875601B2A | 27014 | JM54ACT151B2A-R |
| 5962R8875601SEA | 27014 | JM54ACT151SEA-R |
| 5962R8875601SFA | 27014 | JM54ACT151SFA-R |
| 5962R8875601S2A | 27014 | JM54ACT151S2A-R |

See footnotes on next sheet.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8875602QXA | F8859 | 54ACT151K02Q |
| 5962-8875602QXC | F8859 | 54ACT151K01Q |
| 5962-8875602VXA | F8859 | 54ACT151K02V |
| 5962-8875602VXC | F8859 | 54ACT151K01V |
| 5962F8875602QXA | F8859 | RHFACT151K02Q |
| 5962F8875602QXC | F8859 | RHFACT151K01Q |
| 5962F8875602VXA | F8859 | RHFACT151K02V |
| 5962F8875602VXC | F8859 | RHFACT151K01V |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 27014 | National Semiconductor<br>2900 Semiconductor Drive<br>P.O. Box 58090<br>Santa Clara, CA 95052-8090 |
| F8859 | ST Microelectronics<br>3 rue de Suisse<br>BP4199<br>35041 RENNES cedex2-FRANCE |