



512Kx32 5V FLASH MODULE

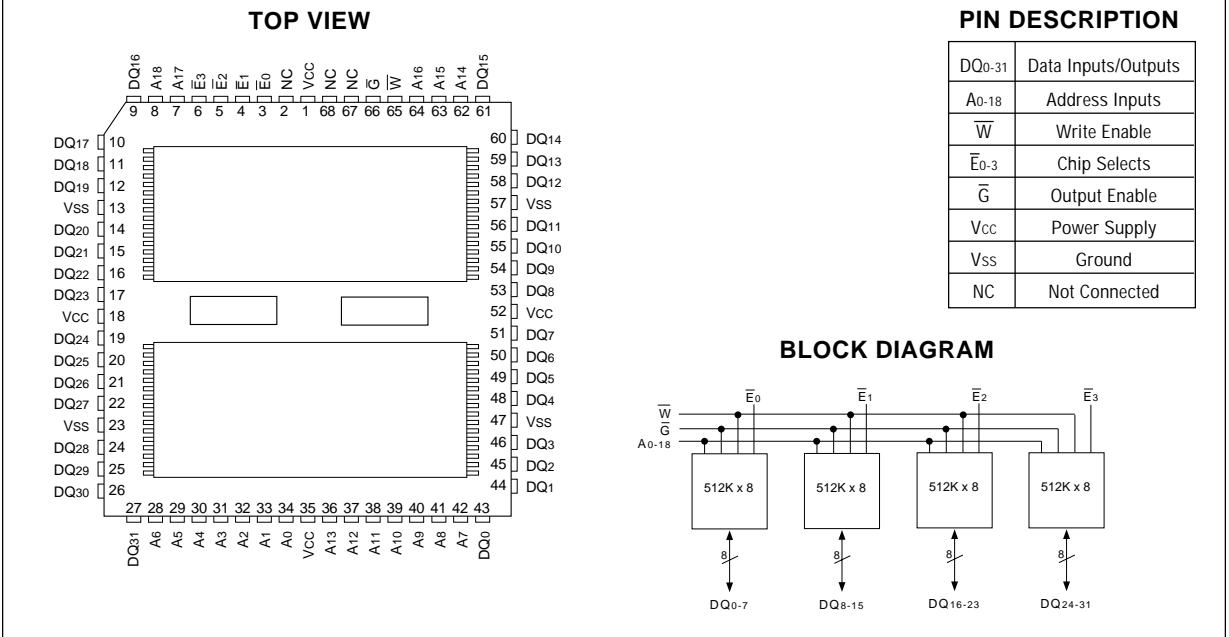
PRELIMINARY*

FEATURES

- Access Times of 60, 90ns
- Based on AMD: AM29F040B-xxEC
- Packaging
 - 68 Lead, Plastic PLCC, 24.94 mm (0.982 inch) square
- Minimum 100,000 Write/Erase Cycles
- Sector Architecture
 - 8 equal size sectors of 64KBytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx32
- Commercial and Industrial Temperature Ranges
- 5 Volt Programming. 5V ±10% Supply
- Low Power CMOS, 500µA Standby
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time
- Built-in Decoupling Caps for Low Noise Operation

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

FIG. 1 PIN CONFIGURATION FOR WED7F325ZXE5SJ-C/A





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature (Com)	0 to +70	°C
Operating Temperature (Ind.)	-40 to +85	°C
Supply Voltage Range (V _{CC})	-2.0 to +7.0	V
Signal Voltage Range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-55 to +125	°C
Data Retention	10 years	
Endurance (write/erase cycles)	100,000 cycles min.	
A ₉ Voltage for Sector Protect (V _{ID}) (3)	-2.0 to +14.0	V

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A₉ pin is -0.5V. During voltage transitions, A₉ may overshoot V_{SS} to -2V for periods of up to 20ns. Maximum DC input voltage on A₉ is +13.5V which may overshoot to 14.0 V for periods up to 20ns.
- Recommended soldering temperature not to exceed 215°C for 20 seconds.**

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Com)	T _A	0	+70	°C
Operating Temp. (Ind)	T _A	-40	+85	°C
A ₉ Voltage for Sector Protect	V _{ID}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\bar{C} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	35	pF
\bar{W} capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	35	pF
\bar{E}_{0-3} capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	12	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	15	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	35	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	Conditions			Unit
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = V _{SS} or V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = V _{SS} or V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\bar{C}\bar{S}$ = V _{IL} , $\bar{O}\bar{E}$ = V _{IH} , f = 5MHz		170	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\bar{C}\bar{S}$ = V _{IL} , $\bar{O}\bar{E}$ = V _{IH}		240	mA
V _{CC} Standby Current	I _{CC4}	V _{CC} = 5.5, $\bar{C}\bar{S}$ = V _{IH} , f = 5MHz		500	μA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\bar{O}\bar{E}$ at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \bar{E} CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol		-60		-70		-90		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{wc}	60		70		90		100		ns
Write Enable Setup Time	t _{wLEL}	t _{ws}	0		0		0		0		ns
Chip Select Pulse Width	t _{ELEH}	t _{CP}	30		35		45		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	25		30		45		45		ns
Data Hold Time	t _{EHDX}	t _{DH}	0		0		0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	40		40		45		45		ns
Chip Select Pulse Width High	t _{EHEL}	t _{CPH}	20		20		20		20		ns
Duration of Byte Programming Operation	t _{WHWH1}			1		1		1		1	ms
Sector Erase Time	t _{WHWH2}			30		30		30		30	sec
Read Recovery Time	t _{GH}	t _{HEL}	0		0		0		0		μs
Chip Programming Time				25		25		25		25	sec
Chip Erase Time	t _{WHWH2}			120		120		120		120	sec



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{WE} CONTROLLED

(V_{CC} = 5.0V, T_A = -40°C to +85°C)

Parameter	Symbol		-60		-70		-90		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		70		90		100		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	30		35		45		50		ns
Address Setup Time	t _{AVWH}	t _{AS}	0		0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	25		30		45		45		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		ns
Address Hold Time	t _{WHAX}	t _{AH}	40		40		45		45		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		ns
Duration of Byte Programming Operation	t _{WHWH1}			1		1		1		1	ms
Sector Erase	t _{WHWH2}			30		30		30		30	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		0		μs
V _{CC} Set-up Time	t _{VCS}		50		60		80		90		μs
Chip Programming Time				50		60		80		90	sec
Output Enable Setup Time		t _{oES}	0		0		0		0		ns
Output Enable Hold Time (1)		t _{oEH}	10		10		10		10		ns
Chip Erase Time	t _{WHWH2}			120		120		120		120	sec

1. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -40°C to +85°C)

Parameter	Symbol		-60		-70		-90		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	60		70		90		100		ns
Address Access Time	t _{AVOV}	t _{ACC}		60		70		90		100	ns
Chip Select Access Time	t _{ELOV}	t _{CCE}		60		70		90		100	ns
Output Enable to Output Valid	t _{GLOV}	t _{OE}		25		30		35		40	ns
Chip Select to Output High Z (1)	t _{EH0Z}	t _{DF}		18		18		20		20	ns
Output Enable High to Output High Z (1)	t _{GH0Z}	t _{DF}		18		18		20		20	ns
Output Hold from Address, \overline{E} or \overline{G} Change, whichever is First	t _{AXOX}	t _{OH}	0		0		0		0		ns

1. Guaranteed by design, but not tested.



FIG. 2
AC WAVEFORMS FOR READ OPERATIONS

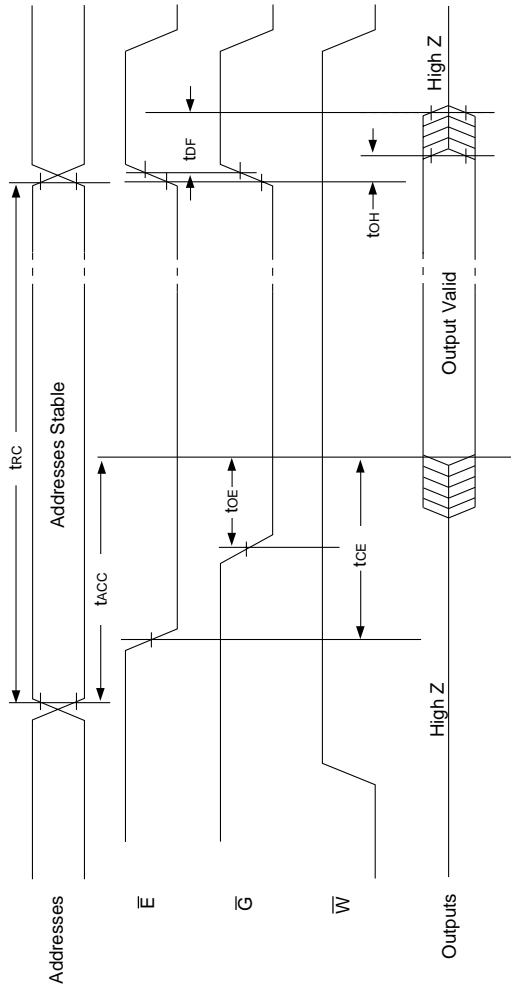
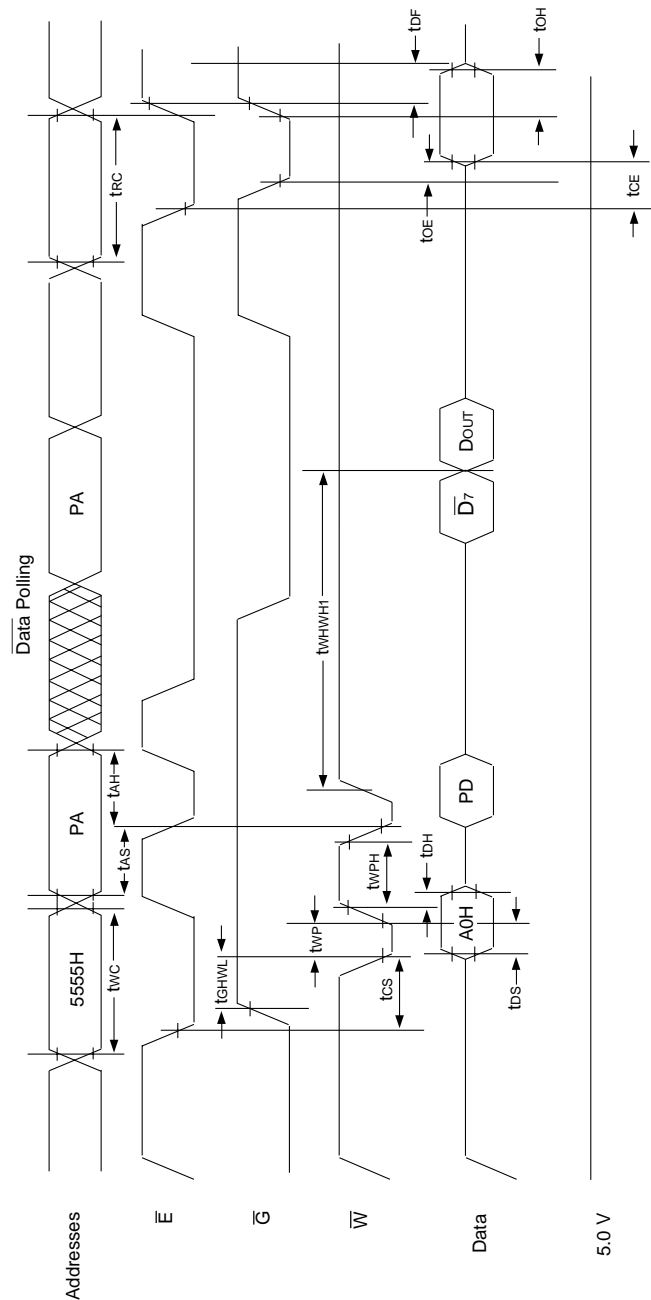




FIG. 3
WRITE/ERASE/PROGRAM
OPERATION, \bar{W} CONTROLLED

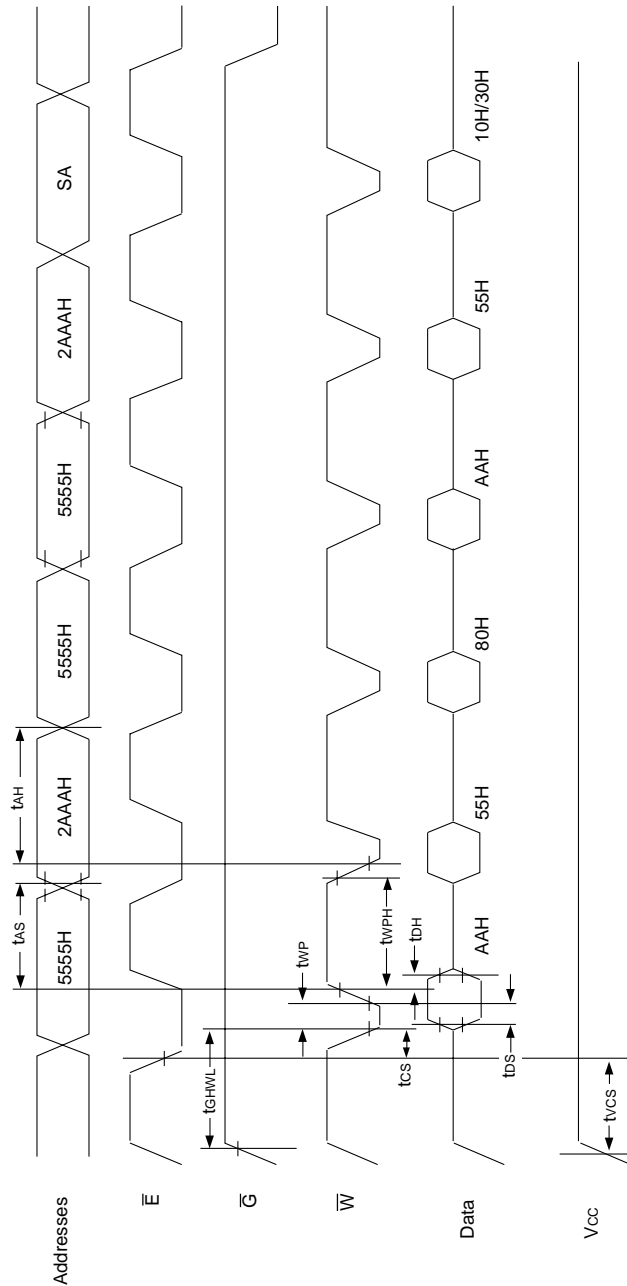


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. D0ut is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 4
AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS



NOTE:
 1. SA is the sector address for sector Erase.



FIG. 5
AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS

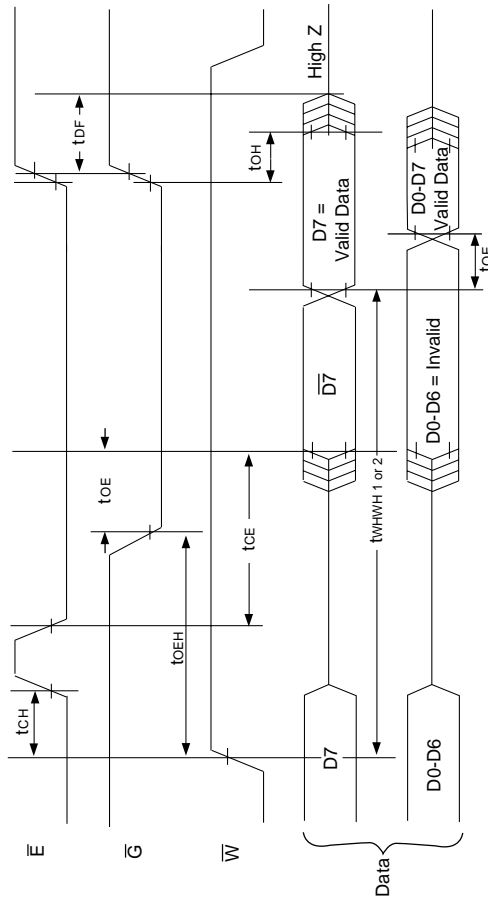
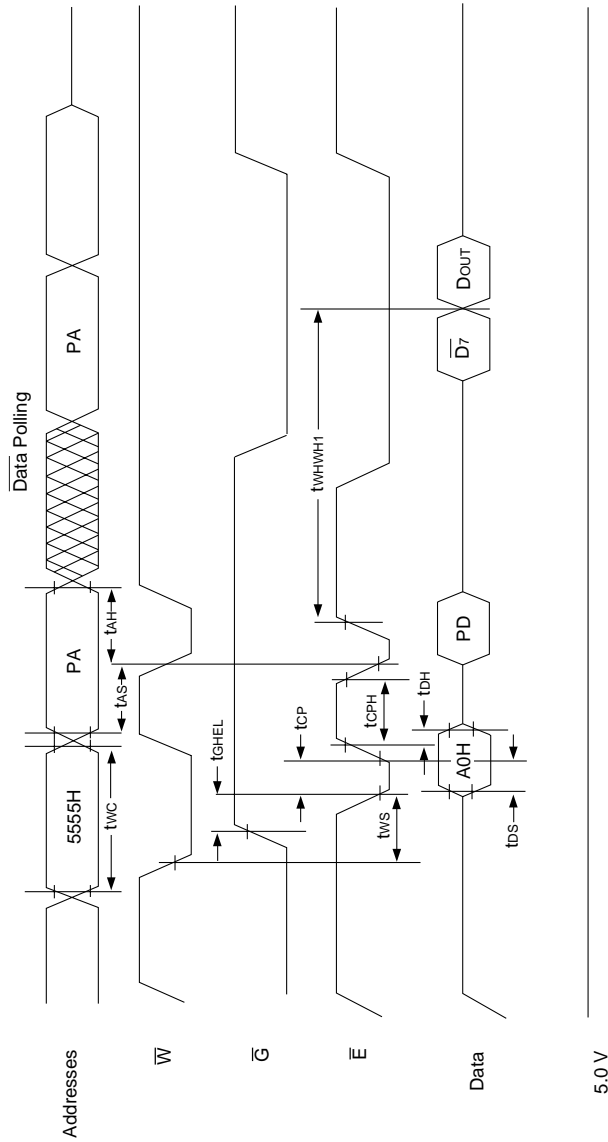




FIG. 6
ALTERNATE \bar{E} CONTROLLED
PROGRAMMING OPERATION TIMINGS

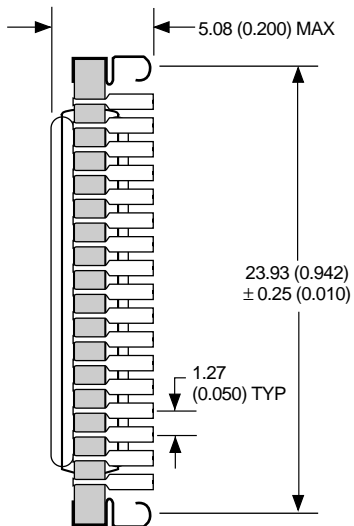
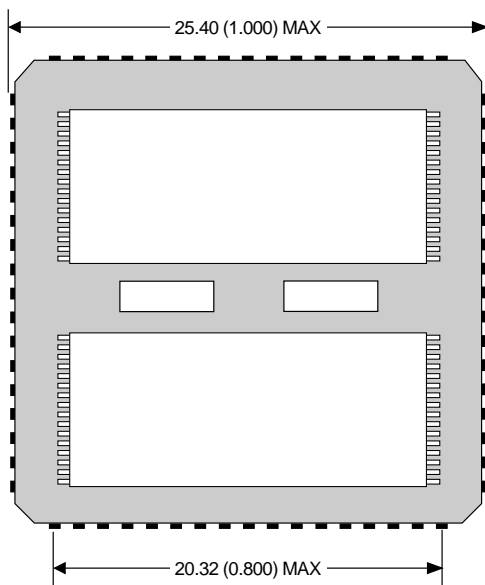


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\bar{D}7$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



PACKAGE DIMENSION: 68 LEAD PLASTIC PLCC



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

WED 7 F 32 5Z X E 5 S J - C/A

