



# IMPORTANT NOTICE

10 December 2015

## 1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors





# BTA204S-600D

3Q Hi-Com Triac

11 August 2014

Product data sheet

## 1. General description

Planar passivated three quadrant triac in a SOT428 (DPAK) surface-mountable plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High blocking voltage capability
- High commutation capability with very sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

## 3. Applications

- AC solenoids
- General purpose motor control circuits
- Home appliances

## 4. Quick reference data

Table 1. Quick reference data

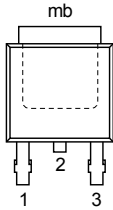

| Symbol                        | Parameter                            | Conditions  | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|---|-----|-----|-----|------|
| $V_{DRM}$                     | repetitive peak off-state voltage    |   | -   | -   | 600 | V    |
| $I_{TSM}$                     | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ;<br>$t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | -   | 25  | A    |
| $I_{T(RMS)}$                  | RMS on-state current                 | full sine wave; $T_{mb} \leq 107\text{ °C}$ ; <a href="#">Fig. 1</a> ;<br><a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>       | -   | -   | 4   | A    |
| <b>Static characteristics</b> |                                      |   |     |     |     |      |
| $I_{GT}$                      | gate trigger current                 | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>                           | -   | -   | 5   | mA   |



| Symbol | Parameter | Conditions   | Min | Typ | Max | Unit |
|--------|-----------|--|-----|-----|-----|------|
|        |           | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G-;$<br>$T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a> | -   | -   | 5   | mA   |
|        |           | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G-;$<br>$T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a> | -   | -   | 5   | mA   |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description                    | Simplified outline  | Graphic symbol   |
|-----|--------|--------------------------------|---|--|
| 1   | T1     | main terminal 1                |  <p style="text-align: center;"><b>DPAK (SOT428)</b></p> |  <p style="text-align: center;"><i>sym051</i></p> |
| 2   | T2     | main terminal 2                |   |  |
| 3   | G      | gate                           |   |  |
| mb  | T2     | mounting base; main terminal 2 |   |  |

## 6. Ordering information

**Table 3. Ordering information**

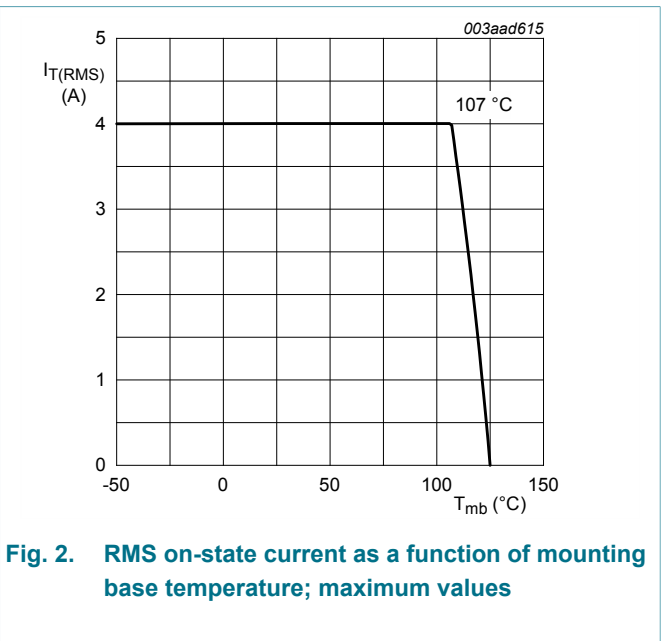
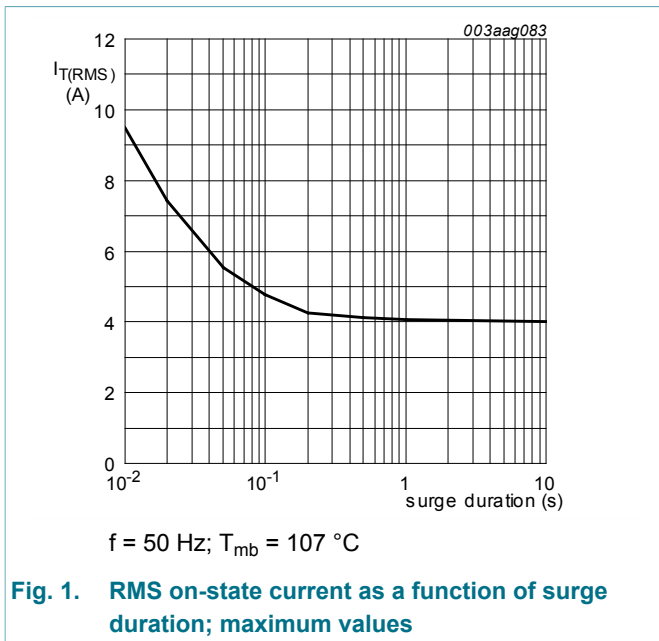
| Type number  | Package |   |         |
|--------------|---------|---|---------|
|              | Name    | Description   | Version |
| BTA204S-600D | DPAK    | plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) | SOT428  |

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol       | Parameter                            | Conditions   | Min | Max | Unit                   |
|--------------|--------------------------------------|--|-----|-----|------------------------|
| $V_{DRM}$    | repetitive peak off-state voltage    |  | -   | 600 | V                      |
| $I_{T(RMS)}$ | RMS on-state current                 | full sine wave; $T_{mb} \leq 107\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>       | -   | 4   | A                      |
| $I_{TSM}$    | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | 25  | A                      |
|              |                                      | full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$   | -   | 27  | A                      |
| $I^2t$       | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; SIN   | -   | 3.1 | $\text{A}^2\text{s}$   |
| $dl_T/dt$    | rate of rise of on-state current     | $I_T = 6\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$   | -   | 100 | $\text{A}/\mu\text{s}$ |
| $I_{GM}$     | peak gate current                    |  | -   | 2   | A                      |
| $P_{GM}$     | peak gate power                      |  | -   | 5   | W                      |
| $P_{G(AV)}$  | average gate power                   | over any 20 ms period  | -   | 0.5 | W                      |
| $T_{stg}$    | storage temperature                  |  | -40 | 150 | $^{\circ}\text{C}$     |
| $T_j$        | junction temperature                 |  | -   | 125 | $^{\circ}\text{C}$     |



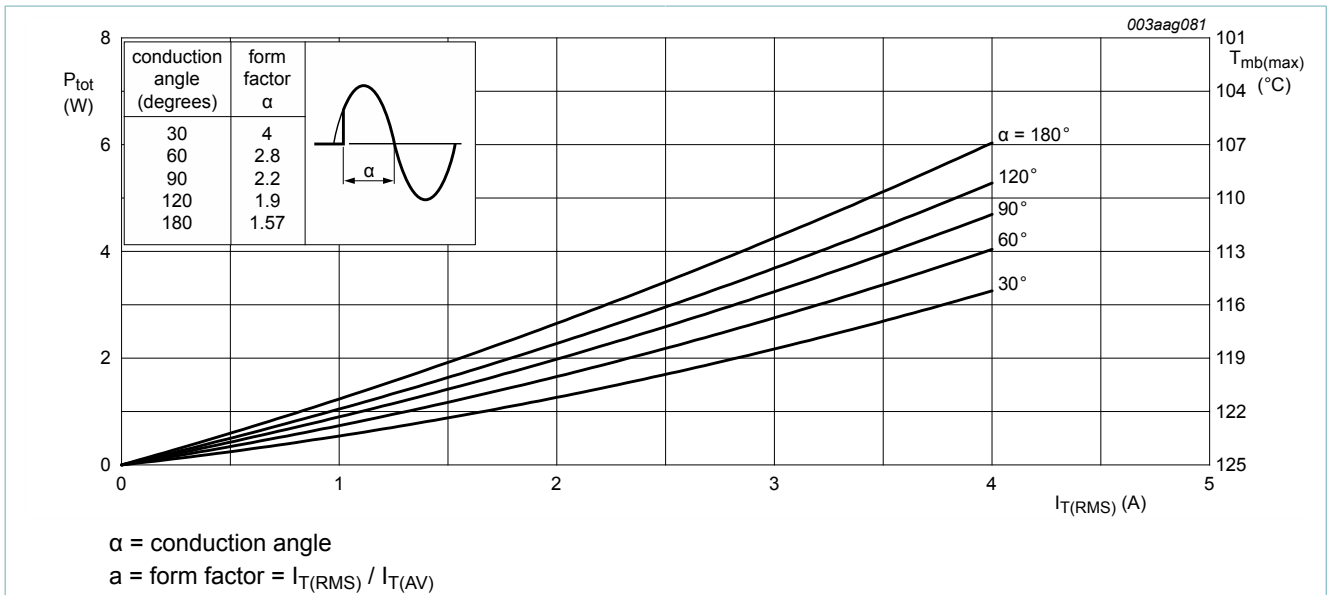


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

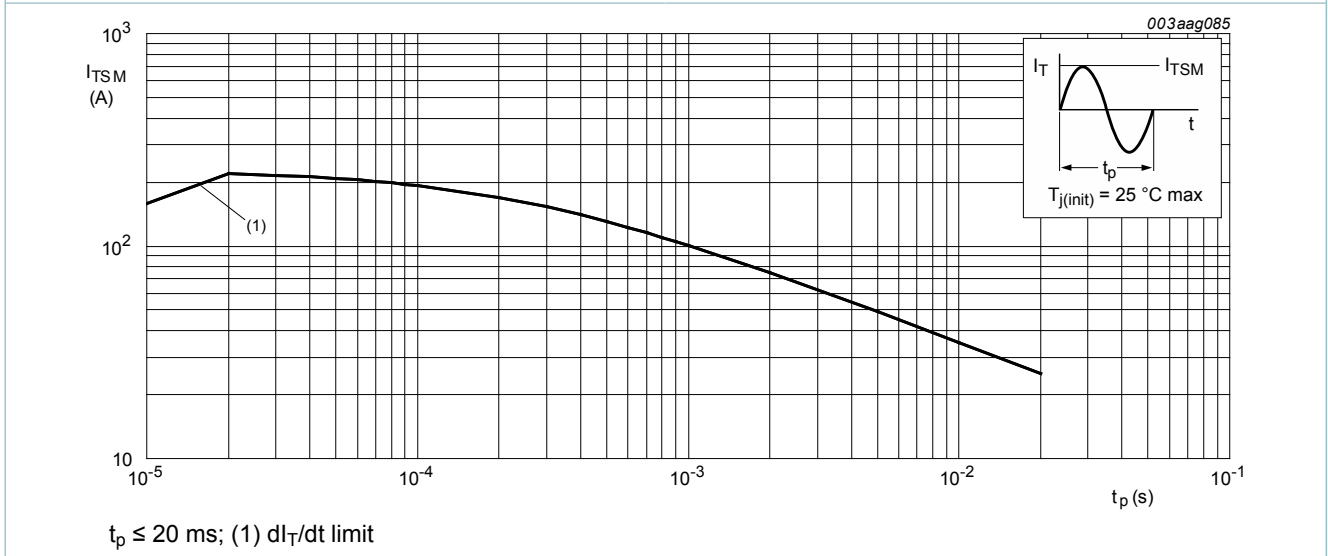
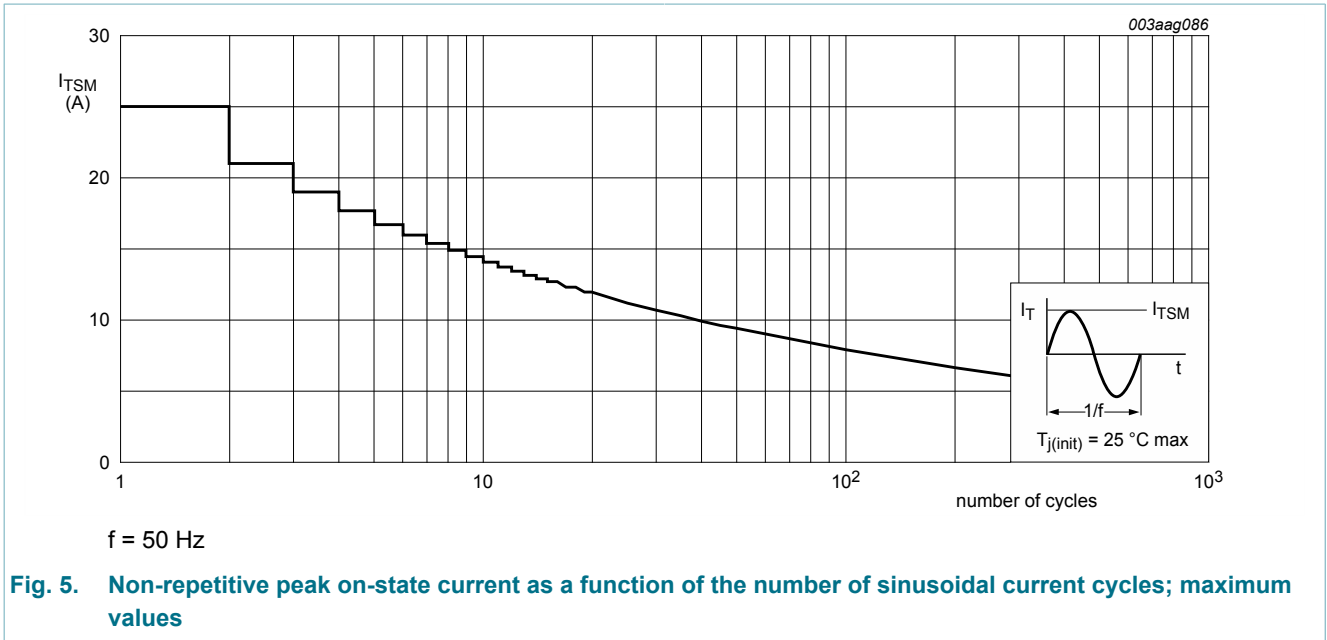


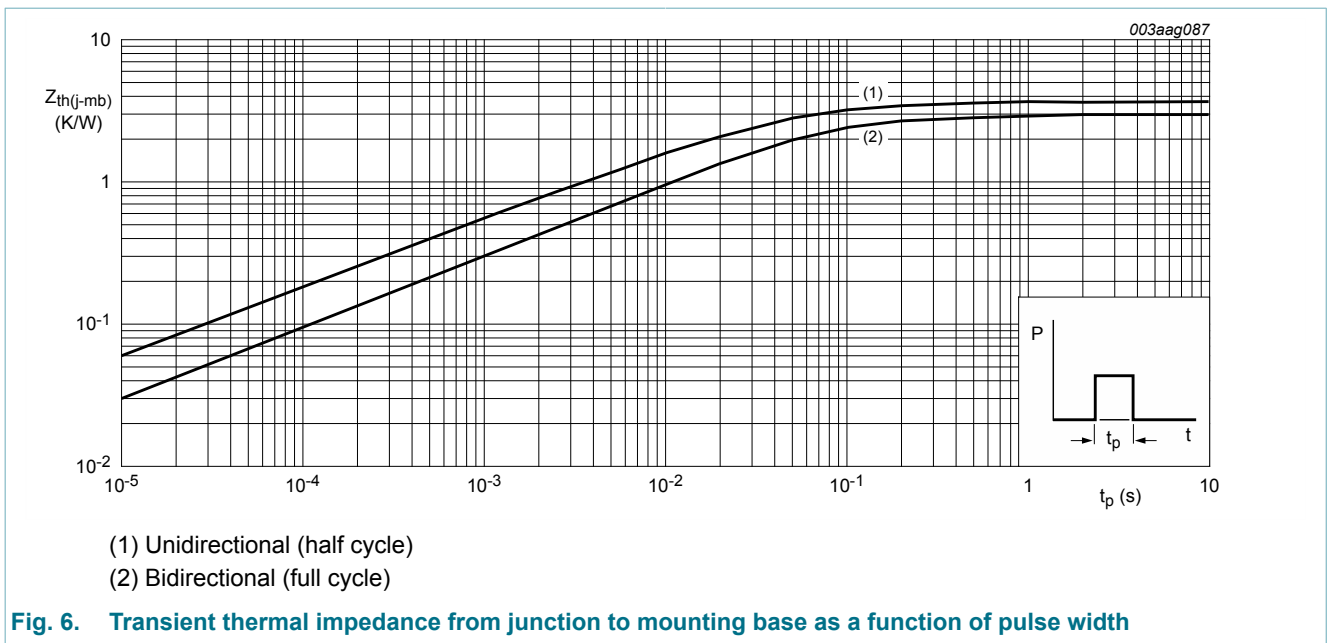
Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



### 8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter   | Conditions                          | Min | Typ | Max | Unit |
|----------------|---|-------------------------------------|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | full cycle; <a href="#">Fig. 6</a>  | -   | -   | 3   | K/W  |
|                |   | half cycle; <a href="#">Fig. 6</a>  | -   | -   | 3.7 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | printed circuit board (FR4) mounted | -   | 75  | -   | K/W  |

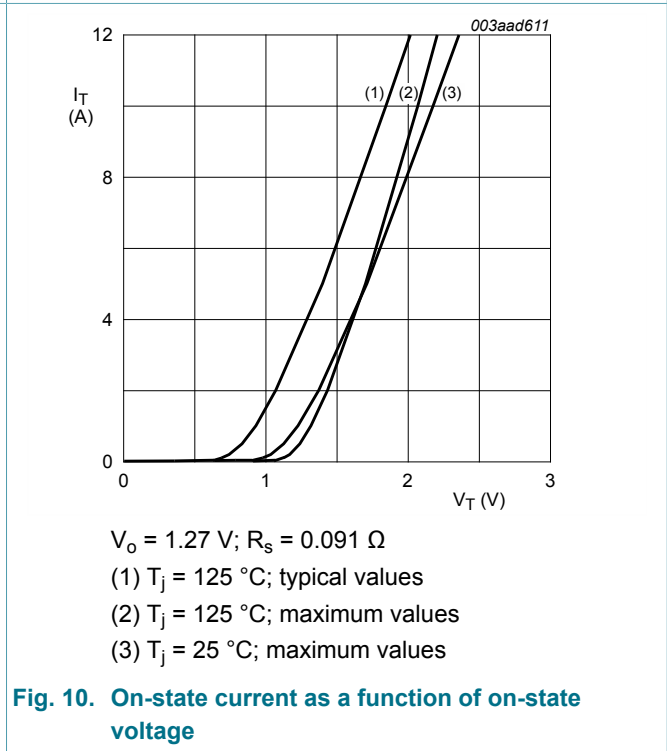
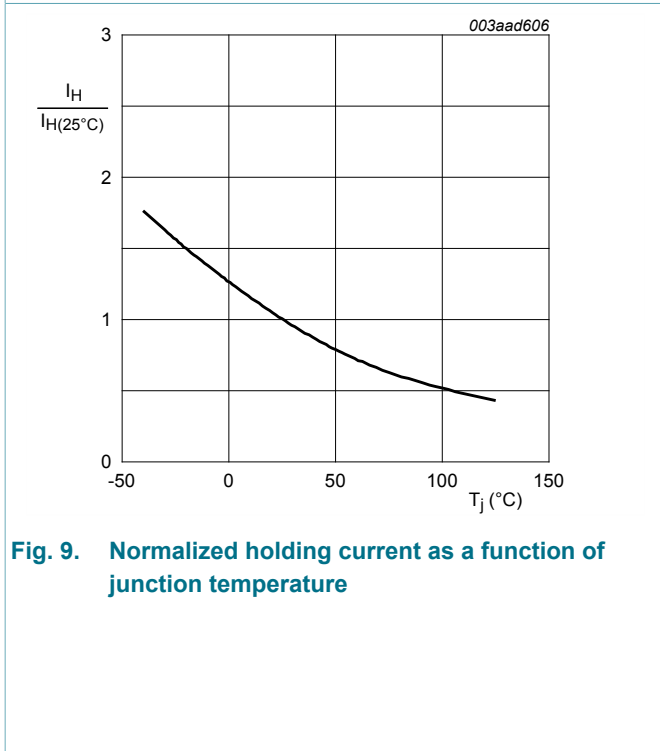
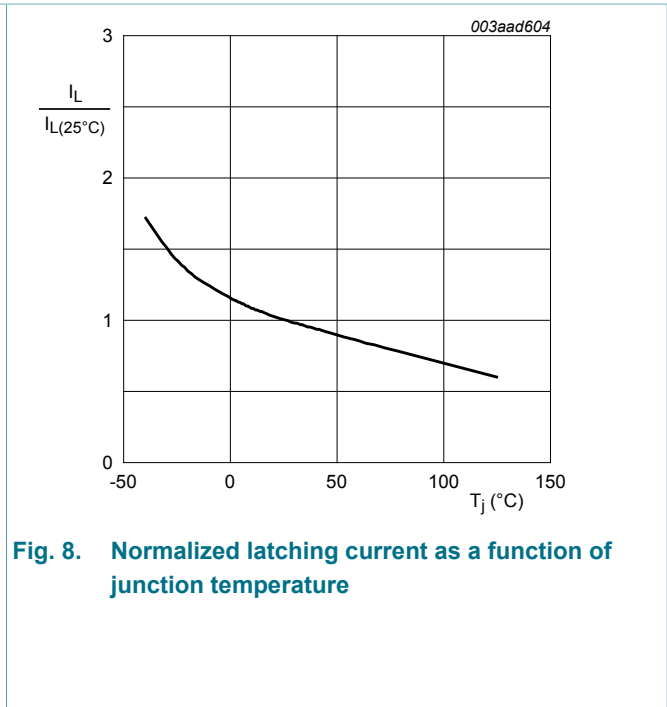
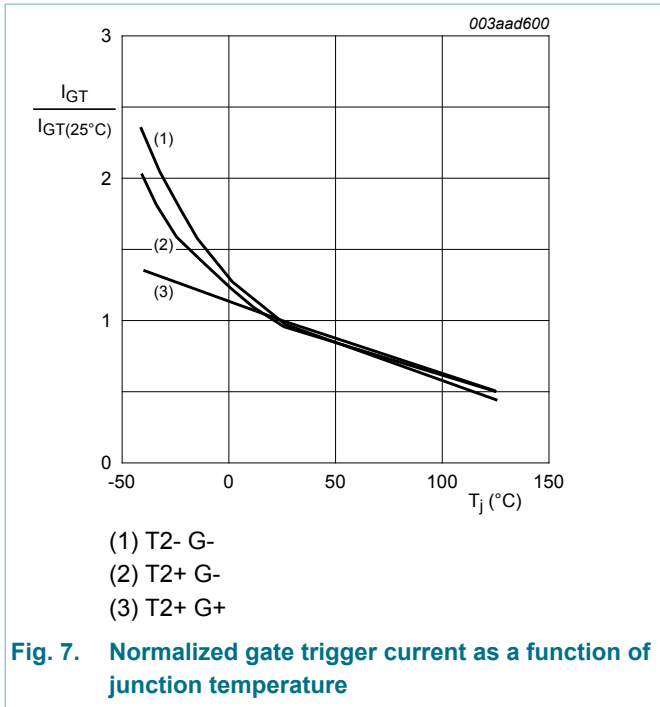


## 9. Characteristics

Table 6. Characteristics

| Symbol                         | Parameter                             | Conditions   | Min  | Typ | Max | Unit       |
|--------------------------------|---------------------------------------|--|------|-----|-----|------------|
| <b>Static characteristics</b>  |                                       |  |      |     |     |            |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>                                      | -    | -   | 5   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>                                      | -    | -   | 5   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>                                      | -    | -   | 5   | mA         |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>                                      | -    | -   | 6   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>                                      | -    | -   | 9   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>                                      | -    | -   | 6   | mA         |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>  | -    | -   | 6   | mA         |
| $V_T$                          | on-state voltage                      | $I_T = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>  | -    | 1.4 | 1.7 | V          |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ;<br><a href="#">Fig. 11</a>   | -    | 0.7 | 1   | V          |
|                                |                                       | $V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$ ;<br><a href="#">Fig. 11</a>   | 0.25 | 0.4 | -   | V          |
| $I_D$                          | off-state current                     | $V_D = 600\text{ V}$ ; $T_j = 125\text{ °C}$   | -    | 0.1 | 0.5 | mA         |
| <b>Dynamic characteristics</b> |                                       |  |      |     |     |            |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit                | 20   | -   | -   | V/ $\mu$ s |
| $dI_{com}/dt$                  | rate of change of commutating current | $V_D = 400\text{ V}$ ; $T_j = 125\text{ °C}$ ; $I_{T(RMS)} = 4\text{ A}$ ;<br>$dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit  | 1.1  | -   | -   | A/ms       |
|                                |                                       | $V_D = 400\text{ V}$ ; $T_j = 125\text{ °C}$ ; $I_{T(RMS)} = 4\text{ A}$ ;<br>$dV_{com}/dt = 0.1\text{ V}/\mu\text{s}$ ; gate open circuit | 4.5  | -   | -   | A/ms       |





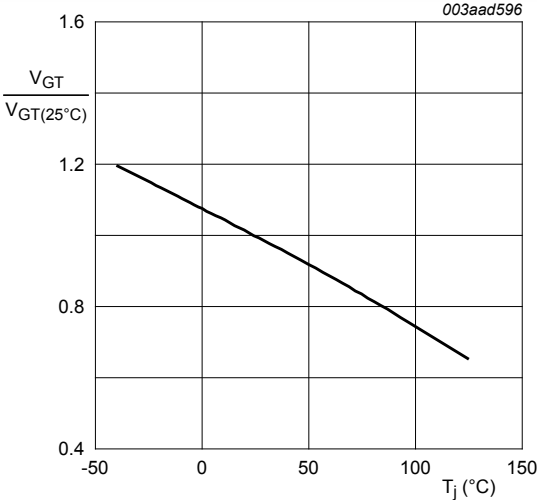
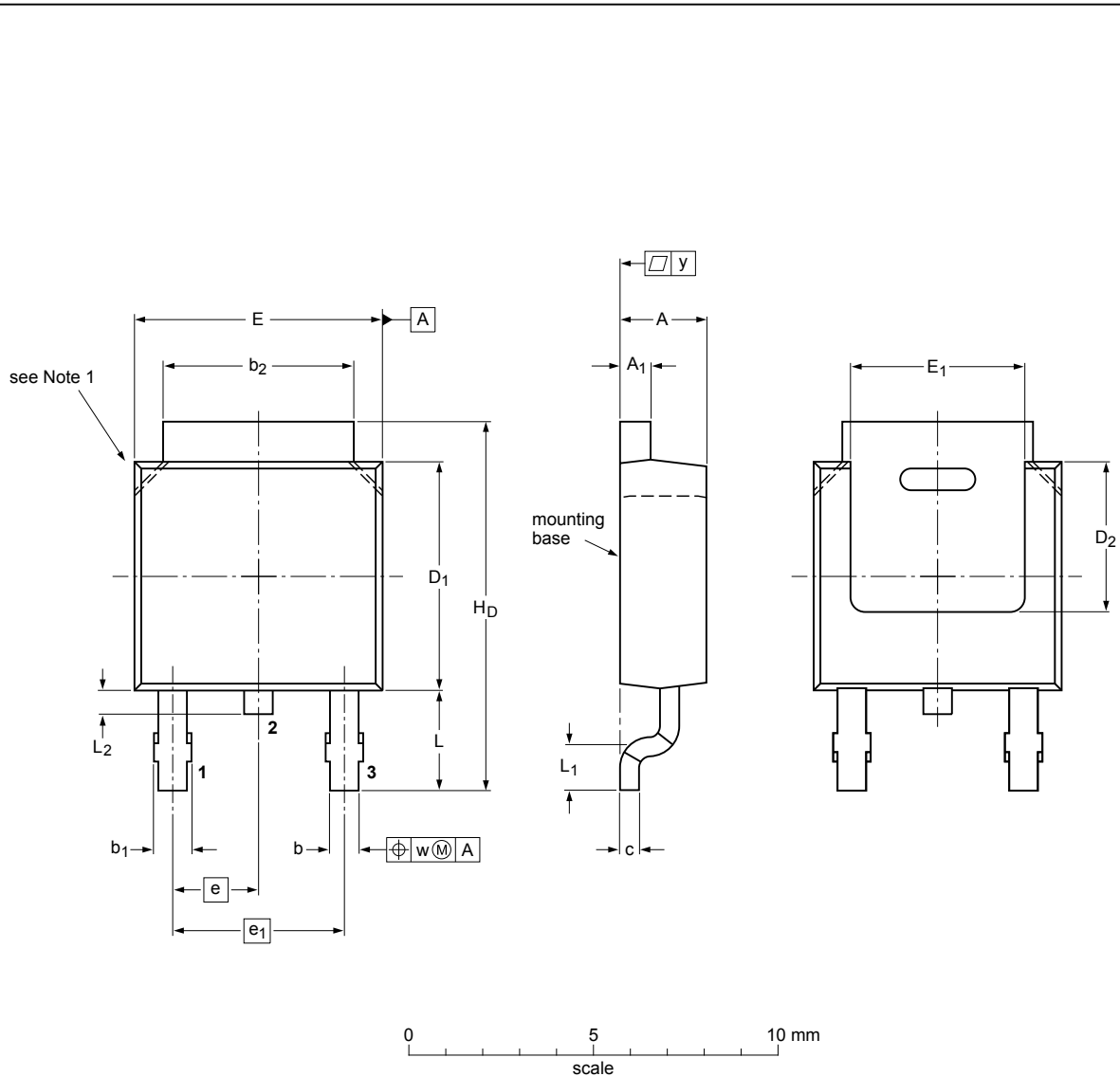


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

### 10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428



Dimensions (mm are the original dimensions)

| Unit | A    | A <sub>1</sub> | b    | b <sub>1</sub> | b <sub>2</sub> | c    | D <sub>1</sub> | D <sub>2</sub> | E    | E <sub>1</sub> | e     | e <sub>1</sub> | H <sub>D</sub> | L    | L <sub>1</sub> | L <sub>2</sub> | w   | y   |
|------|------|----------------|------|----------------|----------------|------|----------------|----------------|------|----------------|-------|----------------|----------------|------|----------------|----------------|-----|-----|
| max  | 2.38 | 0.93           | 0.89 | 1.1            | 5.46           | 0.56 | 6.22           |                | 6.73 |                |       |                | 10.4           | 2.95 |                | 0.9            |     | 0.2 |
| nom  |      |                |      |                |                |      |                |                |      |                | 2.285 | 4.57           |                |      |                |                | 0.2 |     |
| min  | 2.22 | 0.46           | 0.71 | 0.9            | 5.00           | 0.20 | 5.98           | 4.0            | 6.47 | 4.45           |       |                | 9.6            | 2.55 | 0.5            | 0.5            |     |     |

Note

1. Plastic body may have 45° chamfer.

sot428\_po

| Outline version | References |        |       | European projection | Issue date           |
|-----------------|------------|--------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC  | JEITA |                     |                      |
| SOT428          |            | TO-252 | SC-63 |                     | 06-03-16<br>14-06-10 |

Fig. 12. Package outline DPAK (SOT428)

11. Soldering

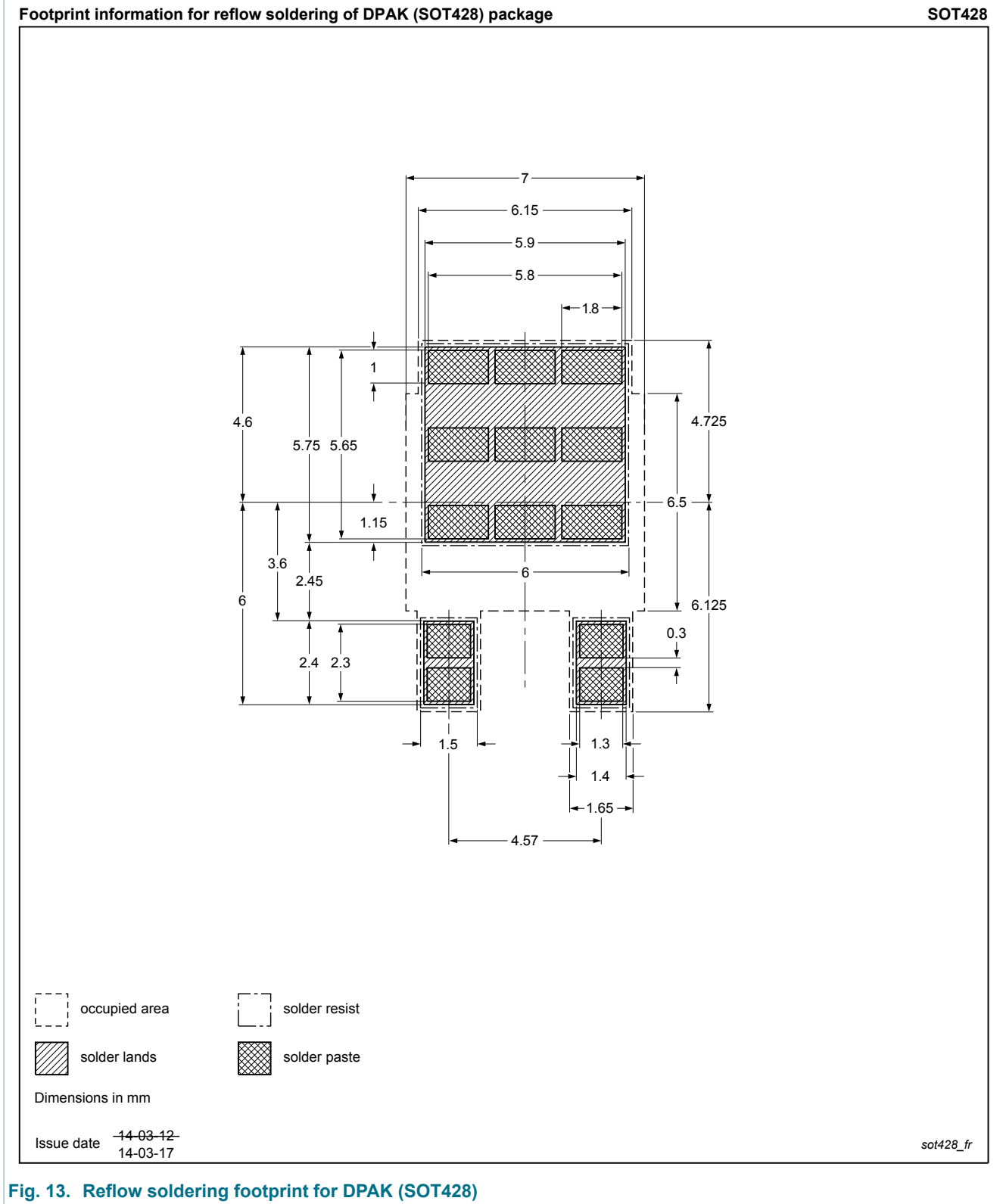


Fig. 13. Reflow soldering footprint for DPAK (SOT428)

## 12. Legal information

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| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
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