512MB – 64Mx64 DDR2 SDRAM UNBUFFERED

FEATURES

- 200-pin, Small-Outline DIMM (SO-DIMM), Raw Card "B"
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 MT/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V$
- $V_{CCSPD} = 1.7V$ to $3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Single Rank
- RoHS Compliant
- JEDEC Package option
  - 200 Pin (SO-DIMM)
  - PCB – 29.21mm (1.15")

DESCRIPTION

The W3HG64M64EEU is a 64Mx64 Double Data Rate 2 SDRAM memory module based on 512Mb DDR2 SDRAM components. The module consists of eight 64Mx8, in FBGA package mounted on a 200 pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-6400*	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	400MHz	333MHz	266MHz	200MHz
CL-t_{RCD}-t_{RP}	6-6-6	5-5-5	4-4-4	3-3-3

* Consult factory for availability

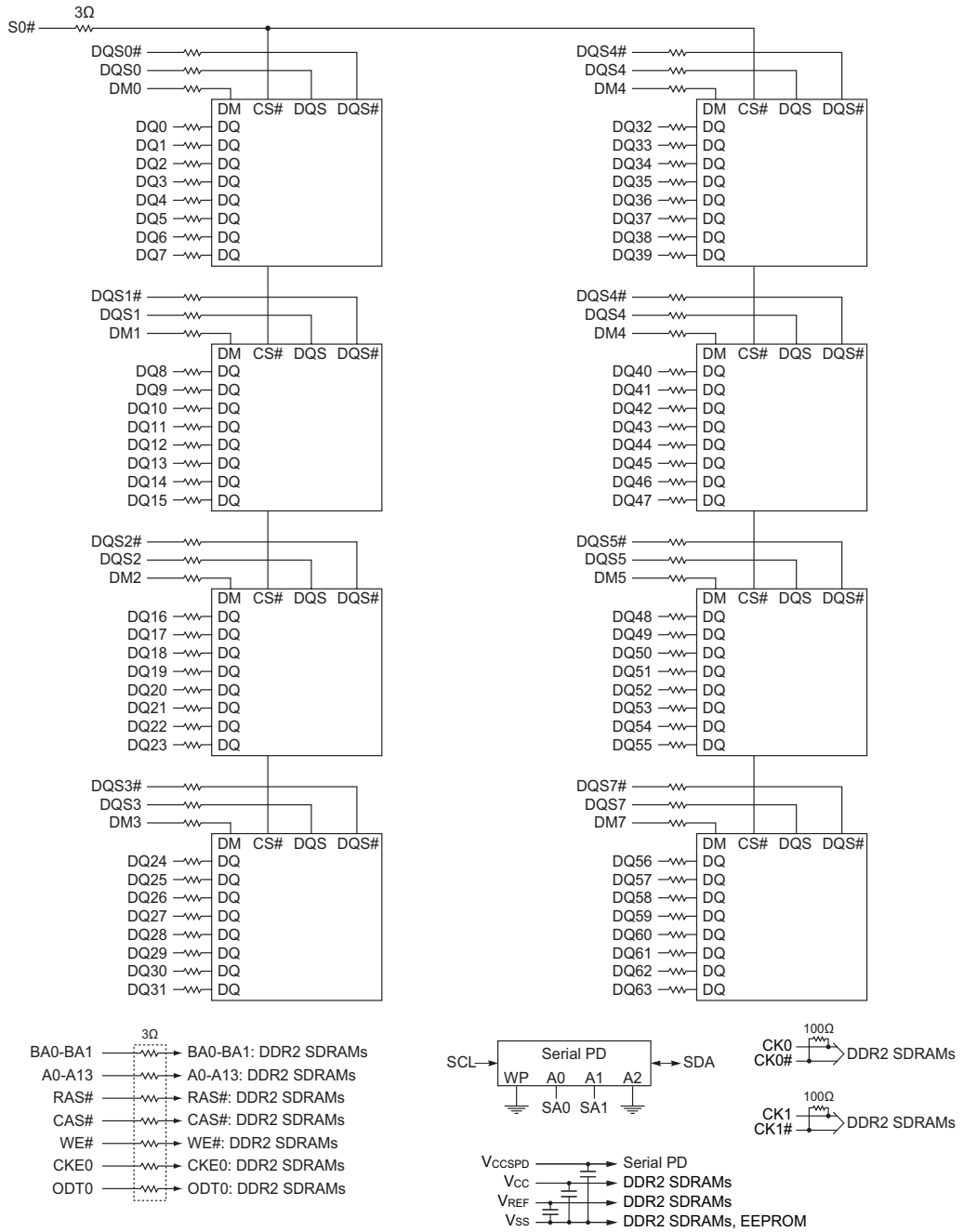
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	51	DQS2	101	A1	151	DQ42
2	V_{SS}	52	DM2	102	A0	152	DQ46
3	V_{SS}	53	V_{SS}	103	V_{CC}	153	DQ43
4	DQ4	54	V_{SS}	104	V_{CC}	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	V_{SS}
6	DQ5	56	DQ22	106	BA1	156	V_{SS}
7	DQ1	57	DQ19	107	BA0	157	DQ48
8	V_{SS}	58	DQ23	108	RAS#	158	DQ52
9	V_{SS}	59	V_{SS}	109	WE#	159	DQ49
10	DM0	60	V_{SS}	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	V_{CC}	161	V_{SS}
12	V_{SS}	62	DQ28	112	V_{CC}	162	V_{SS}
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	CK1
15	V_{SS}	65	V_{SS}	115	NC	165	V_{SS}
16	DQ7	66	V_{SS}	116	A13	166	CK1#
17	DQ2	67	DM3	117	V_{CC}	167	DQS6#
18	V_{SS}	68	DQS3#	118	V_{CC}	168	V_{SS}
19	DQ3	69	NC	119	NC	169	DQS6
20	DQ12	70	DQS3	120	NC	170	DM6
21	V_{SS}	71	V_{SS}	121	V_{SS}	171	V_{SS}
22	DQ13	72	V_{SS}	122	V_{SS}	172	V_{SS}
23	DQ8	73	DQ26	123	DQ32	173	DQ50
24	V_{SS}	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51
26	DM1	76	DQ31	126	DQ37	176	DQ55
27	V_{SS}	77	V_{SS}	127	V_{SS}	177	V_{SS}
28	V_{SS}	78	V_{SS}	128	V_{SS}	178	V_{SS}
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
30	CK0	80	NC	130	DM4	180	DQ60
31	DQS1	81	V_{CC}	131	DQS4	181	DQ57
32	CK0#	82	V_{CC}	132	V_{SS}	182	DQ61
33	V_{SS}	83	NC	133	V_{SS}	183	V_{SS}
34	V_{SS}	84	NC	134	DQ38	184	V_{SS}
35	DQ10	85	NC	135	DQ34	185	DM7
36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	V_{CC}	137	DQ35	187	V_{SS}
38	DQ15	88	V_{CC}	138	V_{SS}	188	DQS7
39	V_{SS}	89	A12	139	V_{SS}	189	DQ58
40	V_{SS}	90	A11	140	DQ44	190	V_{SS}
41	V_{SS}	91	A9	141	DQ40	191	DQ59
42	V_{SS}	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	V_{SS}
44	DQ20	94	A6	144	V_{SS}	194	DQ63
45	DQ17	95	V_{CC}	145	V_{SS}	195	SDA
46	DQ21	96	V_{CC}	146	DQS5#	196	V_{SS}
47	V_{SS}	97	A5	147	DM5	197	SCL
48	V_{SS}	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	V_{SS}	199	V_{CCSPD}
50	NC	100	A2	150	V_{SS}	200	SA1

PIN NAMES

SYMBOL	DESCRIPTION
A0-A12	Address input
ODT0	On-Die Termination
CK0, CK0#	Differential Clock Inputs
CK1, CK1#	Differential Clock inputs
CKE0	Clock Enable input
S0#	Chip select
RAS#, CAS#, WE#	Command Inputs
BA0, BA1	Bank Address Inputs
DM0-DM7	Input Data Mask
DQ0-DQ63	Data Input/Output
DQS0-DQS7 DQS0#-DQS7#	Data Strobe
SCL	Serial Clock for Presence Detect
SA0-SA1	Presence Detect Address Inputs
SDA	Serial Presence Detect Data
V_{CC}	Power Supply: +1.8V ±0.1V
V_{REF}	SSTL_18 reference voltage
V_{SS}	Ground
V_{CCSPD}	Serial EEPROM Positive Power Supply
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All resistor values are 22 ohm unless otherwise specified.

ABSOLUTE MAXIMUM DC CHARACTERISTICS

Symbol	Parameter		Min	Max	Units
V_{CC}	V_{CC} Supply Voltage Relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any Pin Relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	°C
T_{CASE}	DDR2 SDRAM Device Operating Temperature*		0	85	°C
T_{OPR}	Operating Temperature (Ambient)		0	65	°C
I_I	Input Leakage Current; Any input 0V ≤ V_{IN} ≤ V_{CC}; V_{REF} input 0V ≤ V_{IN} ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE	-40	40	µA
		CK, CK#	-20	20	
		DM	-5	5	
I_{OZ}	Output Leakage Current; 0V ≤ V_{OUT} ≤ $V_{CC}Q$; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} Leakage Current; V_{REF} = Valid V_{REF} level		-16	16	µA

* T_{CASE} specifies as the temperature at the top center of the memory devices.

RECOMMENDED DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
Supply Voltage	V_{CC}	1.7	1.9	V	-
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 40	V_{REF} + 40	mV	2

NOTE:

1. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

CAPACITANCE

T_A = 25°C, f = 1MHz, V = 1.8V

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	TBD	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	TBD	pF
Input Capacitance (CKE0)	C_{IN3}	TBD	pF
Input Capacitance (CK0, CK0#)	C_{IN4}	TBD	pF
Input Capacitance (S0#)	C_{IN5}	TBD	pF
Input Capacitance (DQS0#-DQS17#)	C_{IN6}	TBD	pF
Input Capacitance (BA0-BA1)	C_{IN7}	TBD	pF
Data input/output Capacitance (DQ0-DQ63)	C_{OUT}	TBD	pF

DDR2 I_{DD} SPECIFICATIONS AND CONDITIONS

DDR2 SDRAM components only

Parameter	Active Rank State	Condition		806	665	553	403	Units
Operating one device bank active-precharge current;	I_{DD0}	$t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MIN (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	720	640	640	mA
Operating one device bank active-read-precharge current;	I_{DD1}	I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MIN (I_{DD}), $t_{RCD} = t_{RCD}$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DD4W}.		TBD	840	760	720	mA
Precharge power-down current;	I_{DD2P}	All device banks idle; $t_{CK} = t_{CK}$ (I_{DD}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		TBD	40	40	40	mA
Precharge quiet standby current;	I_{DD2Q}	All device banks idle; $t_{CK} = t_{CK}$ (I_{DD}); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		TBD	400	320	280	mA
Precharge standby current;	I_{DD2N}	All device banks idle; $t_{CK} = t_{CK}$ (I_{DD}); CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	440	360	320	mA
Active power-down current;	I_{DD3P}	All device banks open; $t_{CK} = t_{CK}$ (I_{DD}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	TBD	280	240	200	mA
			Slow PDN Exit MR[12] = 1	TBD	80	80	80	mA
Active standby current;	I_{DD3N}	All device banks open; $t_{CK} = t_{CK}$(I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$(I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	520	440	360	mA
Operating burst write current;	I_{DD4W}	All device banks open, Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	1,240	1,040	880	mA
Operating burst read current;	I_{DD4R}	All device banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	1,400	1,160	920	mA
Burst refresh current;	I_{DD5}	$t_{CK} = t_{CK}$ (I_{DD}); Refresh command at every t_{RFC} (I_{DD}) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	1,680	1,600	1, 520	mA
Self refresh current;	I_{DD6}	CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		TBD	40	40	40	mA
Operating device bank interleave read current;	I_{DD7}	All device banks interleaving reads, I_{OUT}= 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD})-1 x t_{CK} (I_{DD}); $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$(I_{DD}), $t_{RRD} = t_{RRD}$(I_{DD}), $t_{RCD} = t_{RCD}$(I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See I_{DD7} Conditions for detail.		TBD	2,240	2,080	1,840	mA

Note:

- IDD specification is based on MICRON components. Other DRAM manufactures specification may be different.

AC OPERATING CONDITIONS

≤T_{CASE}≤+85°C; V_{CC} = +1.8V ±0.1V

	AC Characteristics			806		665		534		403			
	Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Clock	Clock cycle time	CL = 6	t_{CK} (6)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		CL = 5	t_{CK} (5)	TBD	TBD	3,000	8,000	-	-	-	-	ps	16,25
		CL = 4	t_{CK} (4)	TBD	TBD	3, 750	8,000	3,750	8,000	5,000	8,000	ps	16,25
		CL = 3	t_{CK} (3)	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps	16,25
	CK low-level width		t_{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	19
	Half clock period		t_{HP}	TBD	TBD	MIN (t_{CH},t_{CL})		MIN (t_{CH},t_{CL})		MIN (t_{CH},t_{CL})		ps	20
	Clock jitter		t_{JIT}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	18
Data	DQ output access time from CK/CK#		t_{AC}	TBD	TBD	-450	-450	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#		t_{HZ}	TBD	TBD		t_{AC} (MAX)		t_{AC} (MAX)		t_{AC} (MAX)	ps	8, 9
	Data-out low-impedance window from CK/CK#		t_{LZ}	TBD	TBD	t_{AC} (MIN)	t_{AC} (MAX)	t_{AC} (MIN)	t_{AC} (MAX)	t_{AC} (MIN)	t_{AC} (MAX)	ps	8, 10
	DQ and DM input setup time relative to DQS		t_{DS_a}	TBD	TBD	300		350		400		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		t_{DH_a}	TBD	TBD	300		350		400		ps	7, 15, 22
	DQ and DM input setup time relative to DQS		t_{DS_b}	TBD	TBD	100		100		150		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		t_{DH_b}	TBD	TBD	175		225		275		ps	7, 15, 22
	DQ and DM input pulse width (for each input)		t_{DIPW}	TBD	TBD	0.35		0.35		0.35		t_{CK}	
	Data hold skew factor		t_{QHS}	TBD	TBD		340		400		450	ps	
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	TBD	TBD	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ps	15, 17
	Data valid output window (DVW)		t_{DVW}	TBD	TBD	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns	15, 17

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specifications may be different.

AC OPERATING CONDITIONS (continued)

≤T_{CASE}≤+85°C; V_{CC} = +1.8V ±0.1V

	AC Characteristics		806		665		534		403			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Data Strobe	DQS input high pulse width	t_{DQSH}	TBD	TBD	0.35		0.35		0.35		t_{CK}	
	DQS input low pulse width	t_{DQSL}	TBD	TBD	0.35		0.35		0.35		t_{CK}	
	DQS output access time from CK/CK#	t_{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising – setup time	t_{DSS}	TBD	TBD	0.2		0.2		0.2		t_{CK}	
	DQS falling edge from CK rising – hold time	t_{DSH}	TBD	TBD	0.2		0.2		0.2		t_{CK}	
	DQS–DQ skew, DQS to last DQ valid, per group, per access	t_{DQSQ}	TBD	TBD		240		300		350	ps	15, 17
	DQS read preamble	t_{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	36
	DQS read postamble	t_{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	36
	DQS write preamble setup time	t_{WPRES}	TBD	TBD	0		0		0		ps	12, 13, 37
	DQS write preamble	t_{WPRE}	TBD	TBD	0.35		0.25		0.25		t_{CK}	
	DQS write postamble	t_{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	11
	Write command to first DQS latching transition	t_{DQSS}	TBD	TBD	WL - 0.25	WL+ 0.25	WL - 0.25	WL+ 0.25	WL - 0.25	WL+ 0.25	t_{CK}	
Command and Address	Address and control input pulse width for each input	t_{IPW}	TBD	TBD	0.6		0.6		0.6		t_{CK}	
	Address and control input setup time	t_{IS_a}	TBD	TBD	400		500		600		ps	6, 22
	Address and control input hold time	t_{IH_a}	TBD	TBD	400		500		600		ps	6, 22
	Address and control input setup time	t_{IS_b}	TBD	TBD	200		250		350		ps	6, 22
	Address and control input hold time	t_{IH_b}	TBD	TBD	275		375		475			6, 22
	CAS# to CAS# command delay	t_{CCD}	TBD	TBD	2		2		2		t_{CK}	
	ACTIVE to ACTIVE (same bank) command	t_{RC}	TBD	TBD	55		55		55		ns	34
	ACTIVE bank a to ACTIVE bank command	t_{RRD}	TBD	TBD	7.5		7.5		7.5		ns	28
	ACTIVE to READ or WRITE delay	t_{RCD}	TBD	TBD	15		15		15		ns	
	Four Bank Activate period	t_{FAW}	TBD	TBD	37.5		37.5		37.5		ns	31
	ACTIVE to PRECHARGE command	t_{RAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns	21, 34
	Internal READ to precharge command delay	t_{RTP}	TBD	TBD	7.5		7.5		7.5		ns	24, 28
	Write recovery time	t_{WR}	TBD	TBD	15		15		15		ns	28
	Auto precharge write recovery + precharge time	t_{DAL}	TBD	TBD	t_{WR} + t_{RP}		t_{WR} + t_{RP}		t_{WR} + t_{RP}		ns	23
	Internal WRITE to READ command delay	t_{WTR}	TBD	TBD	10		7.5		10		ns	28
	PRECHARGE command period	t_{RP}	TBD	TBD	15		15		15		ns	32
	PRECHARGE ALL command period	t_{RPA}	TBD	TBD	t_{RP} + t_{RP}		t_{RP} + t_{RP}		t_{RP} + t_{RP}		ns	32
	LOAD MODE command cycle time	t_{MRD}	TBD	TBD	2		2		2		t_{CK}	
	CKE low to CK,CK# uncertainty	t_{DELAY}	TBD	TBD	t_{IS} + t_{CK} + t_{IH}		t_{IS} + t_{CK} + t_{IH}		t_{IS} + t_{CK} + t_{IH}		ns	29

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specifications may be different.

AC OPERATING CONDITIONS (continued)

≤T_{CASE}≤+85°C; V_{CC} = +1.8V ±0.1V

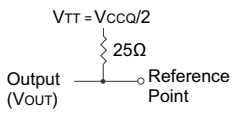
	AC Characteristics		806		665		534		403			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Self Refresh	REFRESH to Active or Refresh to Refresh command interval	$t_{RFC\ (512MB)}$	TBD	TBD	105	70,000	150	70,000	105	70,000		14
	Average periodic refresh interval	t_{XSNR}	TBD	TBD		7.8		7.8		7.8	µs	14
	Exit self refresh to non-READ command	t_{XSNR}	TBD	TBD	t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		ns	
	Exit self refresh to READ command	t_{XSRD}	TBD	TBD	200		200		200		t_{CK}	
	Exit self refresh timing reference	t_{ISXR}	TBD	TBD	t_{IS}		t_{IS}		t_{IS}		ps	6, 30
ODT	ODT turn-on delay	t_{AOND}	TBD	TBD	2	2	2	2	2		t_{CK}	
	ODT turn-on	t_{AOND}			$t_{AC\ (MIN)}$	$t_{AC\ (MAX}$ + 700)	$t_{AC\ (MIN)}$	$t_{AC\ (MAX}$ + 1,000)	$t_{AC\ (MIN)}$	$t_{AC\ (MAX}$ + 1,000)	ps	26
	ODT turn-off delay	t_{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}	
	ODT turn-off	t_{AOF}	TBD	TBD	$t_{AC\ (MIN)}$	$t_{AC\ (MAX}$ + 600)	$t_{AC\ (MIN)}$	$t_{AC\ (MAX}$ + 600)	$t_{AC\ (MIN)}$	$t_{AC\ (MAX}$ + 600)	ps	27
	ODT turn-on (power-down mode)	t_{AONPD}	TBD	TBD	$t_{AC\ (MIN)}$ + 2,000	t_{AC} (MAX) + 1,000	$t_{AC\ (MIN)}$ + 2,000	t_{AC} (MAX) + 1,000	$t_{AC\ (MIN)}$ + 2,000	t_{AC} (MAX) + 1,000	ps	
	ODT turn-off (power-down mode)	t_{AOFPD}	TBD	TBD	$t_{AC\ (MIN)}$ + 2,000	t_{AC} (MAX) + 1,000	$t_{AC\ (MIN)}$ + 2,000	t_{AC} (MAX) + 1,000	$t_{AC\ (MIN)}$ + 2,000	t_{AC} (MAX) + 1,000	ps	
	ODT to power-down entry latency	t_{ANPD}	TBD	TBD	3		3		3		t_{CK}	
	ODT power-down exit latency	t_{AXPD}	TBD	TBD	8		8		8		t_{CK}	
Power Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	TBD	TBD	2		2		2		t_{CK}	
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	TBD	TBD	7 - AL		6 - AL		6 - AL			
	Exit precharge power-down to any non-READ command.	t_{XP}	TBD	TBD	2		2		2		t_{CK}	
	CKE minimum high/low time	t_{CKE}	TBD	TBD	3		3		3		t_{CK}	35

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specifications may be different.

Notes:

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between VIL (AC) and VIH (AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using tISb and the Setup and Hold Time Derating Values table. tIS timing ($^{t}IS_b$) is referenced from VIH(AC) for a rising signal and VIL(DC) for a falling signal. The timing table also lists the $^{t}IS_b$ and $^{t}IH_b$ values for a 1.0V/ns slew rate; these are the "base" values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points. tDS timing ($^{t}DS_b$) is referenced from VIH (AC) for a rising signal and VIL (AC) for a falling signal. tiH timing ($^{t}IH_b$) is referenced from VIH(DC) for a rising signal and VIL(DC) for a falling signal. The timing table lists the t_{DSb} and $^{t}DH_b$ values for a 1.0V/ns slew rate. If the DQS/DQS# differential strobe feature is not enabled, timing is no longer referenced to the crosspoint of DQS/DQS#. Data timing is now referenced to VREF, provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to VIH(AC) for a rising DQS and VIL(DC) for a falling DQS.
8. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
9. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over $^{t}DQSCK$ (MAX) + $^{t}RPST$ (MAX) condition.
10. ^{t}LZ (MIN) will prevail over a $^{t}DQSCK$ (MIN) + $^{t}RPRE$ (MAX) condition
11. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above VIHDC(min) then it must not transition low (below VIH(DC) prior to $^{t}DQSH$(min).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. How-ever, a REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms.
15. Each byte lane has a corresponding DQS.
16. CK and CK# input slew rate must be ≥ 1V/ns (≥ 2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications - ^{t}HP. ($^{t}CK/2$), $^{t}DQSQ$, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. ^{t}JIT specification is currently TBD.
19. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. This value can be greater than the minimum specification limits for ^{t}CL and ^{t}CH). For example, ^{t}CL and ^{t}CH are = 50 percent of the period, less the half period jitter [$^{t}JIT(HP)$] of the clock source, and less the half period jitter due to cross talk [$^{t}JIT(cross\ talk)$] into the clock traces.
20. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs.
21. READs and WRITEs with auto precharge are allowed to be issued before ^{t}RAS (MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM devices.
22. VIL/VIH DDR2 overshoot/undershoot. REFER to the 512Mb SDRAM data sheet for more detail.
23. ^{t}DAL = (nWR) + ($^{t}RP/^{t}CK$): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period; AC Operation Condition Notes: nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. Example: For -533 Mb/s at tCK = 3.75 ns with ^{t}WR programmed to four clocks. ^{t}DAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4) clocks = 8 clocks.
24. The minimum READ to internal PRECHARGE time. This parameter is only applicable when $^{t}RTP/(2*^{t}CK) > 1$. If $^{t}RTP/(2*^{t}CK) \leq 1$, then equation AL + BL/2 applies. Notwithstanding, ^{t}RAS (MIN) has to be satisfied as well. The DDR2 SDRAM device will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
25. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, and system reset condition.
26. ODT turn-on time ^{t}AON (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from $^{t}AOND$.
27. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in high impedance. Both are measured from $^{t}AOFD$.
28. This parameter has a two clock minimum requirement at any ^{t}CK.
29. $^{t}DELAY$ is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.
30. $^{t}ISXR$ is equal to ^{t}IS and is used for CKE setup time during self refresh exit.
31. No more than 4 bank ACTIVE commands may be issued in a given ^{t}FAW(min) period. ^{t}RRD(min) restriction still applies. The ^{t}FAW(min) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
32. ^{t}RPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA(MIN) applies to all 8-bank DDR2 devices.
33. Value is minimum pulse width, not the number of clock registrations.
34. Applicable to Read cycles only. Write cycles generally require additional time due to Write recovery time (^{t}WR) during auto precharge.
35. ^{t}CKE (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 x ^{t}CK + ^{t}IH.
36. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving ($^{t}RPST$) or beginning to drive ($^{t}RPRE$).
37. When DQS is used single-ended, the minimum limit is reduced by 100ps.

ORDERING INFORMATION FOR D4

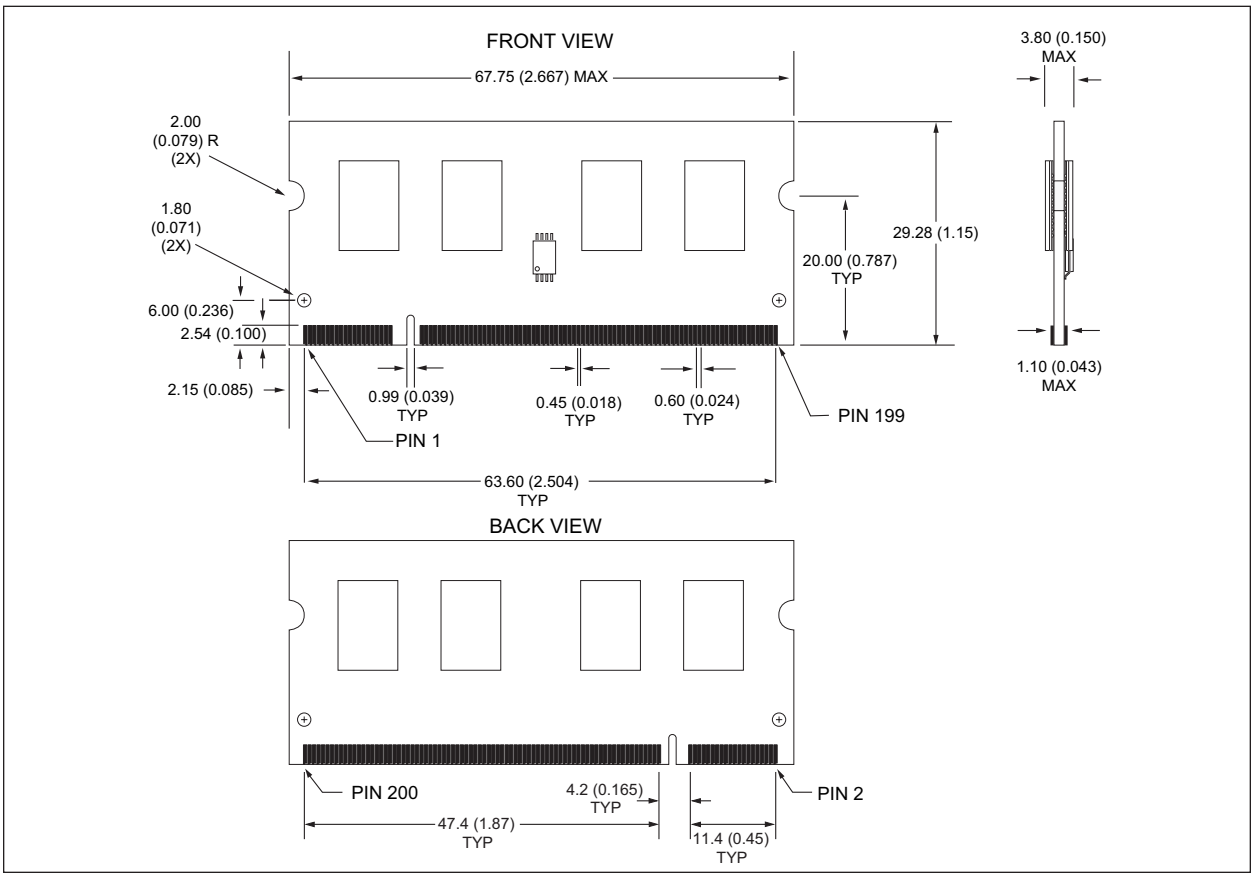
Part Number	Clock/Data Rate Frequency	CAS Latency	t_{RCD}	t_{RP}	Height**
W3HG64M64EEU806D4xG*	400MHz/800Mb/s	6	6	6	29.21mm (1.15")
W3HG64M64EEU665D4xG*	333MHz/667Mb/s	5	5	5	29.21mm (1.15")
W3HG64M64EEU534D4xG	266MHz/533Mb/s	4	4	4	29.21mm (1.15")
W3HG64M64EEU403D4xG	200MHz/400Mb/s	3	3	3	29.21mm (1.15")

* Consult Factory for availability

NOTES:

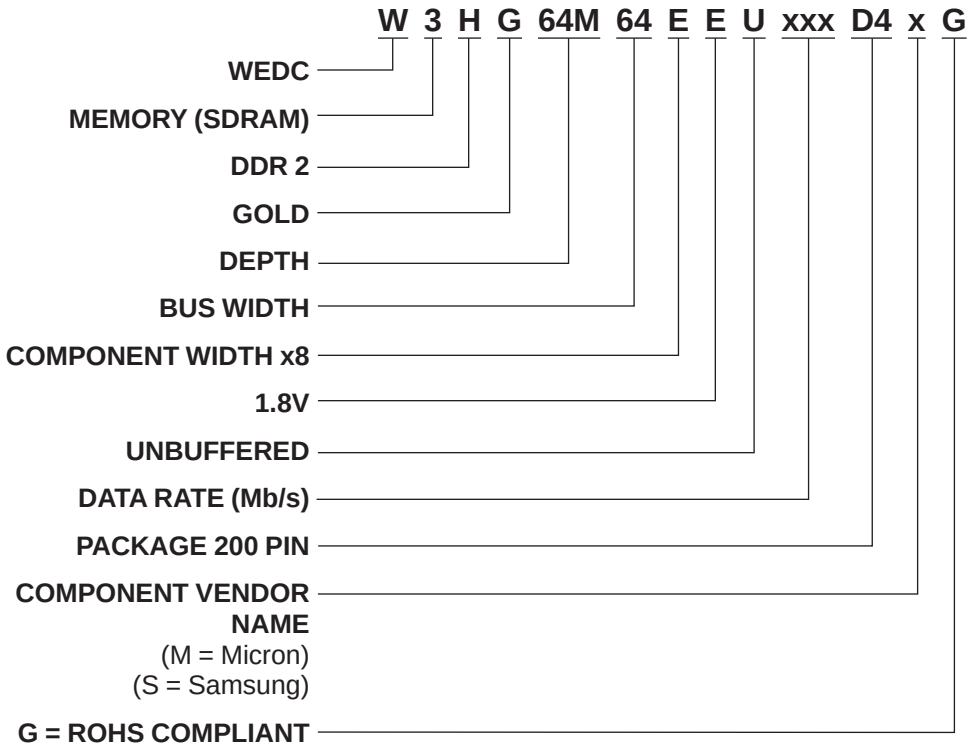
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

512Mb – 64Mx64 DDR2 SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	10-05	Advanced