

# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB

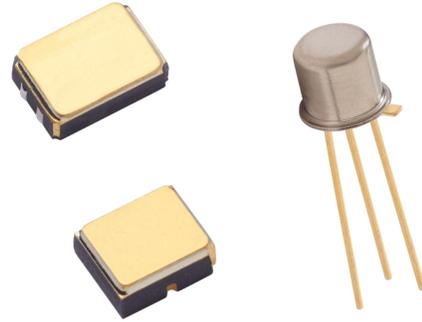


## Radiation Hardened NPN Silicon Switching Transistors

Rev. V3

### Features

- Available in JAN, JANTX, JANTXV, JANS and JANSR per MIL-PRF-19500/255
- Radiation Tolerant Levels M, D, P, L and R
- TO-18 (TO-206AA), Surface mount UA & UB Packages



### Applications

- Switching and Linear Applications
- DC and VHF Amplifier Applications

### Electrical Specifications ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Minimum	Maximum
Collector - Emitter Breakdown	$I_C = 10 \text{ mA dc}$	$V_{(BR)CEO}$	V dc	50	—
Collector - Base Cutoff Current	$V_{CB} = 75 \text{ V dc}$ $V_{CB} = 60 \text{ V dc}$	$I_{CBO1}$ $I_{CBO2}$	$\mu\text{A dc}$ nA dc	—	10 10
Emitter - Base Cutoff Current	$V_{EB} = 6.0 \text{ V dc}$ $V_{EB} = 4.0 \text{ V dc}$	$I_{EBO1}$ $I_{EBO2}$	$\mu\text{A dc}$ nA dc	—	10 10
Collector - Emitter Cutoff Current	$V_{CE} = 50 \text{ V dc}$	$I_{CES}$	nA dc	—	50
Forward Current Transfer Ratio	<p>2N2221A, L, UA, UB</p> <p><math>I_C = 0.1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 1.0 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 10 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 150 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 500 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math></p> <p>2N2222A, L, UA, UB</p> <p><math>I_C = 0.1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 1.0 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 10 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 150 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math>  <math>I_C = 500 \text{ mA dc}, V_{CE} = 10 \text{ V dc}</math></p>	$h_{FE}$		30 35 40 40 20	— 150 — 120 —
Collector - Base Cutoff Current	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc}$ $I_C = 500 \text{ mA dc}; I_B = 50 \text{ mA dc}$	$V_{CE(sat)1}$ $V_{CE(sat)2}$	V dc	—	0.3 1.0
Base - Emitter Saturation Voltage	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc}$ $I_C = 500 \text{ mA dc}; I_B = 50 \text{ mA dc}$	$V_{BE(sat)1}$ $V_{BE(sat)2}$	V dc	0.6 —	1.2 2.0
Collector - Base Cutoff Current	$T_A = +150^\circ\text{C}$ $V_{CB} = 60 \text{ V dc}$	$I_{CBO3}$	$\mu\text{A dc}$		10
Forward Current Transfer Ratio	$T_A = -55^\circ\text{C}$ $V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc}$ 2N2221A (all types) 2N2222A (all types)	$h_{FE6}$		15 35	

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### Electrical Specifications ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Minimum	Maximum
<b>Dynamic Characteristics:</b>					
Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE} = 10\text{ V dc}; I_C = 1\text{ mA dc}; f = 1\text{ kHz}$ 2N2221A, L, UA, UB 2N2222A, L, UA, UB	$h_{fe}$		30 50	—
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE} = 20\text{ V dc}; I_C = 20\text{ mA dc}; f = 100\text{ MHz}$	$ h_{fe} $		2.5	—
Output Capacitance	$V_{CB} = 10\text{ V dc}; I_E = 0; 100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{obo}$	pF	—	8
Input Capacitance (Output Open-Circuited)	$V_{EB} = 0.5\text{ V dc}; I_C = 0; 100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{ibo}$	pF	—	25
<b>Switching Characteristics:</b>					
Turn-On Time	(See figure 17 of MIL-PRF-19500/255)	$t_{on}$	ns	—	35
Turn-Off Time	(See Figure 18 of MIL-PRF-19500/255)	$t_{off}$	ns	—	300

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### Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	$V_{CEO}$	50 V dc
Collector - Base Voltage	$V_{CBO}$	75 V dc
Emitter - Base Voltage	$V_{EBO}$	6 V dc
Collector Current	$I_C$	800 mA dc
Total Power Dissipation <sup>(1)(2)</sup> $T_A = +25^\circ\text{C}$ 2N2221A, AL 2N2222A, AL	$P_T$	0.50 W
Total Power Dissipation <sup>(1)(2)</sup> $T_C = +25^\circ\text{C}$ 2N2221A, AL 2N2222A, AL	$P_T$	1 W
Total Power Dissipation <sup>(1)(2)</sup> $T_A = +25^\circ\text{C}$ 2N2221AUA, UB 2N2222AUA, UB	$P_T$	0.50 W <sup>(4)</sup>
Total Power Dissipation <sup>(1)(2)</sup> $T_{SP(IS)} = +25^\circ\text{C}$ 2N2221AUA, UB 2N2222AUA, UB	$P_T$	1 W
Total Power Dissipation <sup>(1)(2)</sup> $T_{SP(AM)} = +25^\circ\text{C}$ 2N2221AUA, 2N2222AUA	$P_T$	1.5 W
Operating & Storage Temperature Range	$T_J, T_{STG}$	$-65^\circ\text{C}$ to $+200^\circ\text{C}$

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### Thermal Characteristics ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Ambient <sup>(2) (3)</sup> 2N2221A, AL 2N2221AUA, 2N2222AUA 2N2221AUB, 2N2222AUB	$R_{\theta JA}$	325°C/W 325°C/W <sup>(4)</sup> 325°C/W <sup>(4)</sup>
Thermal Resistance, Junction to Case <sup>(2) (3)</sup> 2N2221A, AL 2N2222A, AL	$R_{\theta JC}$	150°C/W 150°C/W
Thermal Resistance, Junction to Solder Pad <sup>(2) (3)</sup> 2N2221AUA, 2N2222AUA 2N2221AUB, 2N2222AUB	$R_{\theta JSP(IS)}$	110°C/W 90°C/W
Thermal Resistance, Junction to Solder Pad <sup>(2) (3)</sup> 2N2221AUA, 2N2222AUA	$R_{\theta JSP(AM)}$	40°C/W

(1) For derating, see figure 7, figure 8, figure 9, figure 10, and figure 11 of MIL-PRF-19500/255

(2) See paragraph 3.3 of MIL-PRF-19500/255 for abbreviations

(3) For thermal impedance curves, see figure 12, figure 13, figure 14, figure 15 and figure 16 of MIL-PRF-19500/255.

(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figure 8 and figure 13 for the UA and UB packages and use  $R_{\theta JA}$ .

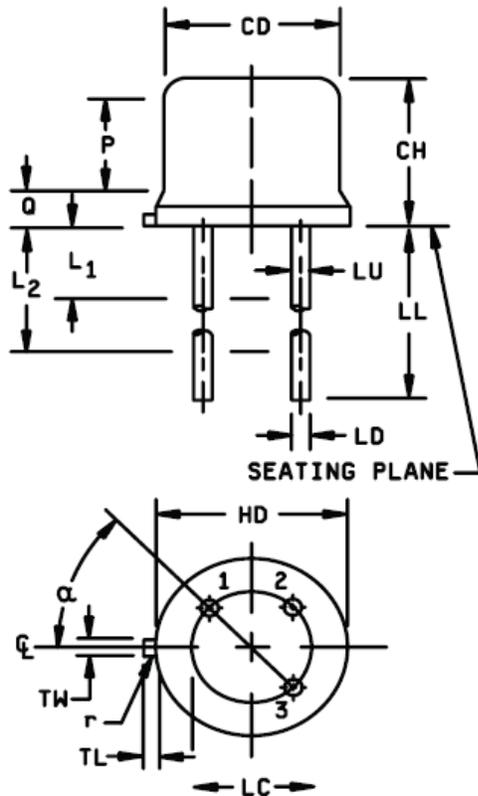
# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB



## Radiation Hardened NPN Silicon Switching Transistors

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### Outline Drawing (TO-18):



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
CD	0.178	0.195	4.52	1.95	—
CH	0.170	0.210	4.32	5.33	—
HD	0.209	0.230	5.31	5.84	—
LC	0.100 Typ.		2.54 Typ		6
LD	0.016	0.021	0.41	0.53	7, 8
LL	0.500	0.750	12.70	19.05	7, 8, 13
LU	0.016	0.019	0.41	0.48	7, 8
L1	—	0.050	—	1.27	7, 8
L2	0.250	—	6.35	—	7, 8
P	0.100	—	2.54	—	—
Q	—	0.030	—	0.76	5
TL	0.028	0.048	0.71	1.22	3, 4
TW	0.036	0.046	0.91	1.17	3
r	—	0.010	—	0.25	10
a	45°Typ.				6
1, 2, 9, 11, 12, 13					

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within 0.007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi$ x symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

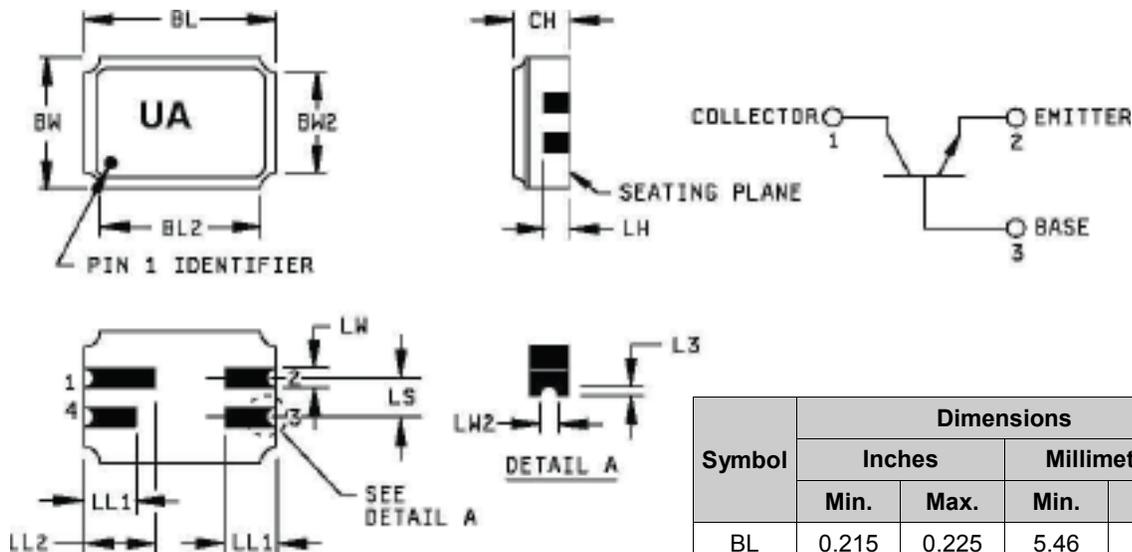
# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB



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### Outline Drawing (UA Surface Mount):



Pin #	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
BL	0.215	0.225	5.46	5.71	—
BL2	—	0.225	—	5.71	—
BW	0.145	0.155	3.68	3.93	—
BW2	0.155		3.93		—
CH	0.061	0.075	1.55	1.90	3
L3	0.003	0.007	0.08	0.18	5
LH	0.029	0.042	0.74	1.07	—
LL1	0.032	0.048	0.81	1.22	—
LL2	0.072	0.088	1.83	2.23	—
LS	0.045	0.055	1.14	1.39	—
LW	0.022	0.028	0.56	0.71	—
LW2	0.006	0.022	0.15	0.56	5

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

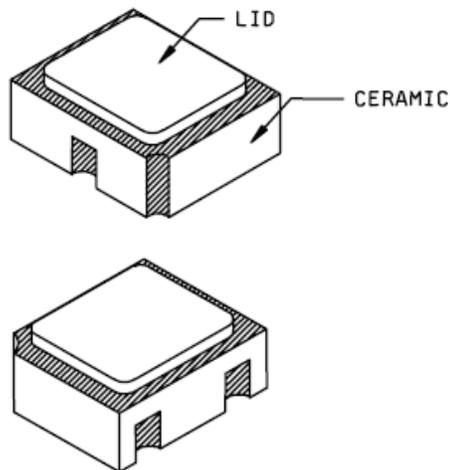
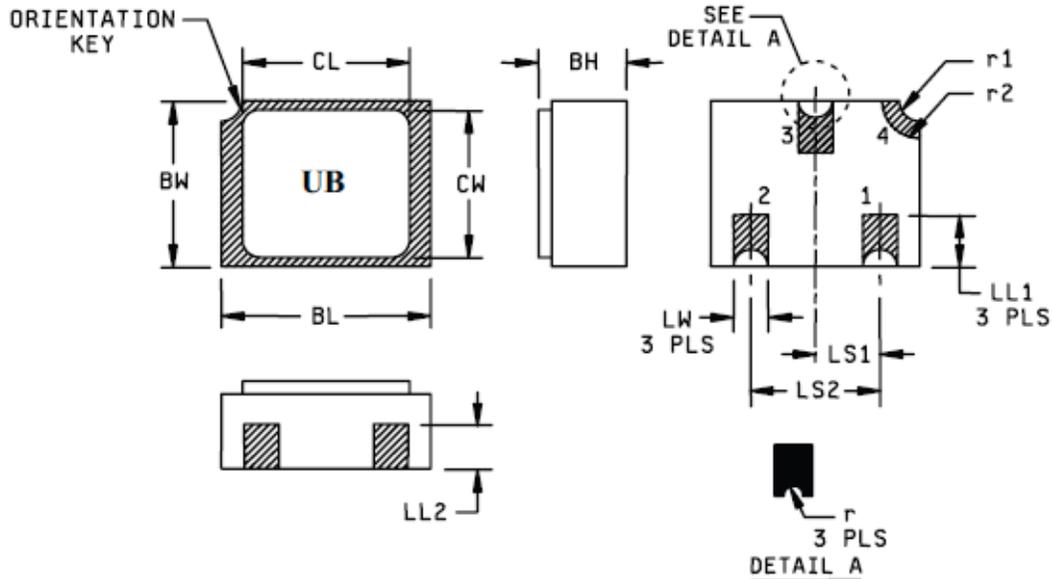
# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB



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### Outline Drawing (UB Surface Mount):



Symbol	Dimensions			
	Inches		Millimeters	
	Min.	Max.	Min.	Max.
BH	0.046	0.056	1.17	1.42
BL	0.115	0.128	2.92	3.25
BW	0.085	0.108	2.16	2.74
CL	—	0.128		3.25
CW		0.108		2.74
LL1	0.022	0.038	0.56	0.96
LL2	0.017	0.035	0.43	0.89
LS1	0.036	0.040	0.91	1.02
LS2	0.071	0.079	1.81	2.01
LW	0.016	0.024	0.41	0.61
r	—	0.008	—	0.203
r1	—	0.012	—	0.305
r2	—	0.022	—	0.559

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metalized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

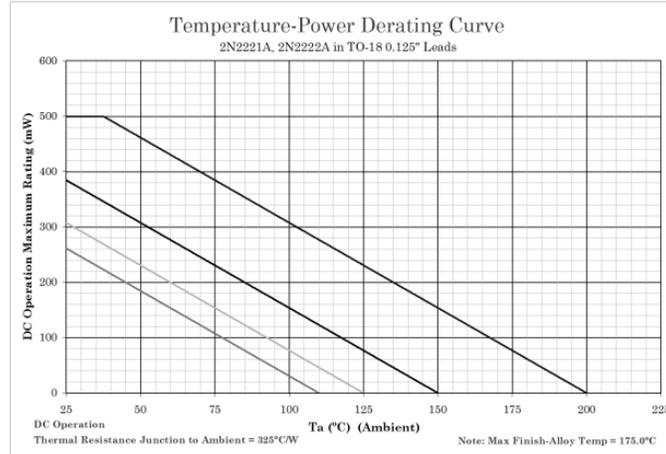
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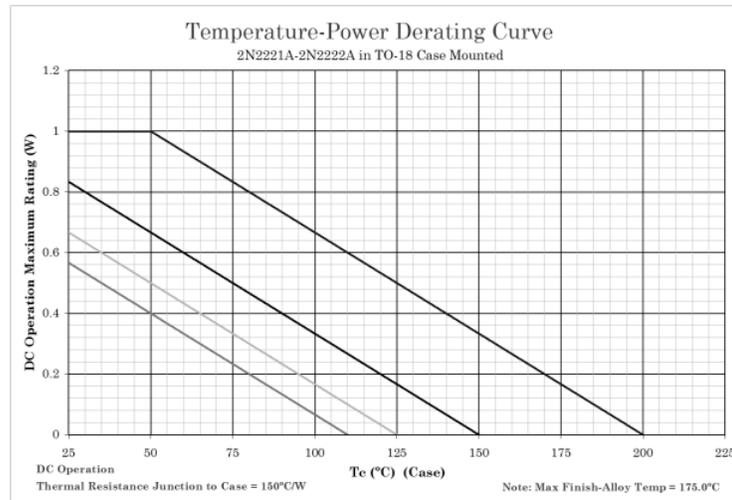
### Temperature-Power Derating Curves



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 7. Temperature-power derating for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18 package).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq +150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq +125^\circ\text{C}$ , and  $+110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 8. Temperature-power derating for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18 package case base mounted).

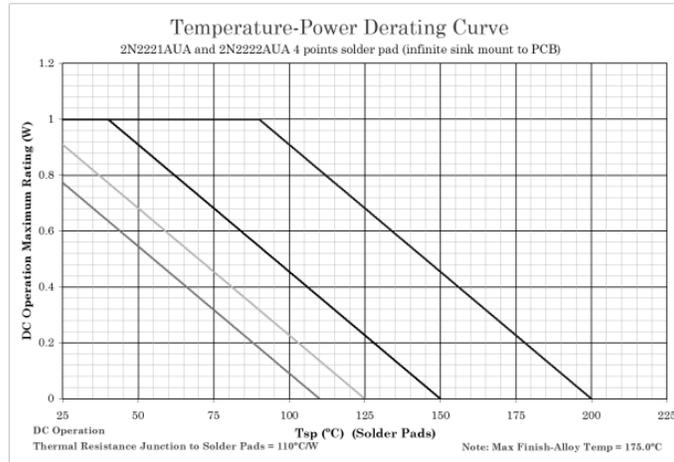
# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB



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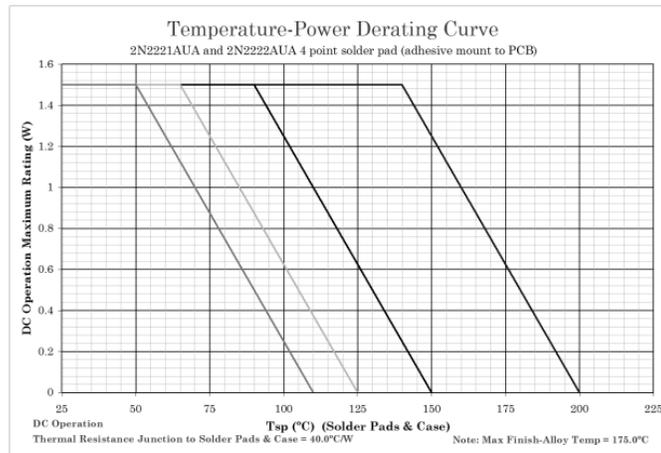
### Temperature-Power Derating Curves



**NOTES:**

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq +150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq +125^\circ\text{C}$ , and  $+110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 9. Temperature-power derating for 2N2221AUA and 2N2222AUA.



**NOTES:**

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq +150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq +125^\circ\text{C}$ , and  $+110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 10. Temperature-power derating for 2N2221AUA and 2N2222AUA.

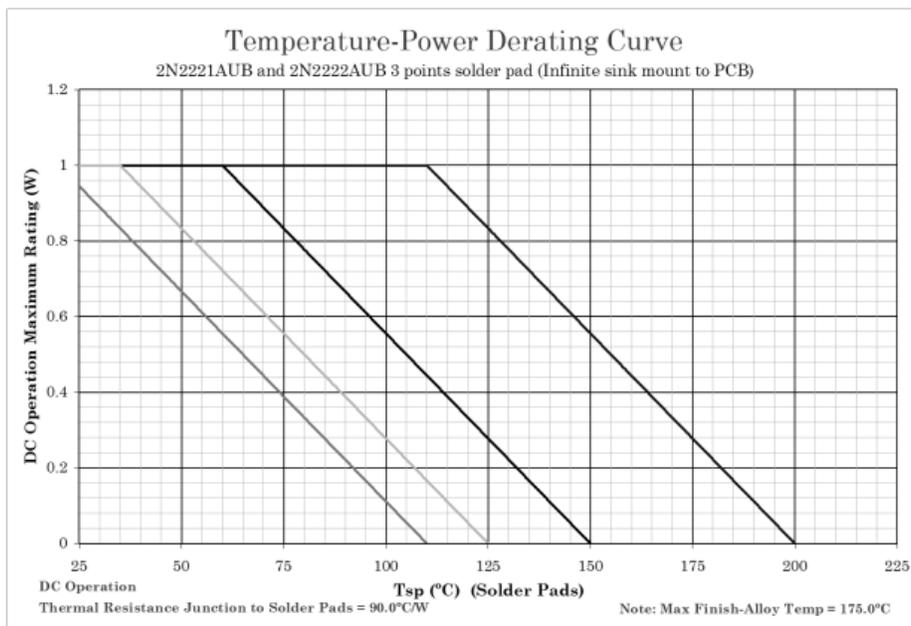
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### Temperature-Power Derating Curves



#### NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq +150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq +125^\circ\text{C}$ , and  $+110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 11. Temperature-power derating curve for 2N2221AUB and UBN and 2N2222AUB and UBCN.

### Thermal Impedance Curves

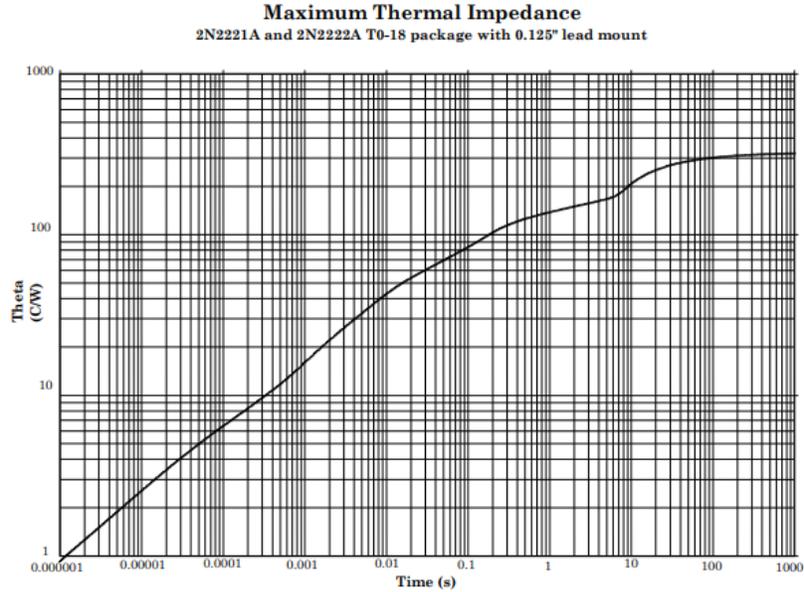


FIGURE 12. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18).

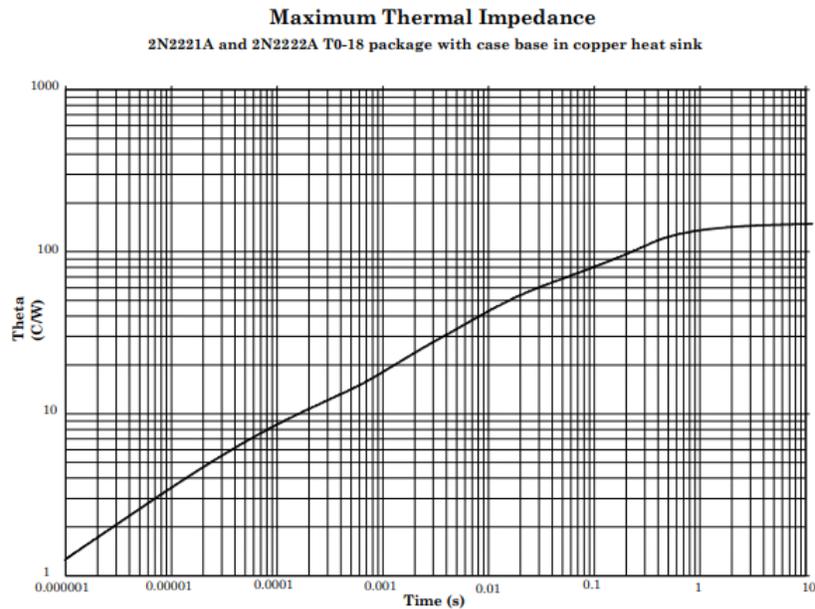


FIGURE 13. Thermal impedance graph ( $R_{\theta JC}$ ) for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18).

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### Thermal Impedance Curves

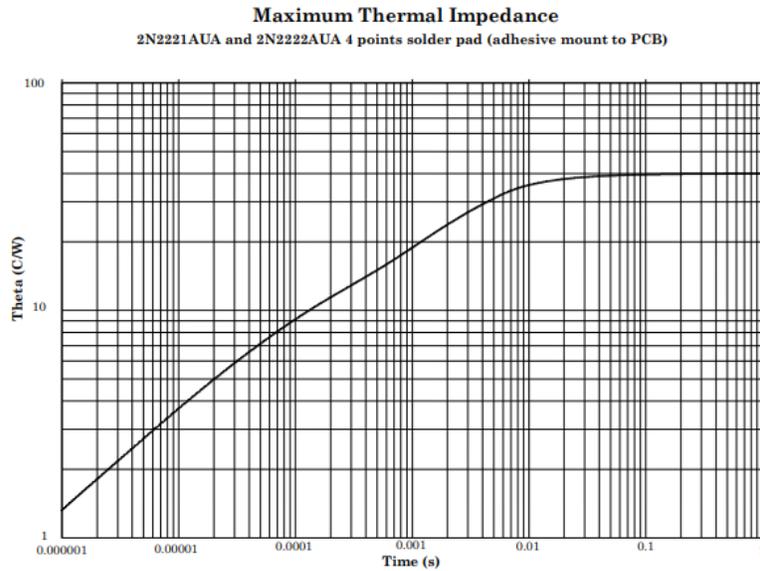


FIGURE 14. Thermal impedance graph ( $R_{\theta SP(AM)}$ ) for 2N2221AUA and 2N2222AUA.

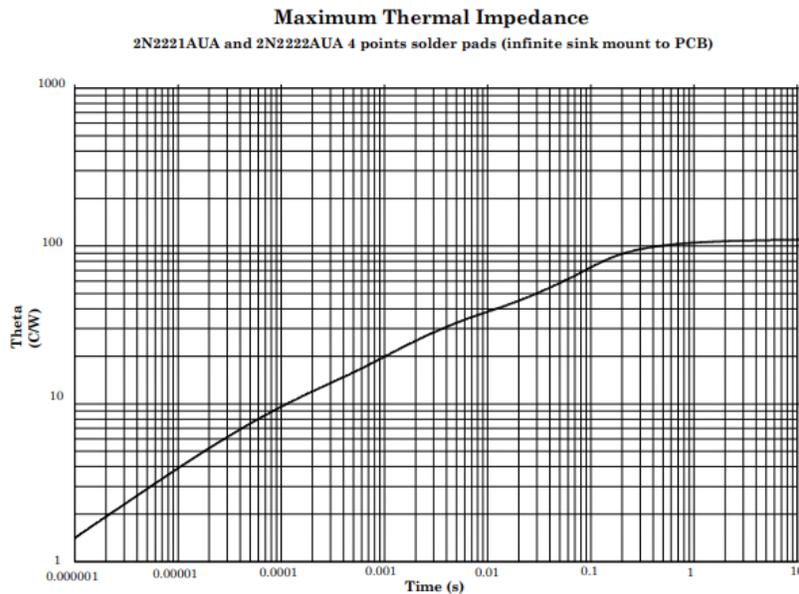


FIGURE 15. Thermal impedance graph ( $R_{\theta SP(S)}$ ) for 2N2221AUA and 2N2222AUA.

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### Thermal Impedance Curves

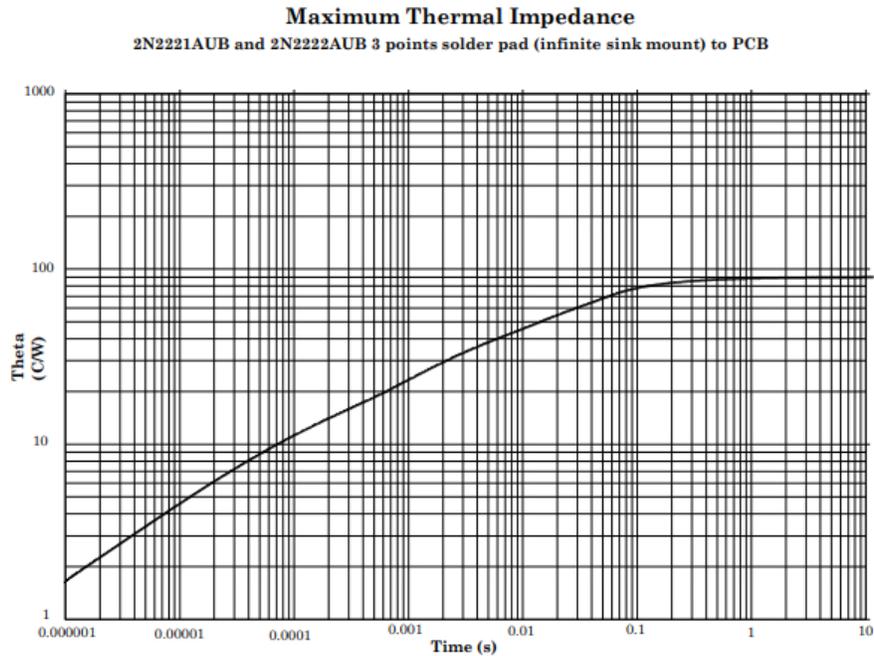


FIGURE 16. Thermal impedance graph ( $R_{\theta_{JSP(S)}}$ ) for 2N2221AUB and UBN and 2N2222AUB and UBCN.

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