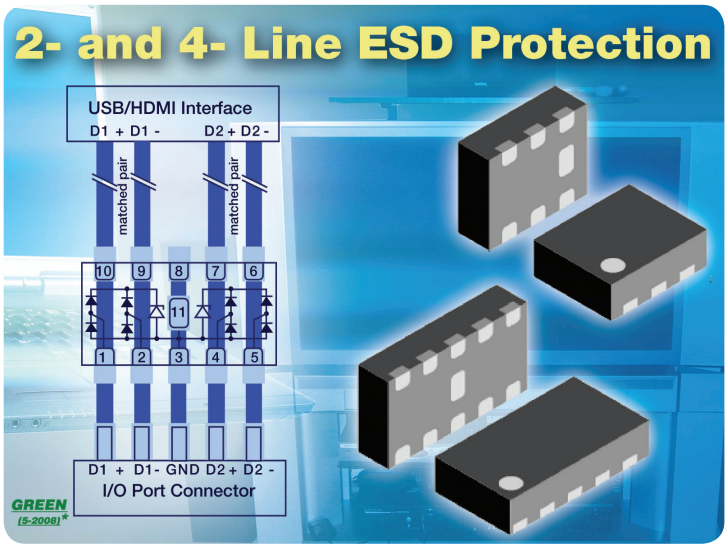
Diodes - ESD Array with Flow-Through Design

ESD Bus Port Protection Array in Ultra-Small LLPxx13 Plastic Package



FEATURES

- 2- and 4-line ESD protection with flow-through design
- Capacitance C_D = 0.8 pF
- ESD immunity = 15 kV (IEC61000-4-2)
- Compact LLP1713 or LLP2513 package with height < 0.6 mm

APPLICATIONS

- ESD protection in high-speed data applications such as USB 2.0, HDMI, display port, eSATA, and 1394/Firewire

END PRODUCTS

- HDTV and mobile electronics, including portable gaming, MP3 players, and mobile phones

BENEFITS

- Supports surge resistance requirements for high-speed data lines

RESOURCES

- Datasheet:
  - for VBUS052CD-FAH - http://www.vishay.com/doc?81881
  - for VBUS054CD-FHI - http://www.vishay.com/doc?81882
- For technical questions contact ESD-Protection@vishay.com
- Material categorization: For definitions of compliance please see http://www.vishay.com/doc?99912

Pb-free e3 RoHS COMPLIANT GREEN (5-2008)*

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FLOW THROUGH DESIGN

Modern digital transmission lines can be clocked up to 480 Mbit/s (USB2.0) or 1.65 Gbit/s (HDMI). At such high data rates the transmission lines like cables or the line traces on the PCBs have to be very homogeneous regarding their surge impedance. This requires well defined trace dimensions as trace width and distance which have to be calculated depending on the requested surge impedance (e.g. 50 Ω) and the PCB material and layer dimensions. Any device connected to the data lines - like ESD-protection devices - have to be connected with minimal changes in these trace dimensions and distances. With the package in the so called “Flow Through Design” this is possible. The lines are running straight along the PCB while the **VBUS054CD-FHI** and **VBUS052CD-FAH** is placed on top without any vias or loops.

ELECTRICAL CHARACTERISTICS VBUS052CD-FAH:

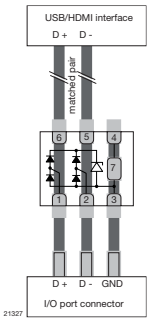
(pin 1 or 2 to pin 3, 4 or 7) (Tamb = 25 °C, unless otherwise specified)

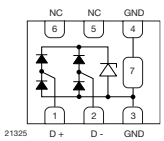
Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	2	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5	V
Reverse voltage	at I_R = 0.1 µA	V_R	5			V
Reverse current	at V_{RWM} = 5 V	I_R		< 0.01	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6.9	7.9	8.7	V
Reverse clamping voltage	at I_{PP} = 1 A	V_C		10	12	V
	at I_{PP} = I_{PPM} = 3.5 A	V_C		15	18	V
Forward clamping voltage	at I_F = 1 A	V_F		1.9	2.4	V
	at I_{PP} = I_{PPM} = 3.5 A	V_F		4	5	V
Capacitance	at V_R = 0 V; f = 1 MHz	C_D		0.8	1	pF

ELECTRICAL CHARACTERISTICS VBUS054CD-FHI:

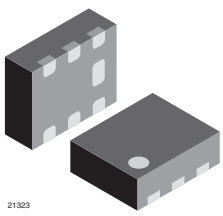
(pin 1, 2, 4 or 5 to pin 3) (Tamb = 25 °C, unless otherwise specified)

Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	4	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5	V
Reverse voltage	at I_R = 0.1 µA	V_R	5			V
Reverse current	at V_{RWM} = 5 V	I_R		< 0.01	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6.9	7.9	8.7	V
Reverse clamping voltage	at I_{PP} = 1 A	V_C		9.1	11	V
	at I_{PP} = I_{PPM} = 3.5 A	V_C		11.6	13	V
Forward clamping voltage	at I_{PP} = 1 A	V_F		1.6	2.4	V
	at I_{PP} = 3.5 A	V_F		3.5	5	V
Capacitance	at V_R = 0 V; f = 1 MHz	C_D		0.8	1	pF

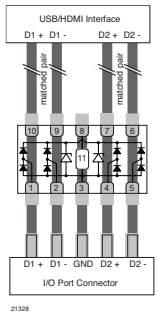


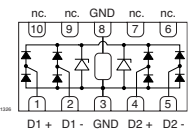


VBUS052CD-FAH
Circuit Configuration:

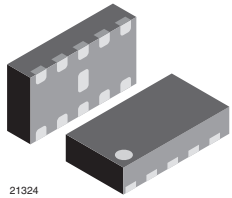


Package: LLP1713





VBUS054CD-FHI
Circuit Configuration:



Package: LLP2513