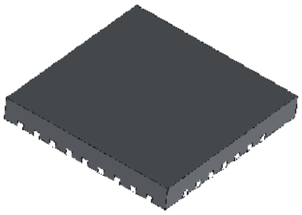
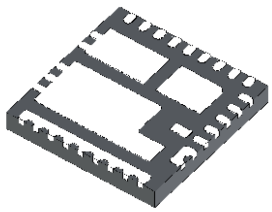
60 A VRPower® Smart Power Stage (SPS) Module with Integrated High Accuracy Current and Temperature Monitors


Top view


Bottom view

DESCRIPTION

The SiC675A is a smart VRPower® device that integrates a high side and low side MOSFET, a high performance driver with integrated bootstrap FET. The SiC675A offers high accuracy current and temperature monitors that can be fed back to the controller and doubler to complete a multiphase DC/DC system. They simplify design and increase performance by eliminating the DCR sensing network and associated thermal compensation. Light-load efficiency is supported via a dedicated left control pin. An industry leading thermally enhanced, 5 mm x 5 mm PowerPAK® MLP package allows minimal overall PCB real estate and low profile construction.

The devices feature a 3.3 V compatible tri-state PWM input that, working together with multiphase PWM controllers, will provide a robust solution in the event of abnormal operating conditions. The SiC675A also improves system performance and reliability with integrated fault protection of UVLO, over-temperature and over-current. An open-drain fault reporting pin simplifies the handshake between the smart VRPower device and multiphase controllers and can be used to disable the controller during start-up and fault conditions.

FEATURES

- Highly efficient
  - Thermally enhanced PowerPAK® MLP55-32L
  - Low-side MOSFET with integrated Schottky diode
  - Low impedance bootstrap switch
  - Low shutdown supply current (10 μA)
- Highly versatile
  - Width input range support: 4.5 V to 21 V
  - Compatible with 3.3 V PWM logic tristate / middle voltage
  - Up to 2 MHz switching frequency
- Robust and reliable
  - Delivers in excess of 60 A continuous current
  - 90 A at 10 ms peak current
  - Down slope current sensing
  - Fault protections
    - Over-temperature protection
    - V_{CC} (3.3 V) / PVCC (5 V) under-voltage lockout (UVLO)
- Effective monitoring / reporting
  - ± 3 % accuracy current monitor (I_{MON})
  - 8 mV/°C temperature monitor with OT flag
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- High frequency and high efficiency VRM and VRD
- Core, graphic, and memory regulators for microprocessors
- High density VR for server, networking, and cloud computing
- POL DC/DC converters and video gaming consoles

TYPICAL APPLICATION DIAGRAM

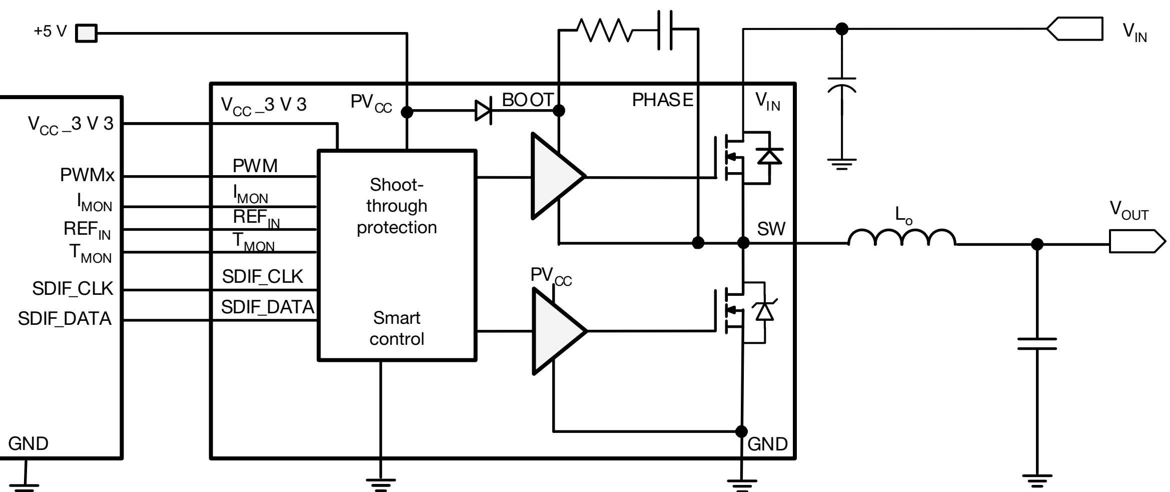


Fig. 1 - Typical Application Block Diagram

FUNCTIONAL BLOCK DIAGRAM

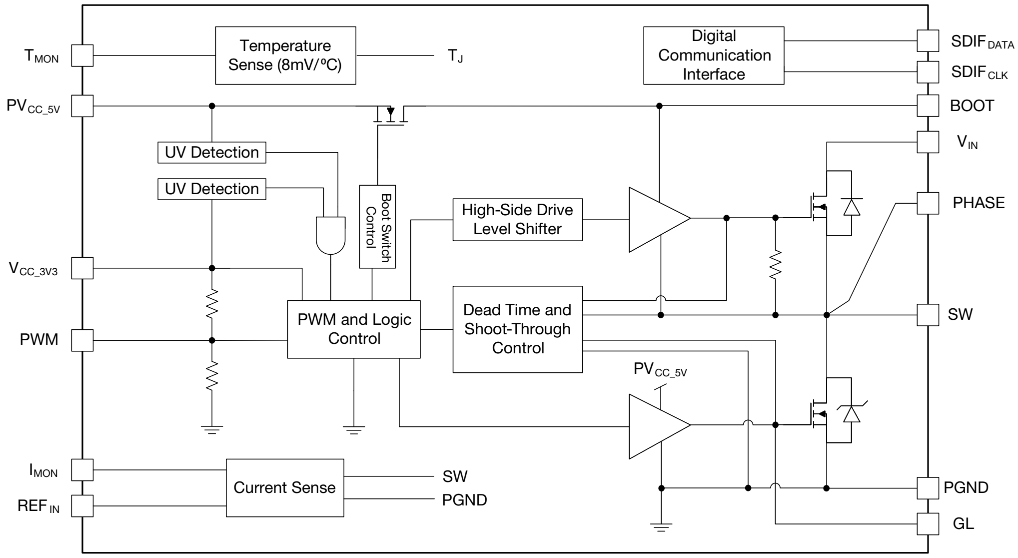


Fig. 2 - Functional Block Diagram

ORDERING INFORMATION

PART NUMBER	MARKING CODE	TEMPERATURE RANGE (°C)	PWM INPUT (V)	PACKAGE (RoHS-compliant)
SiC675ACD-T1-GE3	SiC675A	-40 to +125	3.3	MLP30-55L

PINOUT CONFIGURATION

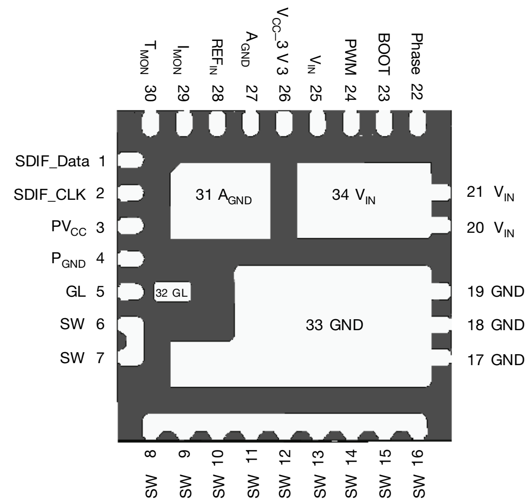


Fig. 3 - Pinout Configuration

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	SDIF_DATA	Serial digital interface data input and output. Connect 1 kΩ to 3.3 V
2	SDIF_CLK	Serial digital interface clock input
3	PV_{CC}	+5 V logic and gate drive bias supply. Place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to A_{GND}
4, 17, 18, 19, 33	P_{GND}	Power ground (source connection of low side MOSFET)
5, 32	GL	This is a low side gate driver output (GL)
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16	SW	No connect (this is a low side gate driver output (GL), optional to monitor for system debugging)
20, 21, 25, 34	V_{IN}	Input of power stage (to drain of High side MOSFET). Place at least 2 ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and P_{GND}. For optimal performance, place as many vias as possible in the bottom side V_{IN} paddle
22	PHASE	Return of boot capacitor. Internally connected to SW node so no external routing required for SW connection
23	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins
24	PWM	PWM input of gate driver, compatible with 3.3 V tri-state PWM signal
26	V_{CC}_3 V 3	+3.3 V logic bias supply. Place a high quality low ESR ceramic capacitor (~1µF/X7R) in close proximity from this pin to GND
27, 31	A_{GND}	A_{GND} of driver IC
28	REF_{IN}	Input for external reference voltage for I_{MON} signal. This voltage should be between 0.8 V and 1.3 V. Connect REF_{IN} to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to A_{GND}
29	I_{MON}	Current monitor output, referenced to REF_{IN}. Pulls low to indicate ZCD in DCM mode. Connect the I_{MON} output to the appropriate current sense input of the controller. No more than 56pF capacitance can be directly connected across the I_{MON} and REF_{IN} pins.
30	T_{MON}	Temperature monitor output. For multiphase, the T_{MON} pins can be connected together as a common bus; the highest voltage (representing the highest temperature) will be sent to the PWM controller. T_{MON} will be pulled high (to 2.5 V) to indicate an over-temperature fault. No more than 250 pF total capacitance can be directly connected across T_{MON} and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kΩ for 100 nF load

ABSOLUTE MAXIMUM RATINGS				
ELECTRICAL PARAMETER	**SYMBOL**	**CONDITONS**	**LIMIT**	**UNIT**
Supply voltage	V_{CC}_3 V 3		-0.3 to +4.3	V
	PV_{CC}_5 V		-0.3 to +6	
Input supply voltage	V_{IN}		-0.3 to +30	
V_{IN}_PHASE	V_{IN_PHASE}	AC, 5ns	-0.3 to +40	
PHASE, SW voltage (AC)	V_{PH_GND}, V_{SW_GND}	AC, 5ns	-0.3 to +45	
			-10 to +45	
BOOT voltage	V_{BOOT_GND}		-0.3 to +50	
Other I/O pin voltage			-0.3 to V_{CC} +0.3	
ESD RATING				
Human Body Mode		JS-001-2017	2	kV
Charged Device Mode		JS-002-2014	750	V
Latch-up		JESD78E; Class 2, level A	100	mA
THERMAL INFORMATION				
Maximum junction temperature			150	°C
Maximum storage temperature range			-65 to +150	
Lead (Pb)-free reflow profile				-
POWER RATING				
Maximum instant power dissipation		T_A = 25 °C, 150 A [b]	100	W
Maximum continuous power dissipation		T_A = 25 °C, Θ_{JA} = 10 °C/W, T_J = 150 °C [b]	12.5	
THERMAL RESISTANCE				
Thermal resistance junction to PCB	Θ_{JB}	[b]	5.2	°C/W
Thermal resistance junction to ambient	Θ_{JA}	0 LFM [b]	10.7	
		400 LFM [b]	9.3	

Notes

a. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

b. Θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features

c. For Θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside

d. These ratings vary with PCB layout and operating condition, and limited by device temperature and thermal shutdown trip point

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
Operating junction temperature range	-40	-	125	°C
Supply voltage V_{CC}_3 V 3	3.135	-	3.465	V
Supply voltage PV_{CC}_5 V	4.75	-	5.25	
Input supply voltage (V_{IN})	4.5	-	21	

ELECTRICAL SPECIFICATIONS (recommended operating conditions, unless otherwise noted. T_J = -40 °C to +125 °C)						
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN. (1)	TYP.	MAX. (1)	
V_{CC} SUPPLY CURRENT						
Logic standby current	I_{VCC_3V3}	PWM = mid-level voltage	-	1.7	-	mA
Gate drive standby current	I_{PVCC}	PWM = mid-level voltage	-	3.6	-	μA
Logic operational current	I_{VCC_3V3}	PWM = 300 kHz	-	1.7	-	mA
Gate drive operation current	I_{PVCC}	PWM = 300 kHz	-	7.5	-	mA
POWER-ON RESET AND ENABLE						
PV_{CC} rising POR threshold			3.63	4.2	4.79	V
PV_{CC} falling POR threshold			3.4	3.9	4.4	V
PV_{CC_3V3} rising POR threshold			-	2.7	3.1	V
PV_{CC_3V3} falling POR threshold			2.1	2.45	-	V
PV_{CC_3V3} POR delay to operation			-	250	-	μs
3.3 V PWM INPUT						
Mid-point lower gate falling threshold		V_{CC_3V3} = 3.3 V, PV_{CC} = 5 V	-	1	-	V
Mid-Point lower gate rising threshold		V_{CC_3V3} = 3.3 V, PV_{CC} = 5 V	-	0.8	-	V
Mid-Point upper gate rising threshold		V_{CC_3V3} = 3.3 V, PV_{CC} = 5 V	-	2.44	-	V
Mid-Point upper gate falling threshold		V_{CC_3V3} = 3.3 V, PV_{CC} = 5 V	-	2.39	-	V
Mid-point shutdown window		V_{CC_3V3} = 3.3 V, PV_{CC} = 5 V	1.14	-	2.3	V
CURRENT MONITOR AND PROTECTION						
REFIN voltage range			0.8	1.2	1.3	V
I_{OUT} closed loop current gain accuracy with renesas digital multiphase controller V_{CC_3V3} = 3.3 V, PV_{CC} = 5 V		≥ 10 A, T_J = +0 °C to +125 °C	-	±3	-	%
		≥ 10 A, T_J = -40 °C to +0 °C	-	±5	-	%
I_{MON} high at over-temperature			-	3.26	-	V
TEMPERATURE MONITOR						
Over-temperature rising threshold			-	150	-	°C
Over-temperature falling threshold			-	130	-	°C
Over-temperature hysteresis			-	18	-	°C
Temperature coefficient			-	0.008	-	mV/K
T_{MON} voltage at +25 °C temperature		V (T_J) = 0.6 V + (8 mV x T_J)	-	0.80	-	V
BOOTSTRAP DIODE						
Forward voltage drop			-	84	-	mV
On-resistance	R_F		-	17	-	Ω

Notes

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design

(2) These ratings vary with PCB layout and operating condition, and limited by SPS temperature and thermal shutdown trip point

(3) Limits apply across the operating temperature range

TIMING DIAGRAM

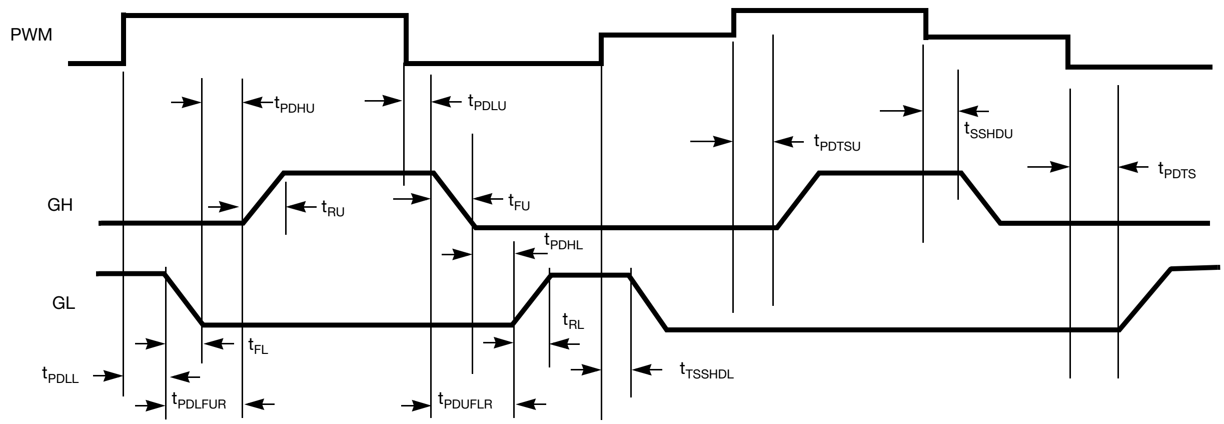


Fig. 4 - Timing Diagram

DETAILED OPERATIONAL DESCRIPTION

The SiC675A is an optimized driver and power stage solution for high density synchronous DC/DC power conversion. It includes high performance GH and GL drivers, a NFET controlled to function as a bootstrap diode, and MOSFET pair optimized for high switching frequency buck voltage regulators. It also includes advanced power management features.

1. Accurate current and thermal reporting outputs
2. Fault protections of HFET over-current, HFET short, over-temperature, V_{CC} UVLO, and V_{IN} UVLO

Power-On Reset (POR)

The V_{CC}_3V3 voltage rise is monitored during initial start-up. If the rising V_{CC}_3V3 voltage exceeds 2.7 V (typical), and the rising $PV_{CC}5$ voltage exceeds 4.13 V normal operation of the driver is enabled after correct initialization by the controller. The PWM signals are passed through to the gate drivers, the T_{MON} output is valid and the I_{MON}- REF_{IN} output starts at zero, and becomes valid on the first GL signal. The driver operation is disabled if either V_{CC}_3V3 or $PV_{CC}5$ drops below its falling threshold.

Bootstrap Function

The SiC675A features an internal NFET that is controlled to function as a bootstrap diode. A high quality ceramic capacitor should be placed in close proximity across the BOOT and PHASE pins. The bootstrap capacitor can range between 0.1 μF to 0.22 μF (0402 to 0603 and X5R to X7R) for normal buck switching applications.

Shoot-Through Protection

Before $PV_{CC}5/V_{CC}$_3V3 POR, the undervoltage protection function is activated and both GH and GL are held active low (HFET and LFET off). If the driver has no bias voltage applied (either V_{CC}_3V3 or $PV_{CC}5$ are missing) and is unable to actively hold the MOSFETs off, an integrated 20 kΩ resistor from the upper MOSFET gate-to-source helps keep the HFET device in its off state. This shoot-through protection can be especially critical in applications in which the input voltage rises before the SiC675A V_{CC}_3V3 and $PV_{CC}5$ supplies.

After POR (the Rising Thresholds; see "Electrical Specifications" on page 7) and a 210 μs delay, the PWM signal is used to control both high-side and low-side MOSFETs.

During switching operation, the SiC675A dead time is optimized for high efficiency and ensures that simultaneous conduction of both FETs cannot occur.

Serial Digital Interface (DSDIF) Bus

The SDIF Bus is used for communication between the SiC675A driver and an appropriate digital multi-phase controller such as the RAA225000 and RAA225001. This communication is used to optimize I_{MON} data and power draw in each individual smart power stage in the system.

Current Monitoring

The LFET current is monitored and a signal proportional to that current is the output on the I_{MON} pin (relative to the REF_{IN} pin) without thermal and V_{CC}_3V3 compensations, which are done inside the controller after SDIF bus polls the information from SPS. Connect the I_{MON} and REF_{IN} pins to the appropriate current sense input pin of the controller. This method does not require external RSENSE or DCR sensing of the inductor current.

Figure 2 depicts the low-side current sense concept. After the falling edge of the PWM, there are two delays: one that represents the expected propagation delay from PWM to GH/SW and a second blanking delay to allow time for the transition to settle; typical total time is ~350ns. The I_{MON} output (within controller) approximates the actual IL waveform.

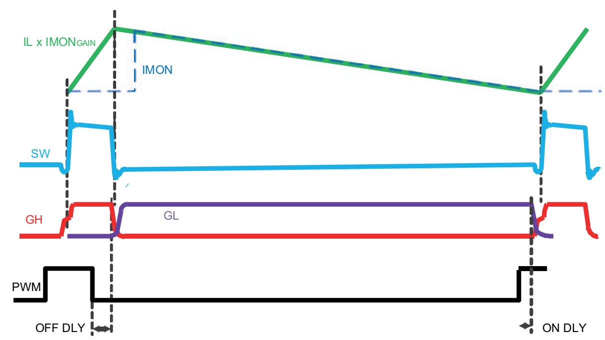


Fig. 5 - LFET Current Sample Diagram

The HFET current is NOT monitored in the same way, so no valid measured current is available while PWM is high (including the short delays before and after). During this time, the I_{MON} outputs the last valid LFET current before the sampling stopped. On start up after POR, the I_{MON} outputs zero (relative to REF_{IN}, which represents zero current) until the switching begins and the current can be properly measured.

Thermal Monitoring

The SiC675A monitors its internal temperature and provides a signal proportional to that temperature on the T_{MON} pin. T_{MON} has a voltage of 600mV at 0°C and reflects temperature at 8mV/°C. The T_{MON} output is valid after the proper command from the controller over the SDIF bus.

In a multiphase, or multi-rail, application each T_{MON} pin will be tied together and a single signal is routed back to the controller. However, each SiC675A will only report its temperature after the appropriate command is sent over the SDIF bus. This allows for individual phase temperature readings instead of simply the maximum temperature at any given time.

If an over-temperature fault occurs, the I_{MON} pin is pulled high to 3.3V.

Thermal Protection

If the internal temperature exceeds the over-temperature trip point (+140°C typical), the I_{MON} pin is pulled to 3.3 V and no other action is taken on-chip. The I_{MON} remains in the fault mode until the junction temperature drops below +130°C (typical); at that point, the I_{MON} resumes normal operation.

FAULT Reporting

Over-temperature detection pulls the I_{MON} pin to a high (3.3V, fault) level, so that the PWM controller quickly recognizes it as out of the normal range.

The fault reporting and respective SPS response are summarized in Table 2.

TABLE 2 - FAULT REPORTING SUMMARY

FAULT EVENT	I_{MON}	RESPONSE
OT	High	Wait for input from controller
PV_{CC} UVLO	I_{MON} - REF_{IN} = 0 V	Switching stops while in UVLO. When above PV_{CC}5 POR, after 210µs: GH and GL follow PWM, T_{MON} is valid, and I_{MON}-REF_{IN} is valid after GL first goes low
V_{CC}_3V3 UVLO	I_{MON} - REF_{IN} = 0 V	Switching stops while in UVLO. Driver requires reinitialization from controller to resume normal operation

PCB LAYOUT CONSIDERATIONS

Proper PCB layout will reduce noise coupling to other circuits, improve thermal performance, and maximize the efficiency. The following is meant to lead to an optimized layout:

- Place multiple 10 µF or greater ceramic capacitors directly at device between V_{IN} and P_{GND}. This is the most critical decoupling and reduced parasitic inductance in the power switching loop. This will reduce overall electrical stress on the device as well as reduce coupling to other circuits. Best practice is to place the decoupling capacitors on the same PCB side as the device. For a design with tight space requirements, these decoupling capacitors can be placed under the device, i.e., bottom layer.
- Connect GND to the system GND plane with a large via array as close to the GND pins as design rules allow. This improves thermal and electrical performance.
- Place PV_{CC}, V_{CC} and BOOT-PHASE decoupling capacitors at the IC pins.
- Note that the SW plane connecting the SiC675A and inductor must carry full load current and will create resistive loss if not sized properly. However, it is also a very noisy node that should not be oversized or routed close to any sensitive signals. Best practice is to place the inductor as close to the device as possible and thus minimizing the required area for the SW connection. If one must choose a long route of either the V_{OUT} side of the inductor or the SW side, choose the quiet V_{OUT} side. Best practice is to locate the SiC648 as close to the final load as possible and thus avoid noisy or lossy routes to the load.
- The I_{MON} and IREF network and their vias should not sit on the top of the V_{IN} plane, a keep out area is recommended.
- The PCB is the best thermal heatsink material than any top side cooling materials. The PCB always has enough vias to connect V_{IN} and GND planes. Insufficient vias will yield lower efficiency and very poor thermal performance.

PRODUCT SUMMARY	
Part number	SiC675A
Description	60 A smart power stage, 4.5 V_{IN} to 21 V_{IN}, 3.3 V PWM with diode emulation mode
Input voltage min. (V)	4.5
Input voltage max. (V)	21
Current rating (A)	60
Switch frequency max. (kHz)	2000
Enable (yes / no)	No
Monitoring features	I_{MON}, T_{MON}
Protection	UVLO, OCP, OTP
Light load mode	Diode emulation
Pulse-width modulation (V)	3.3
Package type	PowerPAK® MLP30-55L
Package size (W, L, H) (mm)	5.0 x 5.0 x 0.75
Status code	1
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

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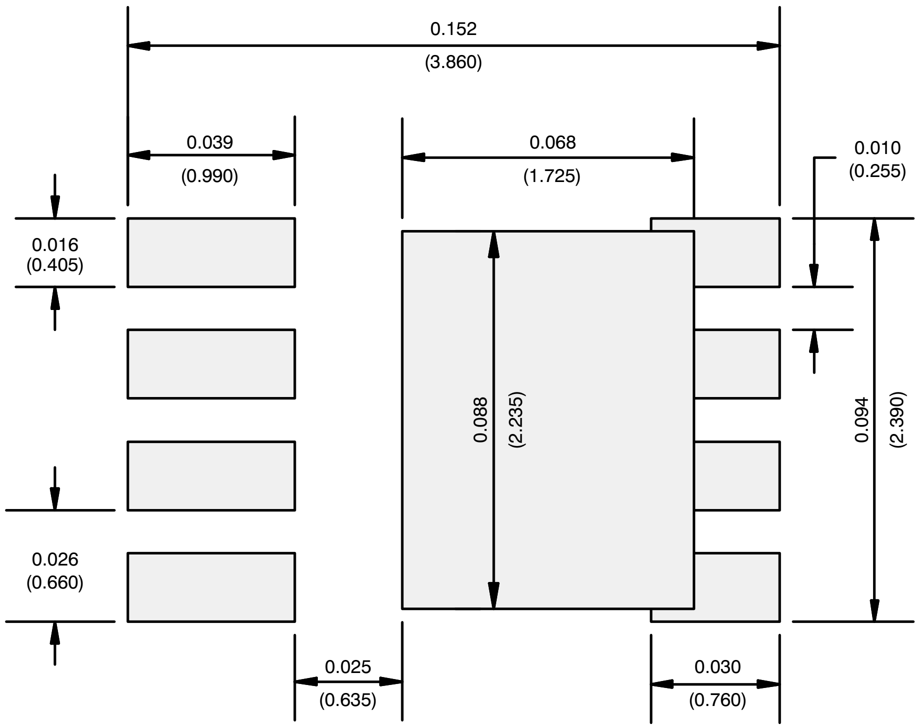
RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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