# Quad Complementary CMOS Analog Switch

## DESCRIPTION

The versatile DG213 analog switch has two NC and two NO switches. It can be used in various configurations, including four single-pole single-throw (SPST), two single-pole double-throw (SPDT), one “T” switch, one DPDT, etc. This device is fabricated in a Vishay Siliconix’ proprietary high-voltage silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

This analog switch was designed for a wide variety of general purpose applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. These switches can handle up to ± 22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All switches feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

For additional information, please refer to Application Note AN208 (www.vishay.com/doc?70606).

## BENEFITS

- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Low cost

## FEATURES

- ± 22 V supply voltage rating
- TTL and CMOS compatible logic
- Low on-resistance - $R_{DS(on)}$: 45 Ω
- Low leakage - $I_{D(on)}$: 20 pA
- Single supply operation possible
- Extended temperature range
- Fast switching - $t_{on}$: 85 ns
- Low charge injection - Q: 1 pC
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

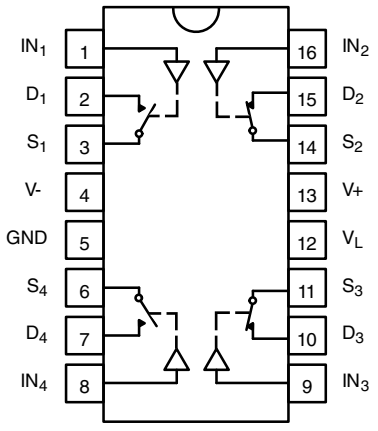
RoHS COMPLIANT

## APPLICATIONS

- Industrial instrumentation
- Test equipment
- Communications systems
- Disk drives
- Computer peripherals
- Portable instruments
- Sample-and-hold circuits

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG213**
**Dual-In-Line. SOIC and TSSOP**




Top View

| TRUTH TABLE | | |
|---|---|---|
| LOGIC | SW1, SW4 | SW2, SW3 |
| 0 | Off | On |
| 1 | On | Off |

**Note**

- Logic “0” ≤ 0.8 V
  Logic “1” ≥ 2.4 V

| ORDERING INFORMATION | | |
|---|---|---|
| **TEMP. RANGE** | **PACKAGE** | **PART NUMBER** |
| -40 °C to +85 °C | 16-pin narrow SOIC | DG213DY-E3<br>DG213DY-T1-E3 |
| | 16-pin TSSOP | DG213DQ-E3<br>DG213DQ-T1-E3 |
| | 16-pin plastic DIP | DG213DJ-E3 |

| **ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted) | | | |
|---|---|---|---|
| **PARAMETER** | | **LIMIT** | **UNIT** |
| Voltages referenced, V+ to V- | | 44 | V |
| GND | | 25 | |
| Digital inputs [a], $V_S$, $V_D$ | | (V-) - 2 to (V+) + 2<br>or 30 mA, whichever occurs first | |
| Current (any terminal) | | 30 | mA |
| Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.) | | 100 | |
| Storage temperature | | -65 to +125 | °C |
| Power dissipation (package) [b] | 16 pin plastic DIP [c] | 470 | mW |
| | 16 pin narrow SOIC [d] | 640 | |
| | 16 pin narrow TSSOP [d] | 500 | |

**Notes**

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 6.5 mW/°C above 75 °C
d. Derate 7.6 mW/°C above 75 °C

## SCHEMATIC DIAGRAM (typical channel)

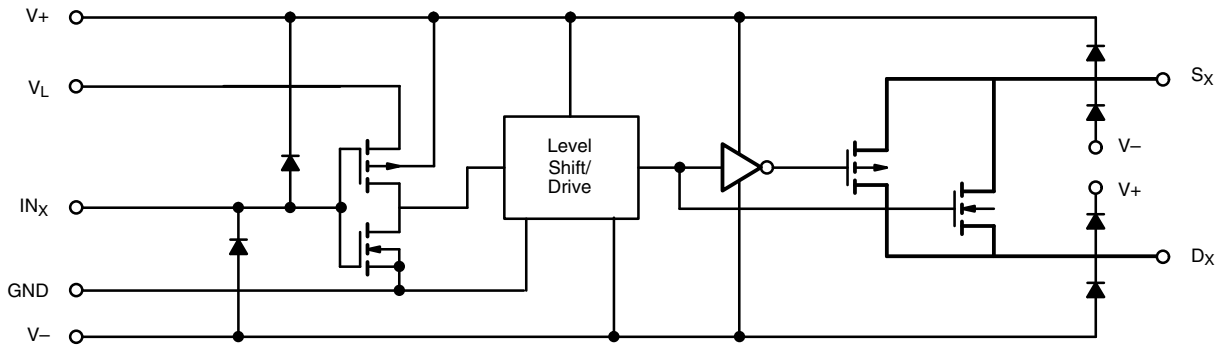



**Fig. 1**

## SPECIFICATIONS

| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V $V_L$ = 5 V, $V_{IN}$ = 2.4 V, 0.8 V [e] | TEMP.[a] | D SUFFIX -40 °C to +85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN. [c] | TYP. [b] | MAX. [c] | |
| **Analog Switch** | | | | | | | |
| Analog signal range [d] | $V_{ANALOG}$ | | Full | V- | - | V+ | V |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_D$ = ± 10 V, $I_S$ = 1 mA | Room | - | 45 | 60 | Ω |
| | | | Full | - | - | 85 | |
| $R_{DS(on)}$ match | $\Delta R_{DS(on)}$ | | Room | - | 1 | 2 | |
| Source off leakage current | $I_{S(off)}$ | $V_S$ = ± 14 V, $V_D$ = ± 14 V | Room | -0.5 | ± 0.01 | 0.5 | nA |
| | | | Full | -5 | - | 5 | |
| Drain off leakage current | $I_{D(off)}$ | $V_D$ = ± 14 V, $V_S$ = ± 14 V | Room | -0.5 | ± 0.01 | 0.5 | |
| | | | Full | -5 | - | 5 | |
| Drain on leakage current | $I_{D(on)}$ | $V_S$ = $V_D$ = ± 14 V | Room | -0.5 | ± 0.02 | 0.5 | |
| | | | Full | -10 | - | 10 | |
| **Digital Control** | | | | | | | |
| Input voltage high | $V_{INH}$ | | Full | 2.4 | - | - | V |
| Input voltage low | $V_{INL}$ | | Full | - | - | 0.8 | |
| Input current | $I_{INH}$ or $I_{INL}$ | $V_{INH}$ or $V_{INL}$ | Full | -1 | - | 1 | µA |
| Input capacitance | $C_{IN}$ | | Room | - | 5 | - | pF |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time | $t_{on}$ | $V_S$ = 10 V, see Fig. 9 | Room | - | 85 | 130 | ns |
| Turn-off time | $t_{off}$ | | Room | - | 55 | 100 | |
| Turn-off time | $t_D$ | $V_S$ = 10 V, see Fig. 10 | Room | 15 | 25 | - | |
| Charge injection | Q | $C_L$ = 1000 pF, $V_{gen}$ = 0 V, $R_{gen}$ = 0 Ω | Room | - | 1 | - | pC |
| Source-off capacitance | $C_{S(off)}$ | $V_S$ = 0 V, f = 1 MHz | Room | - | 5 | - | pF |
| Drain-off capacitance | $C_{D(off)}$ | | Room | - | 5 | - | |
| Channel-on capacitance | $C_{D(on)}$ | $V_D$ = $V_S$ = 0 V, f = 1 MHz | Room | - | 16 | - | |
| Off isolation | $O_{IRR}$ | $C_L$ = 15 pF, $R_L$ = 50 Ω, $V_S$ = 1 $V_{RMS}$, f = 100 kHz | Room | - | 90 | - | dB |
| Channel to channel crosstalk | $X_{TALK}$ | | Room | - | 95 | - | |
| **Power Supply** | | | | | | | |
| Positive supply current | I+ | $V_{IN}$ = 0 V or 5 V | Room | - | - | 1 | µA |
| | | | Full | - | - | 5 | |
| Negative supply current | I- | | Room | -1 | - | - | |
| | | | Full | -5 | - | - | |
| Logic supply current | $I_L$ | | Room | - | - | 1 | |
| | | | Full | - | - | 5 | |
| Power supply range for continuous operation | $V_{OP}$ | | Full | ± 3 | - | ± 22 | V |

**Notes**

a. Room = 25 °C, full = as determined by the operating temperature suffix
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guaranteed by design, not subject to production test
e. $V_{IN}$ = input voltage to perform proper function

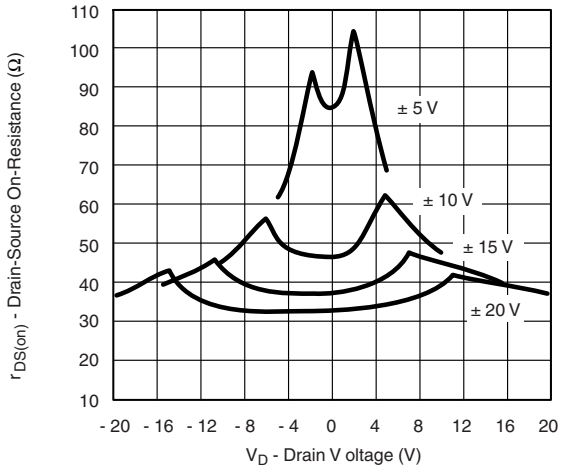
| **SPECIFICATIONS** (for Single Supply) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 12 V, V- = 0 V $V_L$ = 5 V, $V_{IN}$ = 2.4 V, 0.8 V [e] | **TEMP.[a]** | **D SUFFIX** -40 °C to +85 °C | | | **UNIT** |
| | | | | **MIN. [c]** | **TYP. [b]** | **MAX. [c]** | |
| **Analog Switch** | | | | | | | |
| Analog signal range [d] | $V_{ANALOG}$ | | Full | V- | - | V+ | V |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_D$ = 3 V, $I_S$ = 1 mA | Room | - | 90 | 110 | Ω |
| | | | Full | - | - | 140 | |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time | $t_{on}$ | See Fig. 9 | Room | - | 125 | 200 | ns |
| Turn-off time | $t_{off}$ | | Room | - | 45 | 100 | |
| Break-before-make time delay | $t_D$ | $V_S$ = 8 V, see Fig. 10 | Room | 50 | 80 | - | |
| Charge injection | Q | $C_L$ = 1 nF, $V_{gen}$ = 6 V, $R_{gen}$ = 0 Ω | Room | - | 4 | - | pC |
| **Power Supply** | | | | | | | |
| Positive supply current | I+ | $V_{IN}$ = 0 V or 5 V | Room | - | - | 1 | µA |
| | | | Full | - | - | 5 | |
| Negative supply current | I- | | Room | -1 | - | - | |
| | | | Full | -5 | - | - | |
| Logic supply current | $I_L$ | | Room | - | - | 1 | |
| | | | Full | - | - | 5 | |
| Power supply range for continuous operation | $V_{OP}$ | | Full | + 3 | - | + 40 | V |

**Notes**

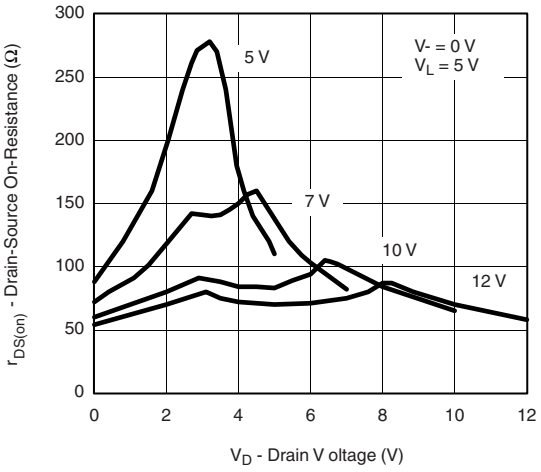
a. Room = 25 °C, full = as determined by the operating temperature suffix
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guaranteed by design, not subject to production test
e. $V_{IN}$ = input voltage to perform proper function

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

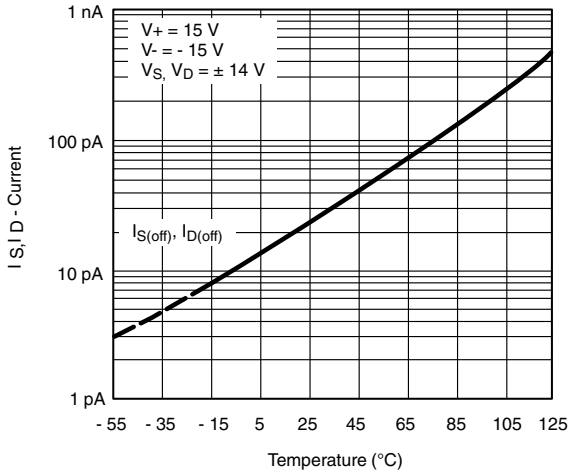



**$R_{DS(on)}$ vs. $V_D$ and Power Supply Voltages**

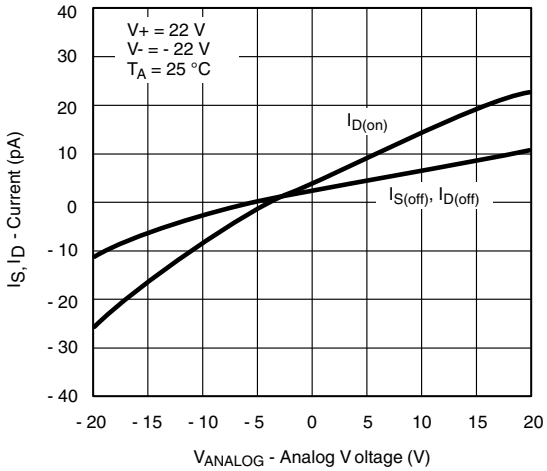



**$R_{DS(on)}$ vs. $V_D$ and Single Power Supply Voltages**

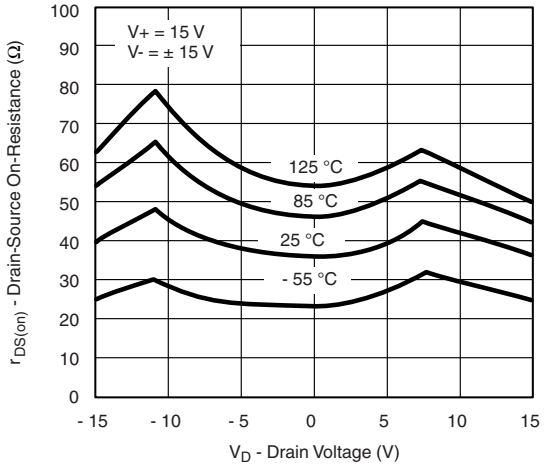
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



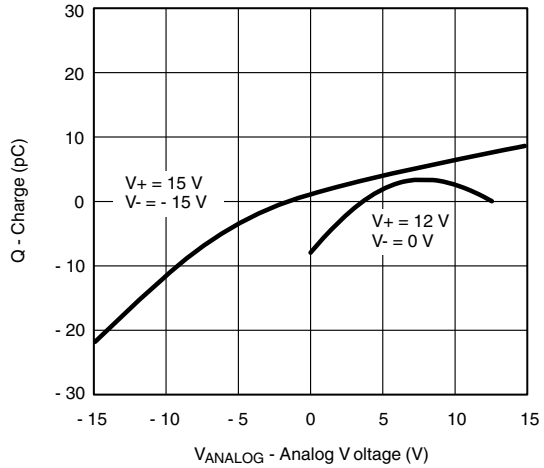

**Leakage Current vs. Temperature**



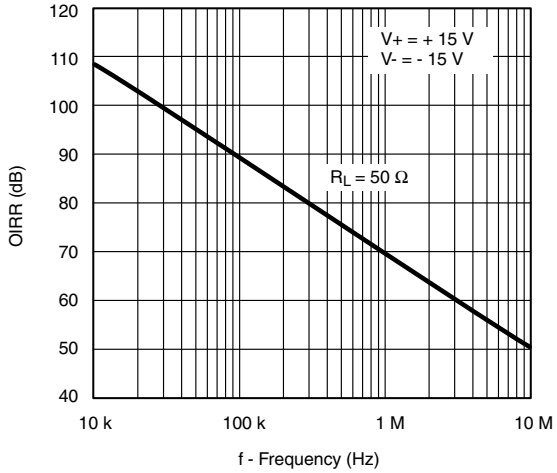

**Leakage Currents vs. Analog Voltage**




**$R_{DS(on)}$ vs. $V_D$ and Temperature**

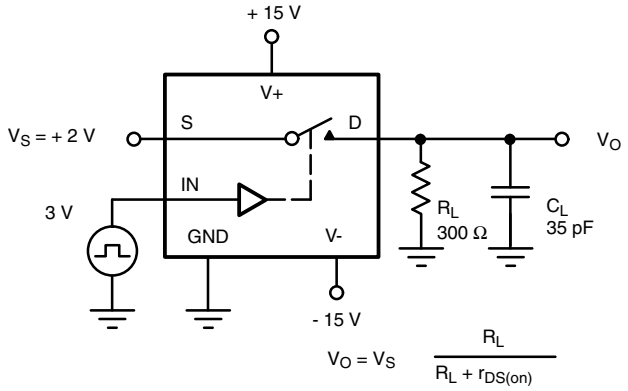



**$Q_S$, $Q_D$ - Charge Injection vs. Analog Voltage**




**Off Isolation vs. Frequency**

## TEST CIRCUITS



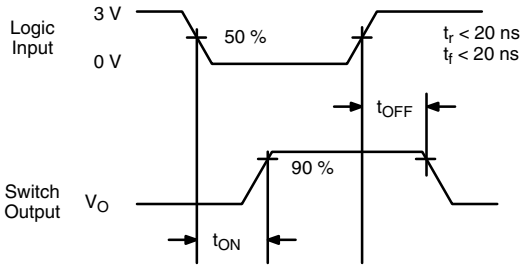
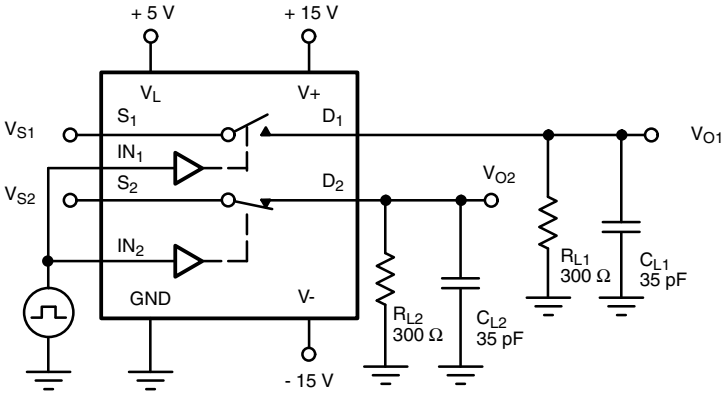
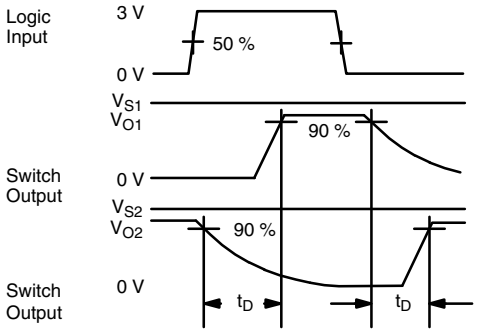




**Fig. 2 - Switching Time**




$C_L$ (includes fixture and stray capacitance)

**Fig. 3 - Break-Before-Make**

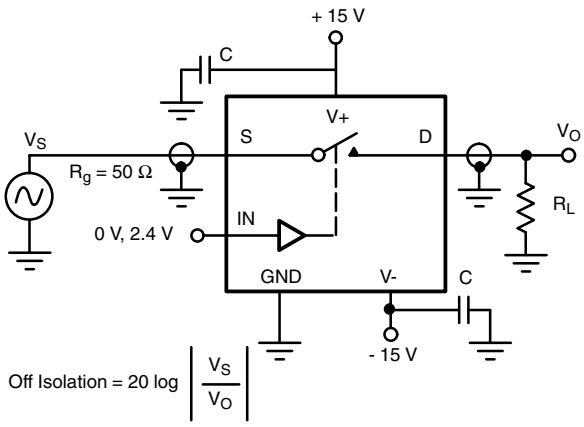



**Fig. 4 - Off Isolation**

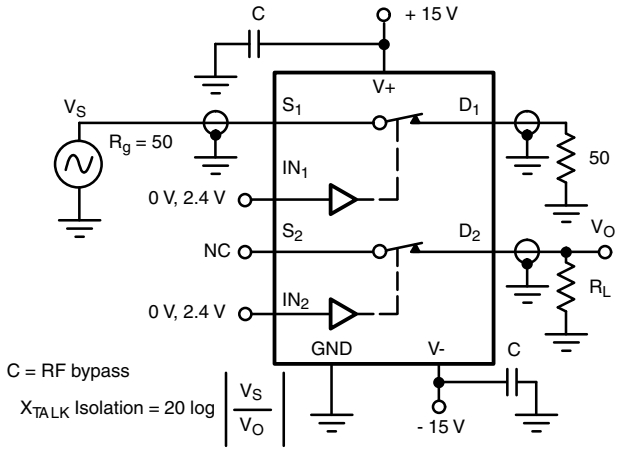
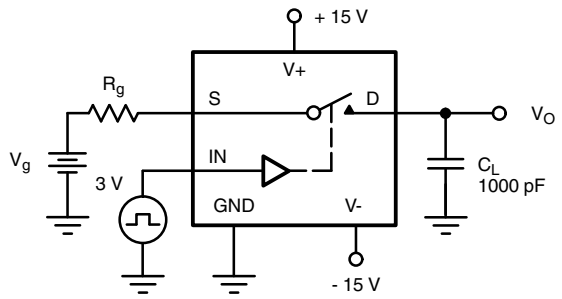
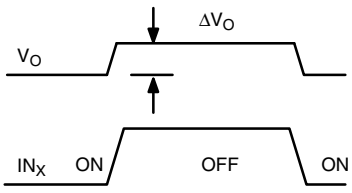



**Fig. 5 - Channel-to-Channel Crosstalk**

## TEST CIRCUITS




$\Delta V_O$ = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

**Fig. 6 - Charge Injection**

## APPLICATIONS

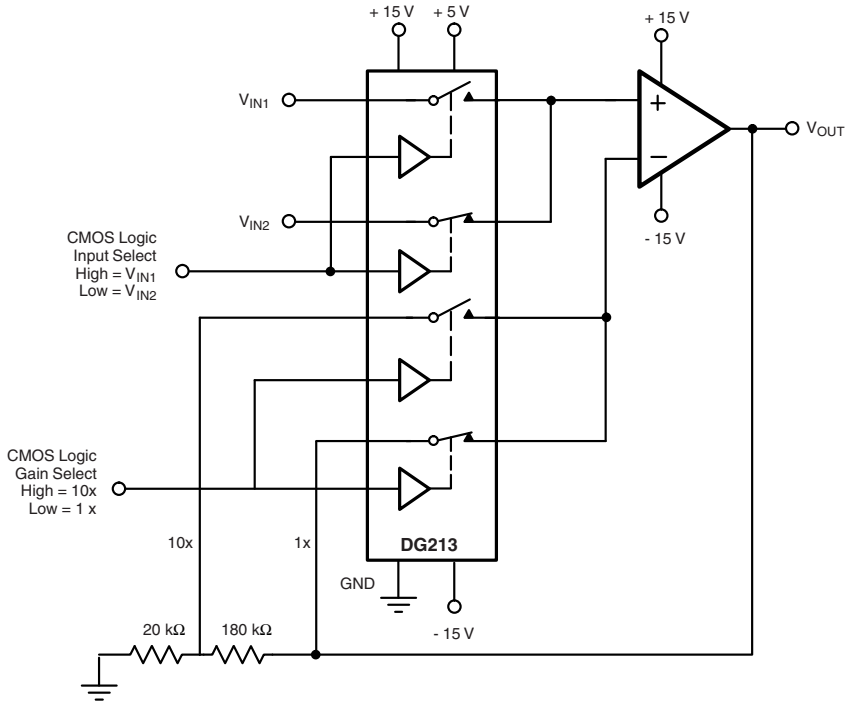
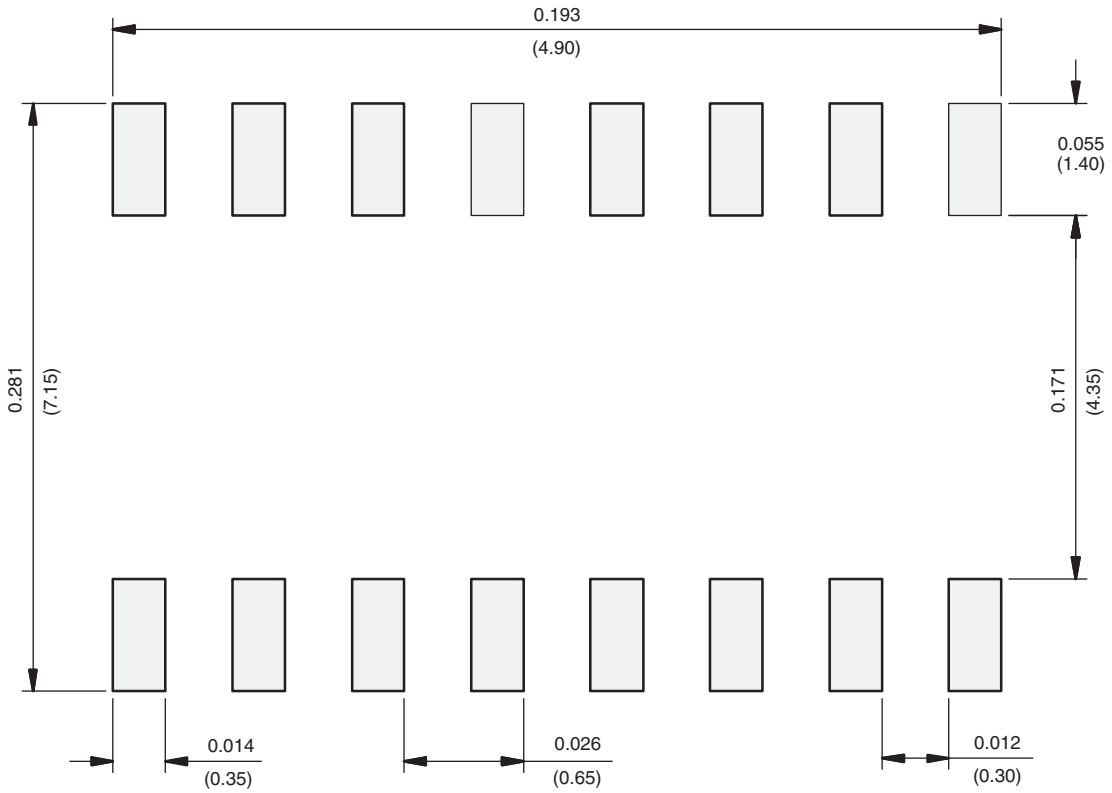



**Fig. 7 - Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain**

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| Part number | DG213 | DG213 | DG213 |
| Status code | 2 | 2 | 2 |
| Configuration | SPST x 4, comp | SPST x 4, comp | SPST x 4, comp |
| Single supply min. (V) | 5 | 5 | 5 |
| Single supply max. (V) | 36 | 36 | 36 |
| Dual supply min. (V) | 5 | 5 | 5 |
| Dual supply max. (V) | 22 | 22 | 22 |
| On-resistance (Ω) | 45 | 45 | 45 |
| Charge injection (pC) | 1 | 1 | 1 |
| Source on capacitance (pF) | - | - | - |
| Source off capacitance (pF) | 5 | 5 | 5 |
| Leakage switch on typ. (nA) | 0.02 | 0.02 | 0.02 |
| Leakage switch off max. (nA) | 0.5 | 0.5 | 0.5 |
| -3 dB bandwidth (MHz) | - | - | - |
| Package | TSSOP-16 | SO-16 (narrow) AS | Plastic DIP-16 |
| Functional circuit / applications | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare |
| Interface | Parallel | Parallel | Parallel |
| Single supply operation | Yes | Yes | Yes |
| Dual supply operation | Yes | Yes | Yes |
| Turn on time max. (ns) | 130 | 130 | 130 |
| Crosstalk and off isolation | -90 | -90 | -90 |

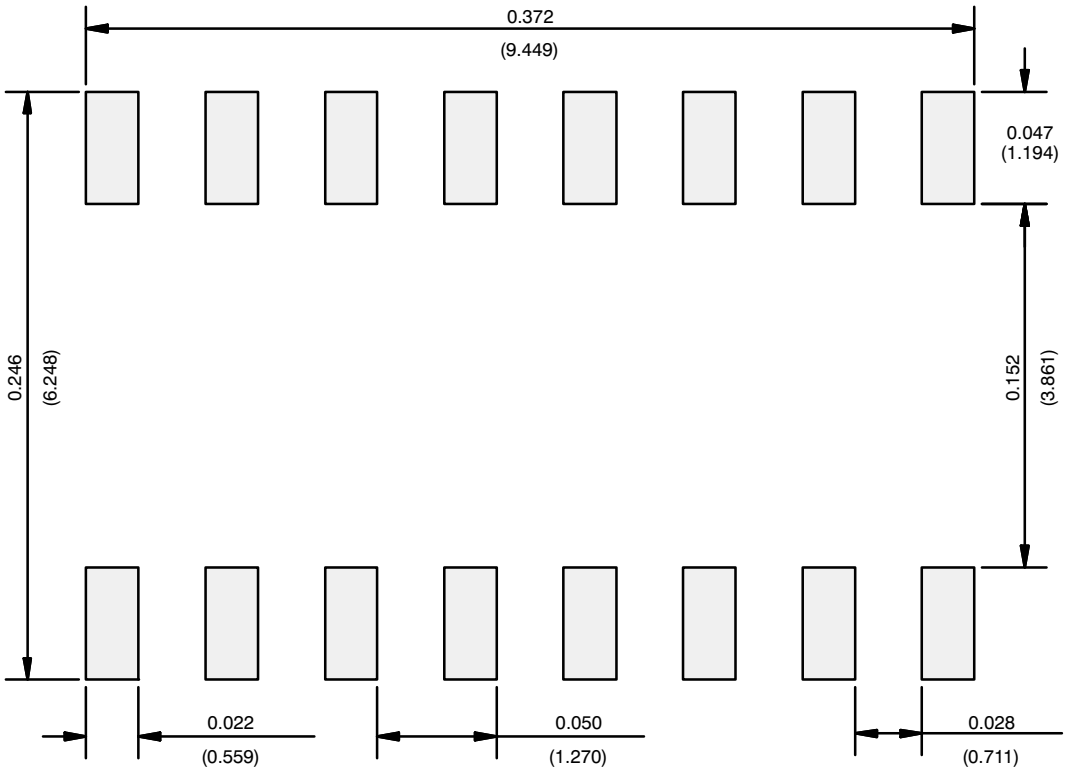
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?61557.*

## RECOMMENDED MINIMUM PAD FOR TSSOP-16




Recommended Minimum Pads
Dimensions in inches (mm)

## RECOMMENDED MINIMUM PADS FOR SO-16




Recommended Minimum Pads
Dimensions in Inches/(mm)

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