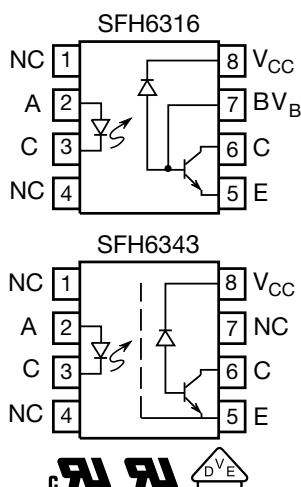
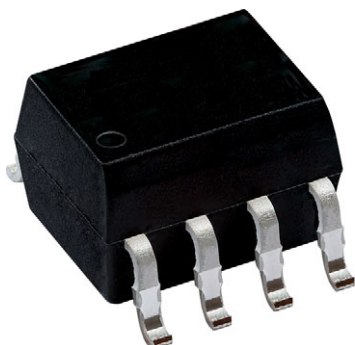


## High Speed Optocoupler, 1 MBd, Transistor Output



### DESCRIPTION

The SFH6316, SFH6343, high speed optocouplers, each consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector and a high speed transistor. The photo detector is junction isolated from the transistor to reduce miller capacitance effects. The open collector output function allows circuit designers to adjust the load conditions when interfacing with different logic systems such as TTL, CMOS, etc.

Because the SFH6343 has a faraday shield on the detector chip, it can also reject and minimize high input to output common mode transient voltages. The SFH6343 provides an isolated base connection to further reduce the potential electrical noise entering the package.

### FEATURES

- Surface mountable
- Compatible with infrared vapor phase reflow and wave soldering processes
- Isolation test voltage, 4000 V<sub>RMS</sub>
- Very high common mode transient immunity: 15 000 V/μs at V<sub>CM</sub> = 1500 V guaranteed (SFH6343)
- High speed: 1 MBd
- Guaranteed AC and DC performance temperature: 0 °C to 70 °C
- Open collector output
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

### APPLICATIONS

- Microprocessor system interface
- Ground loop elimination
- Galvanic noise isolation
- Serial bus systems
- Signal level translation

### AGENCY APPROVALS

- [UL](#)
- [cUL](#)
- [DIN EN 60747-5-5 \(VDE 0884\)](#), available with option 1

### LINKS TO ADDITIONAL RESOURCES



**ORDERING INFORMATION**

<div><div>S</div><div>F</div><div>H</div><div>6</div><div>3</div><div>#</div><div>#</div><div>T</div></div> <div>PART NUMBER</div>									
AGENCY CERTIFIED / PACKAGE			CRT (%)						
UL, cUL			≥ 15				NO BASE CONNECTION		
SOIC-8			SFH6316T				SFH6343T		

**ABSOLUTE MAXIMUM RATINGS** ( $T_{amb} = 25\text{ °C}$ , unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
<b>INPUT</b>				
Reverse voltage		$V_R$	3	V
DC forward current		$I_F$	25	mA
Surge forward current		$I_{FSM}$	1	A
Power dissipation	$T_{amb} \leq 70\text{ °C}$	$P_{diss}$	45	mW
<b>OUTPUT</b>				
Supply voltage		$V_S$	-0.5 to 30	V
Output voltage		$V_O$	-0.5 to 25	V
Output current		$I_O$	8	mA
Power dissipation	$T_{amb} \leq 70\text{ °C}$	$P_{diss}$	100	mW
<b>COUPLER</b>				
Storage temperature range		$T_{stg}$	-55 to +150	°C
Ambient temperature range		$T_{amb}$	-55 to +100	°C
Junction temperature		$T_j$	125	°C
Soldering temperature	Max. 10 s, dip soldering distance to seating plane $\geq 1.5\text{ mm}$		260	°C

**Note**

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

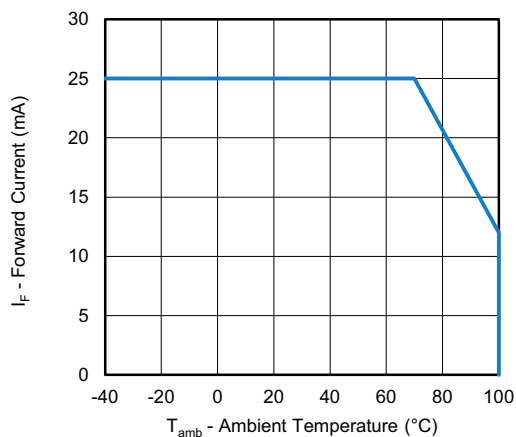


Fig. 1 - Forward Current vs. Ambient Temperature

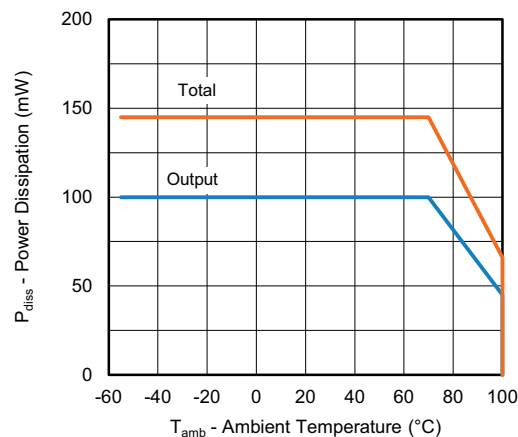


Fig. 2 - Power Dissipation vs. Ambient Temperature



<b>ELECTRICAL CHARACTERISTICS</b> ( $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ ; typical values are at $T_{amb} = 25\text{ }^{\circ}\text{C}$ )							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>INPUT</b>							
Forward voltage	$I_F = 16\text{ mA}^{(1)}$		$V_F$	-	1.3	1.8	V
	$I_F = 16\text{ mA}$		$V_F$	-	1.3	1.9	V
Reverse current	$V_R = 3\text{ V}$		$I_R$	-	0.001	10	$\mu\text{A}$
Capacitance	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		$C_{IN}$	-	24	-	pF
Temperature coefficient of forward voltage	$I_F = 16\text{ mA}$		$\Delta V_F / \Delta T_{amb}$	-	-1.7	-	mW/ $^{\circ}\text{C}$
<b>OUTPUT</b>							
Logic low supply current	$I_F = 16\text{ mA}$ , $V_O = \text{open}$ , $V_{CC} = 15\text{ V}$		$I_{CCL}$	-	215	-	$\mu\text{A}$
Logic high supply current	$I_F = 0\text{ mA}$ , $V_O = \text{open}$ , $V_{CC} = 15\text{ V}^{(1)}$		$I_{CCH}$	-	0.1	1	$\mu\text{A}$
	$I_F = 0\text{ mA}$ , $V_O = \text{open}$ , $V_{CC} = 15\text{ V}$		$I_{CCH}$	-	0.1	2	$\mu\text{A}$
Logic low output voltage	$I_F = 16\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ , $I_O = 3\text{ mA}^{(1)}$	SFH6316	$V_{OL}$	-	0.25	0.4	V
	$I_F = 16\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ , $I_O = 2.4\text{ mA}$		$V_{OL}$	-	0.22	0.5	V
	$I_F = 16\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ , $I_O = 3\text{ mA}^{(1)}$	SFH6343	$V_{OL}$	-	0.25	0.4	V
	$I_F = 16\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ , $I_O = 2.4\text{ mA}$		$V_{OL}$	-	0.22	0.5	V
Logic high output current	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 5.5\text{ V}^{(1)}$		$I_{OH}$	-	0.003	0.5	$\mu\text{A}$
	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 15\text{ V}^{(1)}$		$I_{OH}$	-	0.01	1	$\mu\text{A}$
	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 15\text{ V}$		$I_{OH}$	-	-	50	$\mu\text{A}$
<b>COUPLER</b>							
Capacitance (input to output) <sup>(2)</sup>	$f = 1\text{ MHz}$		$C_{IO}$	-	0.4	-	pF

**Notes**

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

<sup>(1)</sup>  $T_{amb} = 25\text{ }^{\circ}\text{C}$

<sup>(2)</sup> A 0.1  $\mu\text{F}$  bypass capacitor connected between pins 5 and 8 is recommended

<b>CURRENT TRANSFER RATIO</b> ( $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ ; typical values are at $T_{amb} = 25\text{ }^{\circ}\text{C}$ )							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Current transfer ratio	$I_F = 16\text{ mA}$ , $V_O = 0.4\text{ V}$ , $V_{CC} = 4.5\text{ V}^{(1)}$	SFH6316	CTR	19	28	50	%
	$I_F = 16\text{ mA}$ , $V_O = 0.5\text{ V}$ , $V_{CC} = 4.5\text{ V}$		CTR	15	29	-	%
	$I_F = 16\text{ mA}$ , $V_O = 0.4\text{ V}$ , $V_{CC} = 4.5\text{ V}^{(1)}$	SFH6343	CTR	19	28	50	%
	$I_F = 16\text{ mA}$ , $V_O = 0.5\text{ V}$ , $V_{CC} = 4.5\text{ V}$		CTR	15	29	-	%

**Notes**

- Current transfer ratio in percent equals the ratio of output collector current ( $I_O$ ) to the forward LED input current ( $I_F$ ) times 100. A 0.1  $\mu\text{F}$  bypass capacitor connected between pins 5 and 8 is recommended.

<sup>(1)</sup>  $T_{amb} = 25\text{ }^{\circ}\text{C}$

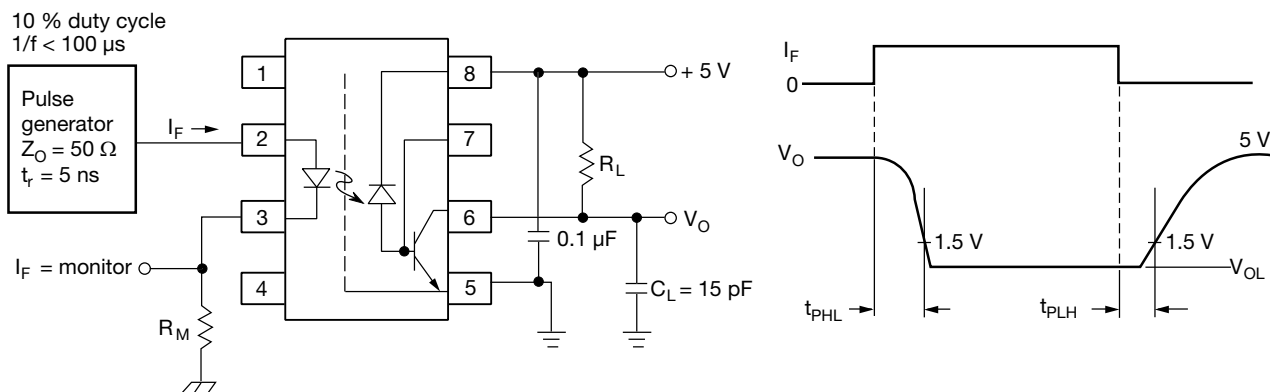


Fig. 3 - Test Circuit for Switching Times

**SWITCHING CHARACTERISTICS**

( $T_{amb} = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5$  V,  $I_F = 16$  mA; typical values are at  $T_{amb} = 25^\circ\text{C}$ )

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low at output (see Fig. 1)	$R_L = 1.9$ k $\Omega$	$t_{PHL}^{(1)}$	-	0.6	0.8	$\mu$ s
		$t_{PHL}$	-	0.6	1.0	$\mu$ s
Propagation delay time to logic high at output (see Fig. 1)	$R_L = 1.9$ k $\Omega$	$t_{PLH}^{(1)}$	-	0.3	0.8	$\mu$ s
		$t_{PLH}$	-	0.3	1.0	$\mu$ s

**Notes**

- The 1.9 k $\Omega$  load represents 1 TTL unit load of 1.6 mA and the 5.6 k $\Omega$  pull-up resistor.
- The 4.1 k $\Omega$  load represents 1 LSTTL unit load of 0.36 mA and the 6.1 k $\Omega$  pull-up resistor.
- (1)  $T_{amb} = 25^\circ\text{C}$

**COMMON MODE TRANSIENT IMMUNITY ( $T_{amb} = 25^\circ\text{C}$ )**

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Common mode transient immunity at logic high level output (see Fig. 2)	$R_L = 1.9$ k $\Omega$ , $I_F = 0$ mA, $V_{CM} = 10$ V <sub>PP</sub>	SFH6316	$ CM_H $	-	1000	-	V/ $\mu$ s
	$R_L = 1.9$ k $\Omega$ , $I_F = 0$ mA, $V_{CM} = 1500$ V <sub>PP</sub>	SFH6343	$ CM_H $	15 000	30 000	-	V/ $\mu$ s
Common mode transient immunity at logic low level output (see Fig. 2)	$R_L = 1.9$ k $\Omega$ , $I_F = 0$ mA, $V_{CM} = 10$ V <sub>PP</sub>	SFH6316	$ CM_L $	-	1000	-	V/ $\mu$ s
	$R_L = 1.9$ k $\Omega$ , $I_F = 0$ mA, $V_{CM} = 1500$ V <sub>PP</sub>	SFH6343	$ CM_L $	15 000	30 000	-	V/ $\mu$ s

**Note**

- Common mode transient immunity in a logic high level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse ( $V_{CM}$ ) to assure that the output will remain in a logic high state (i.e.,  $V_O > 2$  V). Common mode transient immunity in a logic low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse signal ( $V_{CM}$ ) to assure that the output will remain in logic low state, i.e.,  $V_O < 0.8$  V).
- The 1.9 k $\Omega$  load represents 1 TTL unit load of 1.6 mA and the 5.6 k $\Omega$  pull-up resistor.
- The 4.1 k $\Omega$  load represents 1 LSTTL unit load of 0.36 mA and the 6.1 k $\Omega$  pull-up resistor.

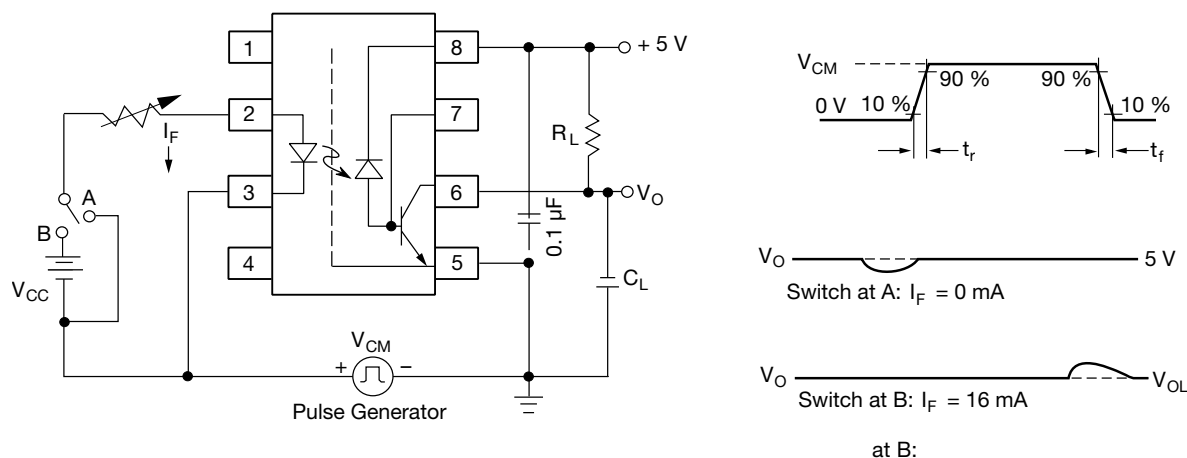


Fig. 4 - Test Circuit for Transient Immunity and Typical Waveforms

SAFETY AND INSULATION RATINGS (T <sub>amb</sub> = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		55 / 100 / 21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, t = 1 min	V <sub>ISO</sub>	4000	V <sub>RMS</sub>
Maximum transient isolation voltage	According to DIN EN 60747-5-5	V <sub>IOTM</sub>	6000	V <sub>peak</sub>
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	V <sub>IORM</sub>	560	V <sub>peak</sub>
Isolation resistance	T <sub>amb</sub> = 25 °C, V <sub>IO</sub> = 500 V	R <sub>IO</sub>	≥ 10 <sup>12</sup>	Ω
	T <sub>amb</sub> = 100 °C, V <sub>IO</sub> = 500 V	R <sub>IO</sub>	≥ 10 <sup>11</sup>	Ω
Output safety power		P <sub>SO</sub>	350	mW
Input safety current		I <sub>SI</sub>	150	mA
Safety temperature		T <sub>S</sub>	165	°C
Creepage distance	SOIC-8		≥ 4	mm
Clearance distance			≥ 4	mm
Insulation thickness		DTI	≥ 0.2	mm

### Note

- As per IEC 60747-5-5, §7.4.3.8.1, this optocoupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits.
- <sup>(1)</sup> Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

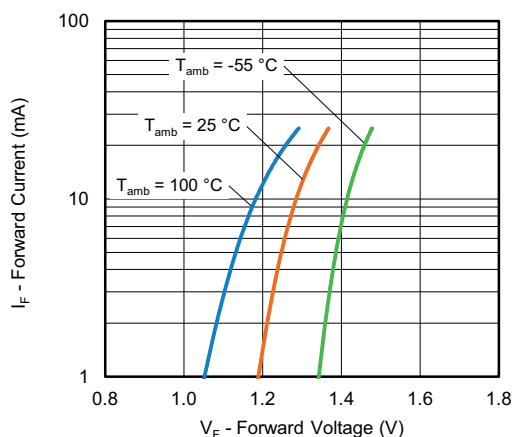
**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


Fig. 5 - Forward Current vs. Forward Voltage

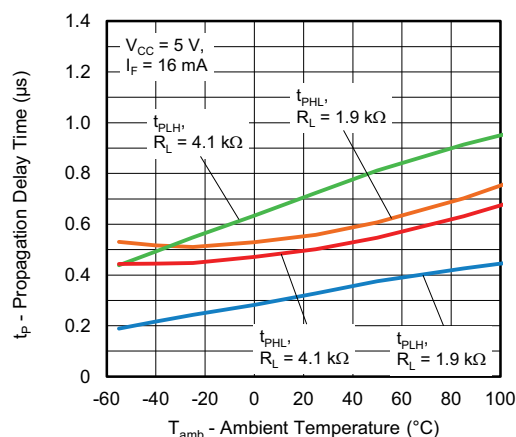


Fig. 8 - Propagation Delay Time vs. Ambient Temperature

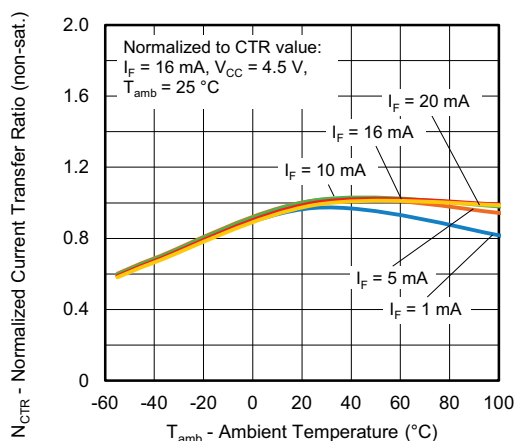


Fig. 6 - Normalized Current Transfer Ratio (non-saturated) vs. Ambient Temperature

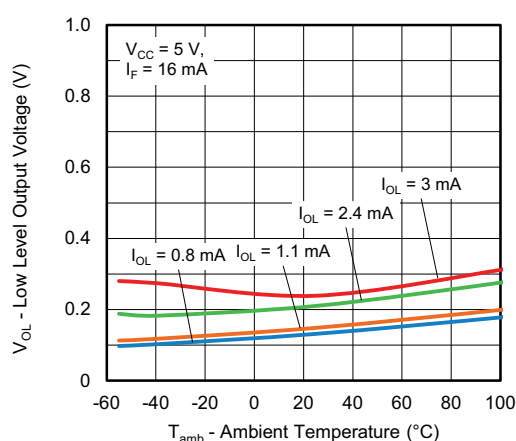


Fig. 9 - Low Level Output Voltage vs. Ambient Temperature

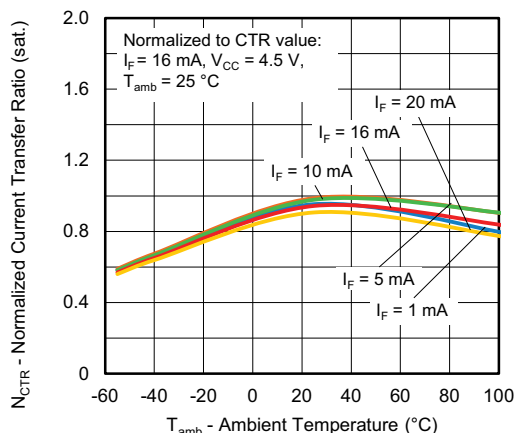


Fig. 7 - Normalized Current Transfer Ratio (saturated) vs. Ambient Temperature

**PACKAGE DIMENSIONS** (in millimeters)

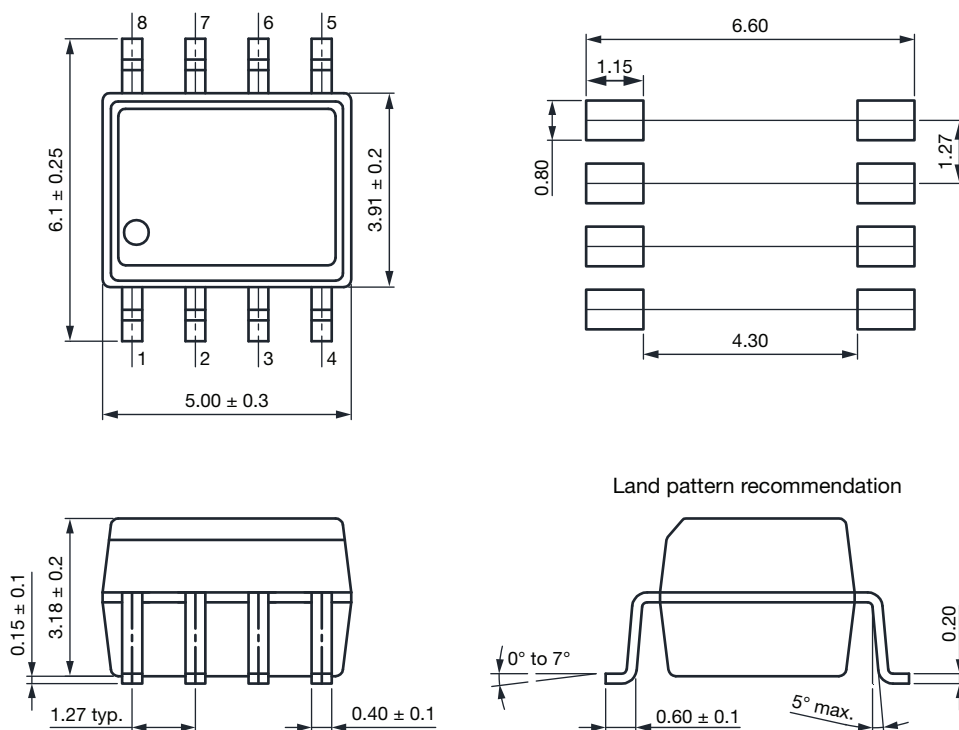
**SOIC-8**


Fig. 10

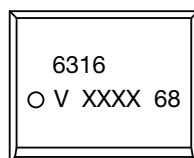
**PACKAGE MARKING**


Fig. 11 - Example of SFH6316T

**Notes**

- XXXX = LMC (lot marking code)
- Tape and reel suffix (T) is not part of the package marking

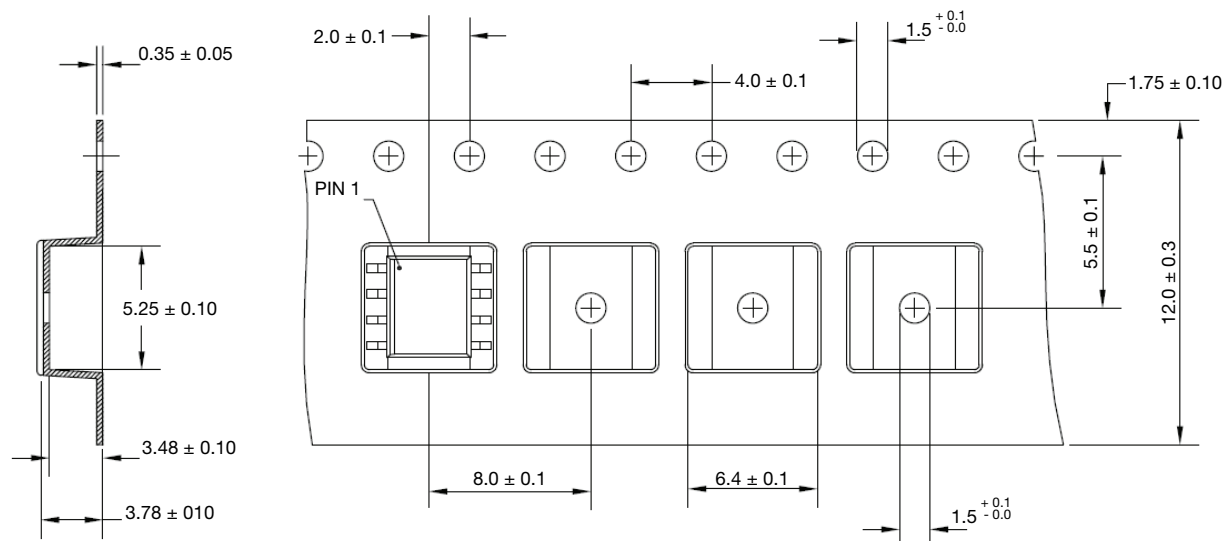
**PACKAGING INFORMATION** (in millimeters)


Fig. 12 - Tape and Reel Packaging (2000 pieces on reel)

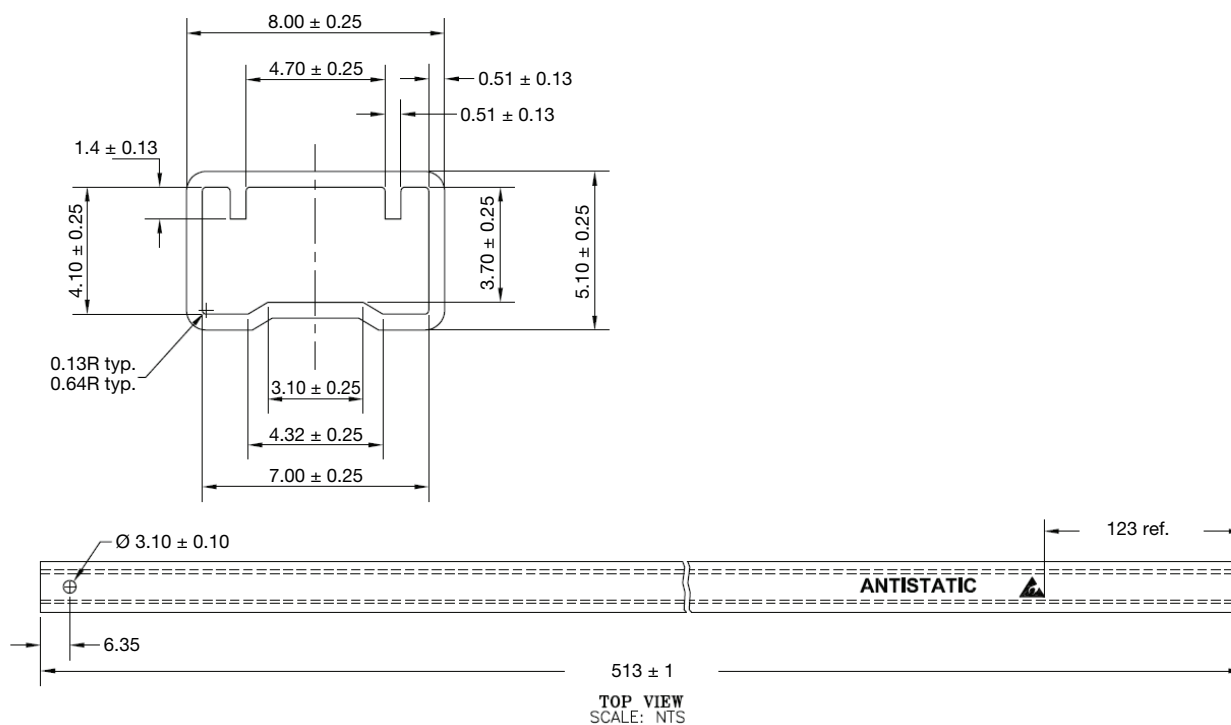


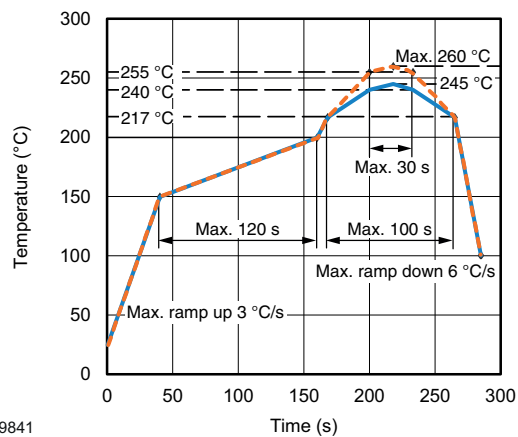
Fig. 13 - Tupe Packing

DEVICE PER TUBE			
TYPE	UNITS/TUBE	TUBES/BOX	UNITS/BOX
SOIC-8	100	30	3000





## SOLDER PROFILES



19841

Fig. 14

## HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 1C

Floor life: unlimited

Conditions:  $T_{amb} < 30\text{ °C}$ , RH < 85 %

Moisture sensitivity level 1, according to J-STD-020



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