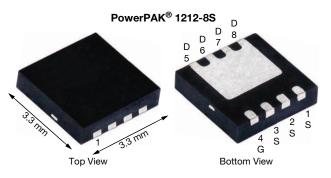
SiSS63DN

www.vishay.com

Vishay Siliconix

P-Channel 20 V (D-S) MOSFET



PRODUCT SUMMARY	
V _{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0027
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.0036
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	0.0070
Q _g typ. (nC)	72.2
I _D (A)	-127.5
Configuration	Single

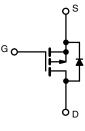
FEATURES

TrenchFET[®] Gen III p-channel power MOSFET

- Leadership R_{DS(on)} in compact and thermally enhanced package
- 100 % R_q and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Battery management
- · Load switch



RoHS

COMPLIANT HALOGEN

FREE

P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS63DN-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	-20	V	
Gate-source voltage		V _{GS}	± 12	V	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		-127.5		
	T _C = 70 °C	1 . F	-102		
	T _A = 25 °C		-35.1 ^{b, c}		
	T _A = 70 °C	1 1	-28.1		
Pulsed drain current (t = 100 µs)		I _{DM}	-200	— A	
Continuous source-drain diode current	T _C = 25 °C		-54.8		
	T _A = 25 °C	I _S	-4.2 ^{b, c}		
Single pulse avalanche current L = 0.1 mH		I _{AS}	-25		
Single pulse avalanche energy		E _{AS}	31.2	mJ	
	T _C = 25 °C		65.8		
Maximum power dissipation	T _C = 70 °C		42.1	14/	
	T _A = 25 °C	P _D	5 b, c	W	
	T _A = 70 °C	1 [3.2 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^c		1	260		

THERMAL RESISTANCE RATING	GS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.5	1.9	0/10

Notes a. $T_C = 25 \ ^{\circ}C$

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection d.

Rework conditions: manual soldering with a soldering iron is not recommended for leadless components e.

f. Maximum under steady state conditions is 65 °C/W

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For technical questions, contact: pmostechsupport@vishay.com

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	•				•	
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = -250 \mu\text{A}$	-20	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = -10 mA	-	-15	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	4	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	-0.5	-	-1.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$	-	-	100	nA
Zara gata valtaga drain aurrent		$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	-1	
Zero gate voltage drain current	I _{DSS}	$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 70 ^{\circ}\text{C}$	-	-	-15	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge$ -10 V, V_{GS} = -10 V	-20	-	-	Α
		V _{GS} = -10 V, I _D = -15 A	-	0.0022	0.0027	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -10 A	-	0.0030	0.0036	Ω
		V _{GS} = -2.5 V, I _D = -5 A	-	0.0053	0.0070	
Forward transconductance ^a	g fs	V _{DS} = -10 V, I _D = -15 A	-	75	-	S
Dynamic ^b						
Input capacitance	C _{iss}		-	7080	-	
Output capacitance	C _{oss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	-	1000	-	pF
Reverse transfer capacitance	C _{rss}			1110	-	
Total acta charge	0	V_{DS} = -10 V, V_{GS} = -8 V, I_D = -35.1 A	-	157.2	236	
Total gate charge	Qg		-	72.2	110	nC
Gate-source charge	Q _{gs}	V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -35.1 A	-	17.7	-	no
Gate-drain charge	Q _{gd}		-	22	-	
Gate resistance	Rg	f = 1 MHz	0.3	1.5	3	Ω
Turn-on delay time	t _{d(on)}		-	20	40	
Rise time	t _r	V_{DD} = -10 V, R_L = 0.36 Ω , $I_D \cong$ -28.1 A,	-	28	56	
Turn-off delay time	t _{d(off)}	V_{GEN} = -10 V, R_g = 1 Ω	-	80	160	
Fall time	t _f		-	25	50	ns
Turn-on delay time	t _{d(on)}		-	40	80	115
Rise time	tr	V_{DD} = -10 V, R _L = 0.36 Ω, I _D ≅ -28.1 A,	-	60	120	
Turn-off delay time	t _{d(off)}	V_{GEN} = -4.5 V, R_{g} = 1 Ω	-	100	200	
Fall time	t _f		-	70	140	
Drain-Source Body Diode Characteristi	cs					
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-54.8	•
Pulse diode forward current	I _{SM}		-	-	-200	A
Body diode voltage	V _{SD}	$I_{\rm S} = -5$ A, $V_{\rm GS} = 0$ V	-	-0.66	-1.2	V
Body diode reverse recovery time	t _{rr}		-	20	40	ns
Body diode reverse recovery charge	Q _{rr}	I _F = -28.1 A, di/dt = 100 A/μs,	-	9.5	19	nC
Reverse recovery fall time	ta	$T_{\rm J} = 25 ^{\circ}{\rm C}$	-	11.5	-	
Reverse recovery rise time	t _b		-	8.5	- 1	ns

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

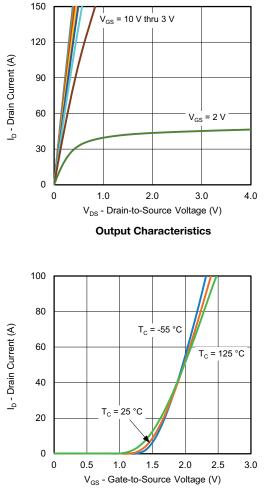
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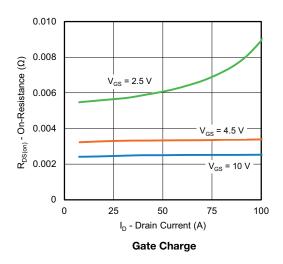
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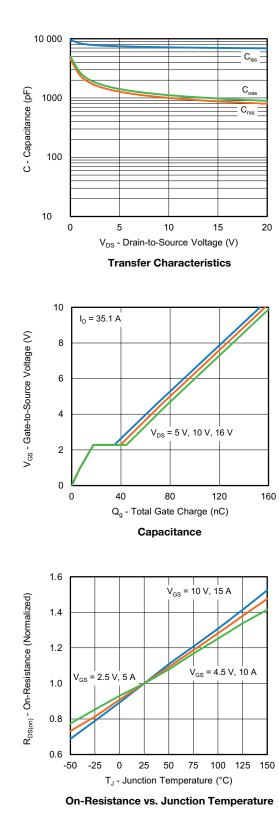
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



On-Resistance vs. Drain Current and Gate Voltage



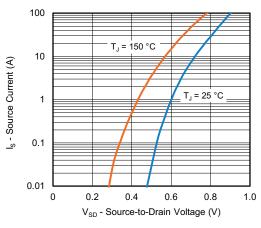


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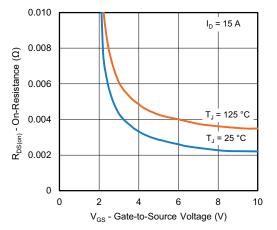
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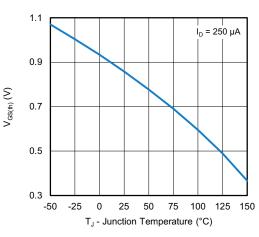
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



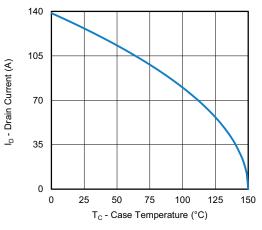
Source-Drain Diode Forward Voltage



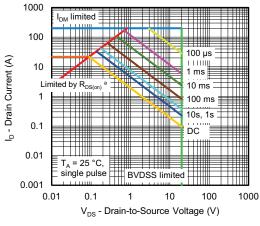
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

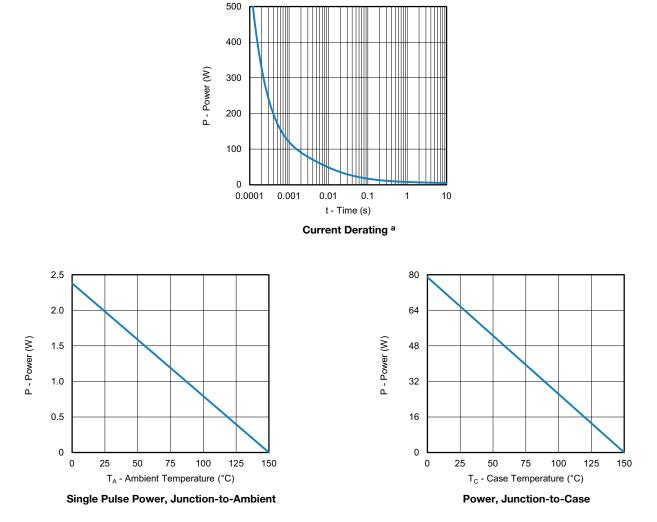
Note a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

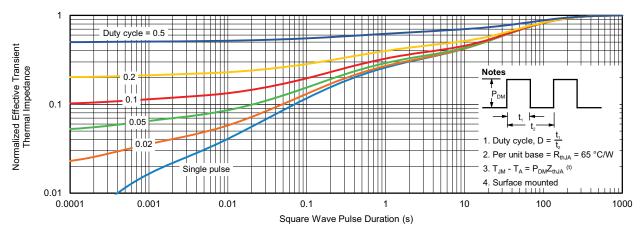


Note

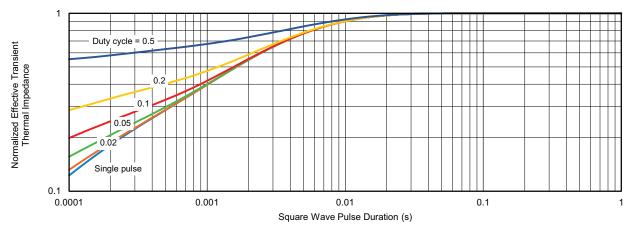
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Case Outline for PowerPAK[®] 1212-8S







DIM		MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	MIN. NOM.		
А	0.67	0.75	0.83	0.026	0.030	0.033	
A1	0.00	-	0.05	0.000	-	0.002	
A3		0.20 ref.		0.008 ref			
b	0.25	0.30	0.35	0.010	0.012	0.014	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	2.15	2.25	2.35	0.085	0.089	0.093	
E	3.20	3.30	3.40	0.126	0.130	0.134	
E1	1.60	1.70	1.80	0.063	0.067	0.071	
е		0.65 bsc.			0.026 bsc.		
К		0.76 ref.			0.030 ref.		
K1		0.41 ref.		0.016 ref.			
L	0.33	0.43	0.53	0.013	0.017	0.021	
Z	0.525 ref.			0.021 ref.			
N: C20-0862-Re /G: 6008	v. B, 20-Jul-2020			•			

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