Improved Quad SPST CMOS Analog Switches

DESCRIPTION

The DG441B, DG442B are monolithic quad analog switches designed to provide high speed, low error switching of analog and audio signals. The DG441B, DG442B are upgrades to the original DG441, DG442. Combing low on-resistance (45 Ω, typ.) with high speed (t_{on} 120 ns, typ.), the DG441B, DG442B are ideally suited for data acquisition, communication systems, automatic test equipment, or medical instrumentation. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

The DG441B, DG442B are built using Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

When on, each switch conducts equally well in both directions and blocks input voltages to the supply levels when off.

BENEFITS

- Less signal errors and distortion
- Reduced power supply requirements
- Faster throughput
- Reduced pedestal errors
- Simple interfacing

FEATURES

- Low on-resistance: 45 Ω
- Low power consumption: 1 mW
- Fast switching action - t_{on}: 120 ns
- Low charge injection - Q: -1 pC
- TTL/CMOS-compatible logic
- Single supply capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

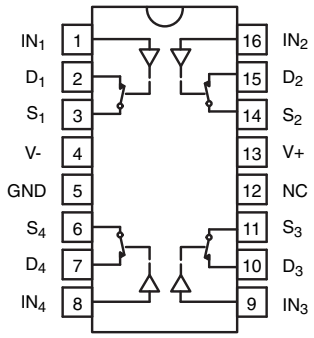
- Audio switching
- Data acquisition
- Sample-and-hold circuits
- Communication systems
- Automatic test equipment
- Medical instruments

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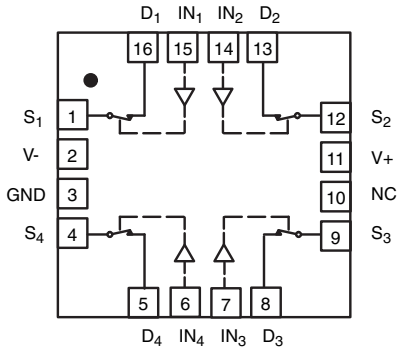
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG441B
Dual-In-Line and SOIC



Top View

DG441B
QFN16 (4 x 4 mm)



Top View

TRUTH TABLE		
LOGIC	**DG441B**	**DG442B**
0	On	Off
1	Off	On

Note

- Logic "0" ≤ 0.8 V
  Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
TEMP. RANGE	**PACKAGE**	**PART NUMBER**
-40 °C to +85 °C	16-pin plastic DIP	DG441BDJ-E3
		DG442BDJ-E3
	16-pin narrow SOIC	DG441BDY-E3
		DG441BDY-T1-E3
		DG442BDY-E3
		DG442BDY-T1-E3
	16 pin QFN 4 x 4 mm (variation 1)	DG441BDN-T1-E4
		DG442BDN-T1-E4

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
PARAMETER		**LIMIT**	**UNIT**
V+ to V-		44	V
GND to V-		25	
Digital inputs [a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous current (any terminal)		30	mA
Current (S or D) pulsed at 1 ms, 10 % duty cycle		100	
Storage temperature		-65 to +125	°C
Power dissipation (package) [b]	16-pin plastic DIP [c]	470	mW
	16-pin narrow body SOIC [d]	900	
	QFN-16 [d]	850	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 6 mW/°C above 75 °C
d. Derate 12 mW/°C above 75 °C

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SPECIFICATIONS [a] (for dual supplies)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V+ = 15 V, V- = -15 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [e]	TEMP. [b]	D SUFFIX -40 °C TO +85 °C			UNIT
				MIN. [d]	TYP. [c]	MAX. [d]	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	-15	-	15	V
Drain-source on-resistance	R_{ON}	I_S = 1 mA, V_D = ± 10 V	Room	-	45	80	Ω
			Full	-	-	95	
On-resistance match between channels [e]	$\Delta R_{DS(on)}$	I_S = 1 mA, V_D = ± 10 V	Room	-	2	4	
			Full	-	-	5	
Switch off leakage current	$I_{S(off)}$	V_D = ± 14 V, V_S = ± 14 V	Room	-0.5	± 0.01	0.5	nA
			Full	-5	-	5	
	$I_{D(off)}$		Room	-0.5	± 0.01	0.5	
			Full	-5	-	5	
Channel on leakage current	$I_{D(on)}$	V_S = V_D = ± 14 V	Room	-0.5	± 0.02	0.5	
			Full	-10	-	10	
Digital Control							
Input voltage low	V_{INL}		Full	-	-	0.8	V
Input voltage high	V_{INH}		Full	2.4	-	-	
Input current V_{IN} low	I_{INL}	V_{IN} under test = 0.8 V, all other = 2.4 V	Full	-1	-0.01	1	µA
Input current V_{IN} high	I_{INH}	V_{IN} under test = 2.4 V, all other = 0.8 V	Full	-1	0.01	1	
Dynamic Characteristics							
Turn-on time	t_{on}	R_L = 1 kΩ, C_L = 35 pF, V_S = 10 V, see Fig. 2	Room	-	120	220	ns
Turn-off time	t_{off}		Room	-	65	120	
Charge injection [e]	Q	C_L = 1 nF, V_S = 0 V, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-	-1	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 15 pF, V_S = 1 V_{RMS}, f = 100 kHz	Room	-	-90	-	dB
Crosstalk (channel-to-channel)	X_{TALK}		Room	-	-95	-	
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	-	4	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	-	4	-	
Channel on capacitance [e]	$C_{D(on)}$	V_S = V_D = 0 V, f = 1 MHz	Room	-	16	-	
Power Supplies							
Positive supply current	I+	V+ = 16.5 V, V- = -16.5 V, V_{IN} = 0 V or 5 V	Room	-	-	1	µA
			Full	-	-	5	
Negative supply current	I-		Room	-1	-	-	
			Full	-5	-	-	

SPECIFICATIONS (for single supplies)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V+ = 12 V, V- = 0 V, V_{IN} = 2.4 V, 0.8 V [e]	TEMP. [b]	D SUFFIX -40 °C TO +85 °C			UNIT
				MIN. [d]	TYP. [c]	MAX. [d]	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	0	-	12	V
Drain-source on-resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = 3 V, 8 V	Room	-	90	160	Ω
			Full	-	-	200	
Dynamic Characteristics							
Turn-on time	t_{on}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V, see Fig, 2	Room	-	120	300	ns
Turn-off time	t_{off}		Room	-	60	200	
Charge injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	-	4	-	pC

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SPECIFICATIONS (for single supplies)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS SPECIFIED V+ = 12 V, V- = 0 V, V_{IN} = 2.4 V, 0.8 V [e]**	**TEMP. [b]**	**D SUFFIX -40 °C TO +85 °C**			**UNIT**
				MIN. [d]	**TYP. [c]**	**MAX. [d]**	
Power Supplies							
Positive supply current	I+	V_{IN} = 0 V or 5 V	Room	-	-	1	µA
			Full	-	-	5	
Negative supply current	I-		Room	-1	-	-	
			Full	-5	-	-	

Notes

a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = input voltage to perform proper function

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM (typical channel)

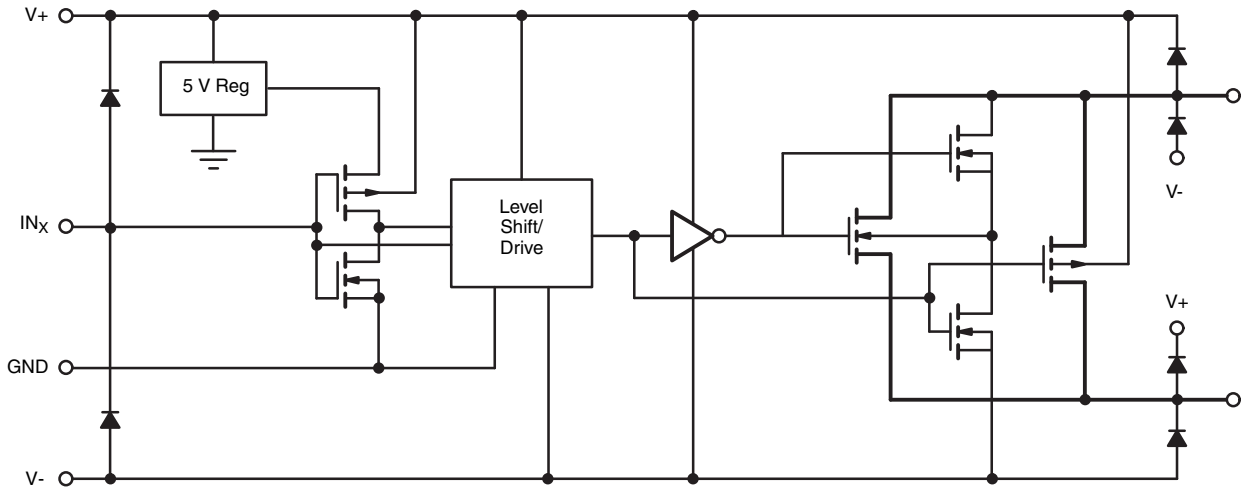
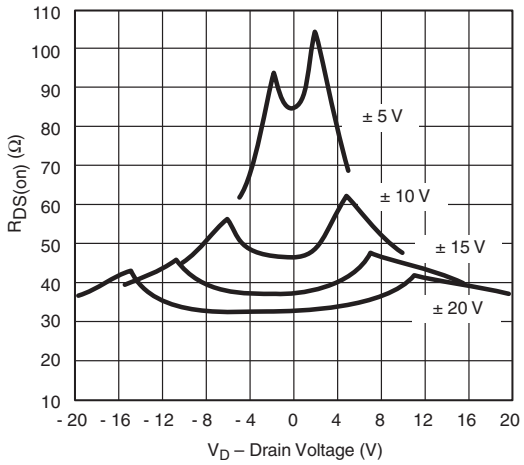


Fig. 1

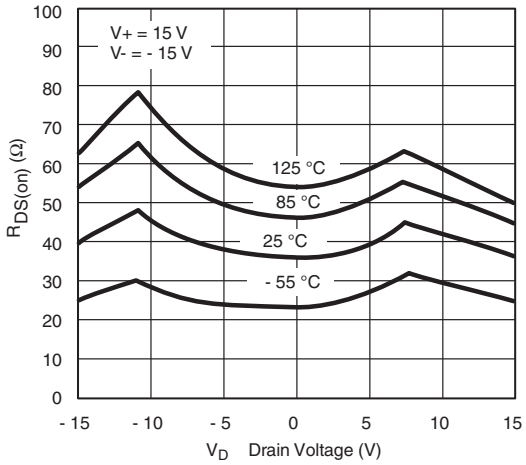
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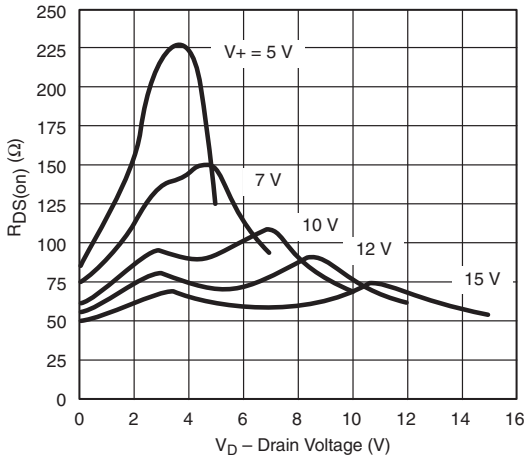
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



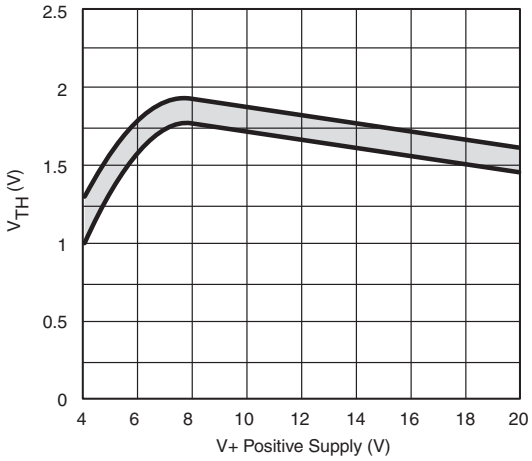
$R_{DS(on)}$ vs. V_D and Power Supply Voltages



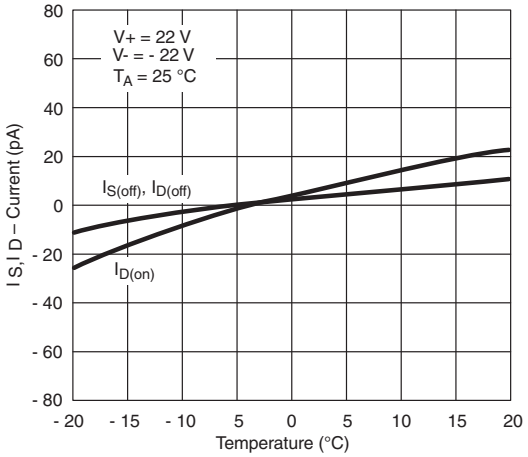
$R_{DS(on)}$ vs. V_D and Temperature



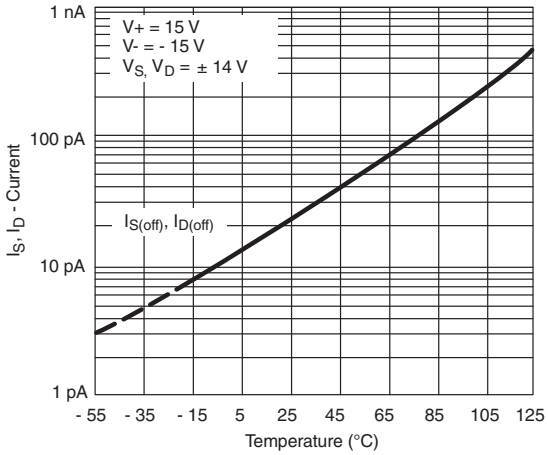
$R_{DS(on)}$ vs. V_D and Single Power Supply Voltages



Input Switching Threshold vs. Supply Voltage



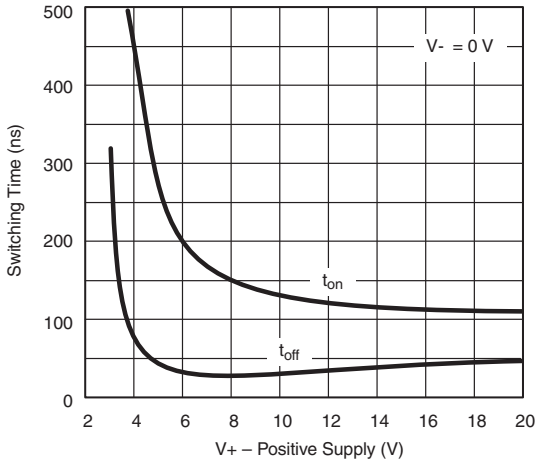
Leakage Currents vs. Analog Voltage



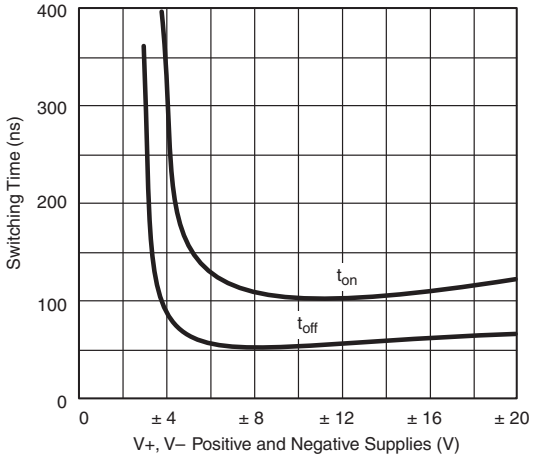
Leakage Currents vs. Temperature

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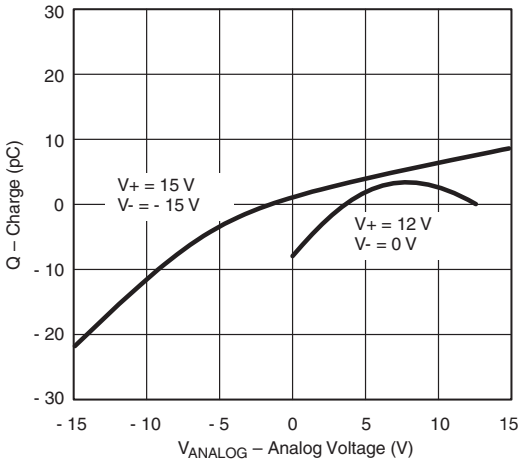
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



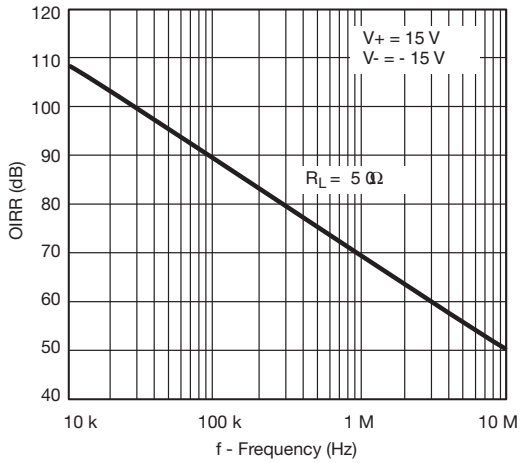
Switching Time vs. Single Supply Voltage



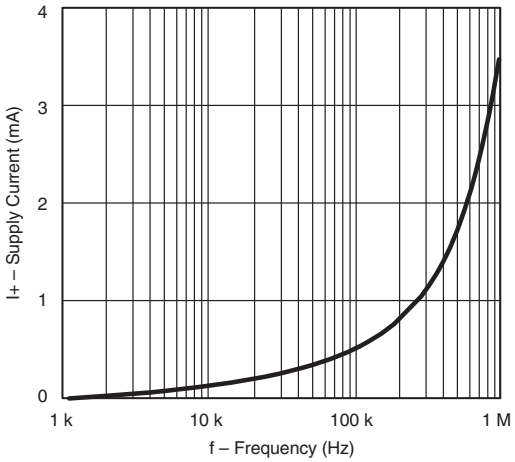
Switching Times vs. Power Supply Voltage



Q_S, Q_D - Charge Injection vs. Analog Voltage



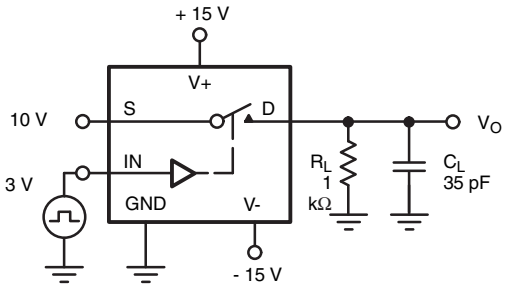
Off Isolation vs. Frequency



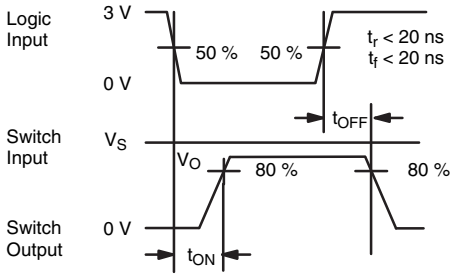
Supply Current vs. Switching Frequency

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TEST CIRCUITS

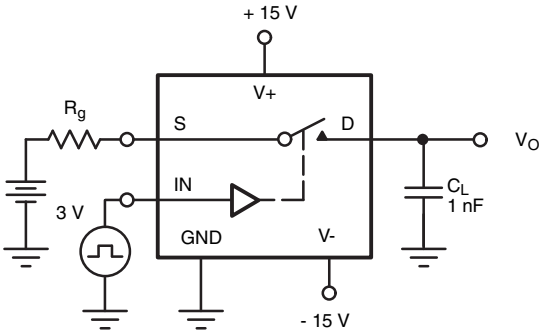


C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

Fig. 2 - Switching Time



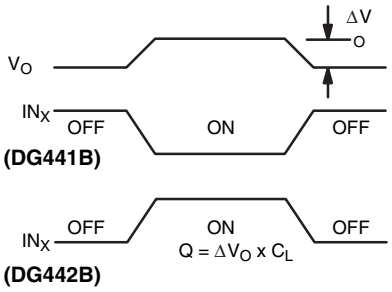
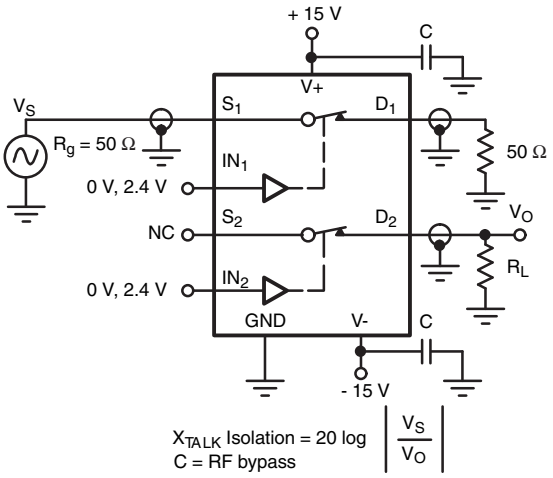


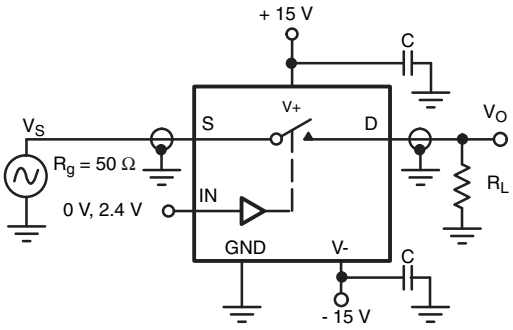
Fig. 3 - Charge Injection

C = 1 mF tantalum in parallel with 0.01 mF ceramic



X_{TALK} Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$
C = RF bypass

Fig. 4 - Crosstalk



Off Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

Fig. 5 - Off Isolation

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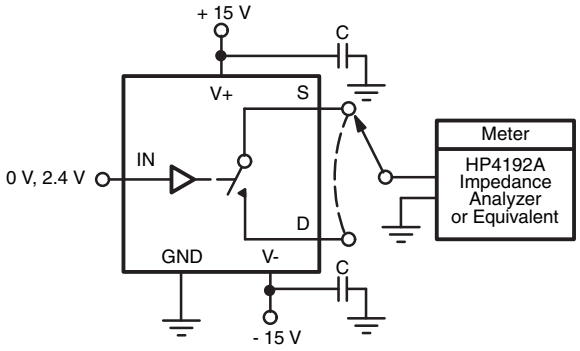


Fig. 6 - Source/Drain Capacitances

APPLICATIONS

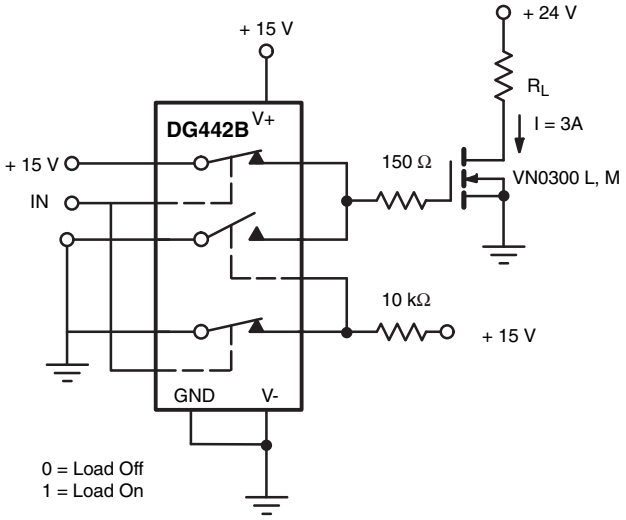


Fig. 7 - Power MOSFET Driver

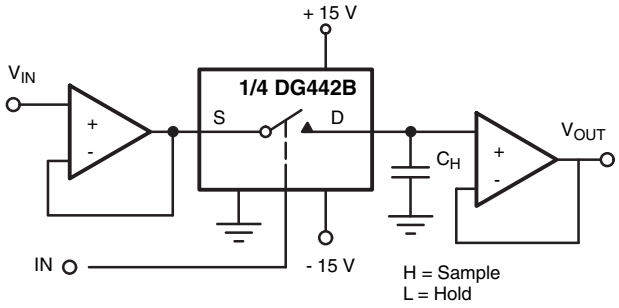


Fig. 8 - Open Loop Sample-and-Hold

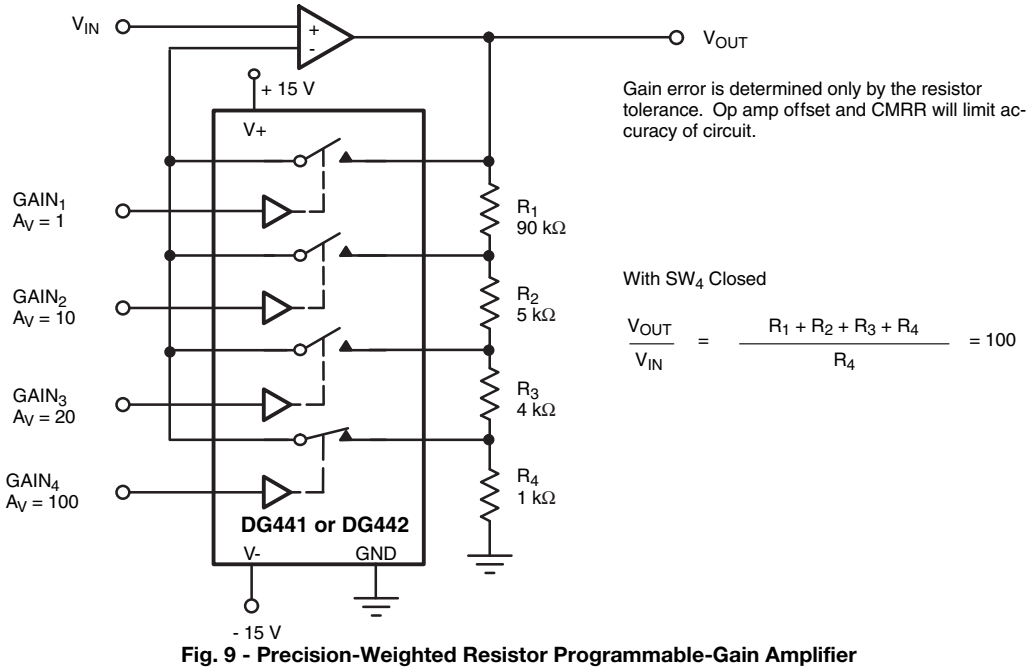


Fig. 9 - Precision-Weighted Resistor Programmable-Gain Amplifier

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PRODUCT SUMMARY						
Part number	DG441B	DG441B	DG441B	DG442B	DG442B	DG442B
Status code	2	2	2	2	2	2
Configuration	SPST x 4, NC	SPST x 4, NC	SPST x 4, NC	SPST x 4, NO	SPST x 4, NO	SPST x 4, NO
Single supply min. (V)	5	5	5	5	5	5
Single supply max. (V)	36	36	36	36	36	36
Dual supply min. (V)	5	5	5	5	5	5
Dual supply max. (V)	22	22	22	22	22	22
On-resistance (Ω)	45	45	45	45	45	45
Charge injection (pC)	-1	-1	-1	-1	-1	-1
Source on capacitance (pF)	16	16	16	16	16	16
Source off capacitance (pF)	4	4	4	4	4	4
Leakage switch on typ. (nA)	0.02	0.02	0.02	0.02	0.02	0.02
Leakage switch off max. (nA)	0.5	0.5	0.5	0.5	0.5	0.5
-3 dB bandwidth (MHz)	-	-	-	-	-	-
Package	Plastic DIP-16	QFN-16 4 x 4	SO-16 (narrow) AS	Plastic DIP-16	QFN-16 4 x 4	SO-16 (narrow) AS
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Turn on time max. (ns)	220	220	220	220	220	220
Crosstalk and off isolation	-95	-95	-95	-95	-95	-95

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72625.

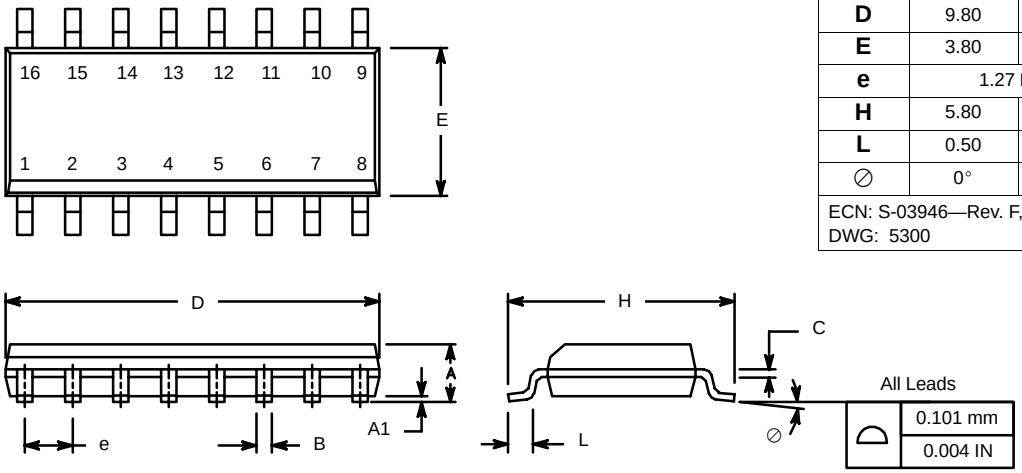
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SOIC (NARROW): 16-LEAD

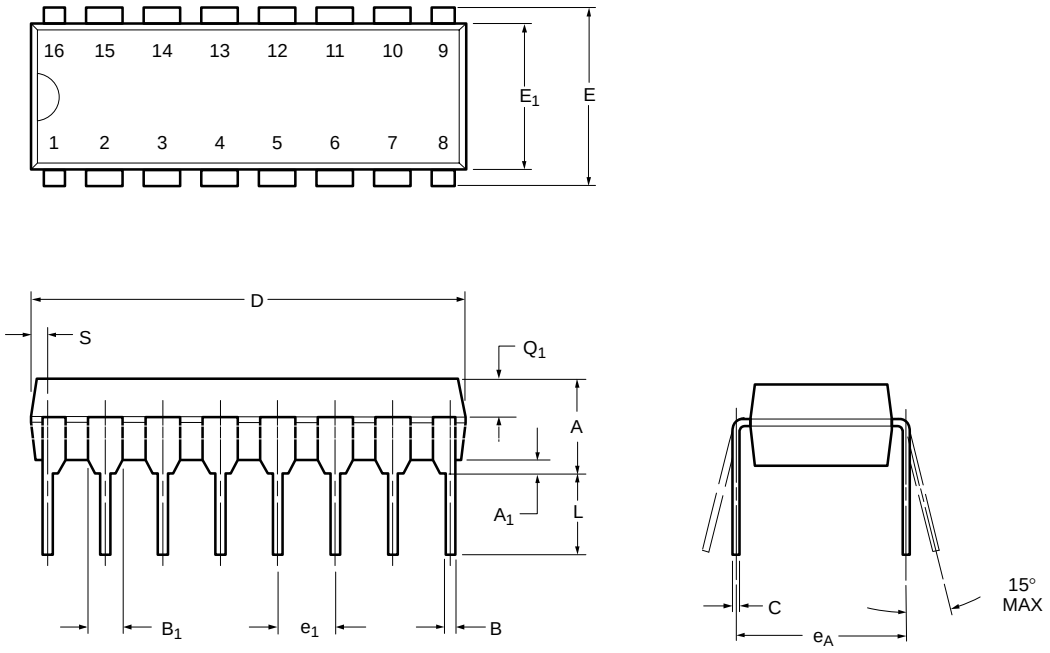
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

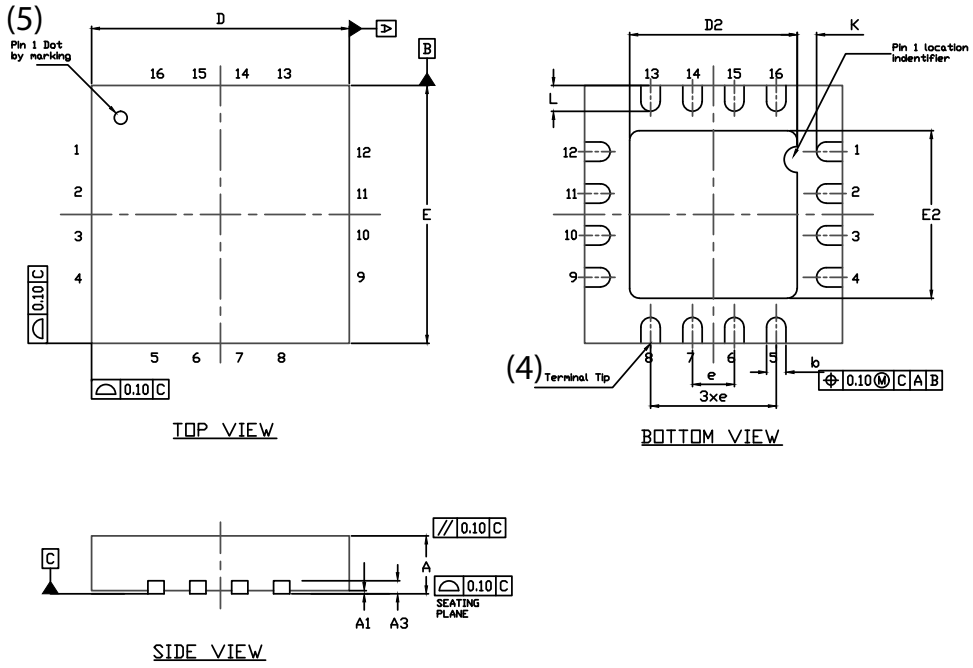


PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS[1]			INCHES			MILLIMETERS[1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N[3]	16			16			16			16		
Nd[3]	4			4			4			4		
Ne[3]	4			4			4			4		

Notes

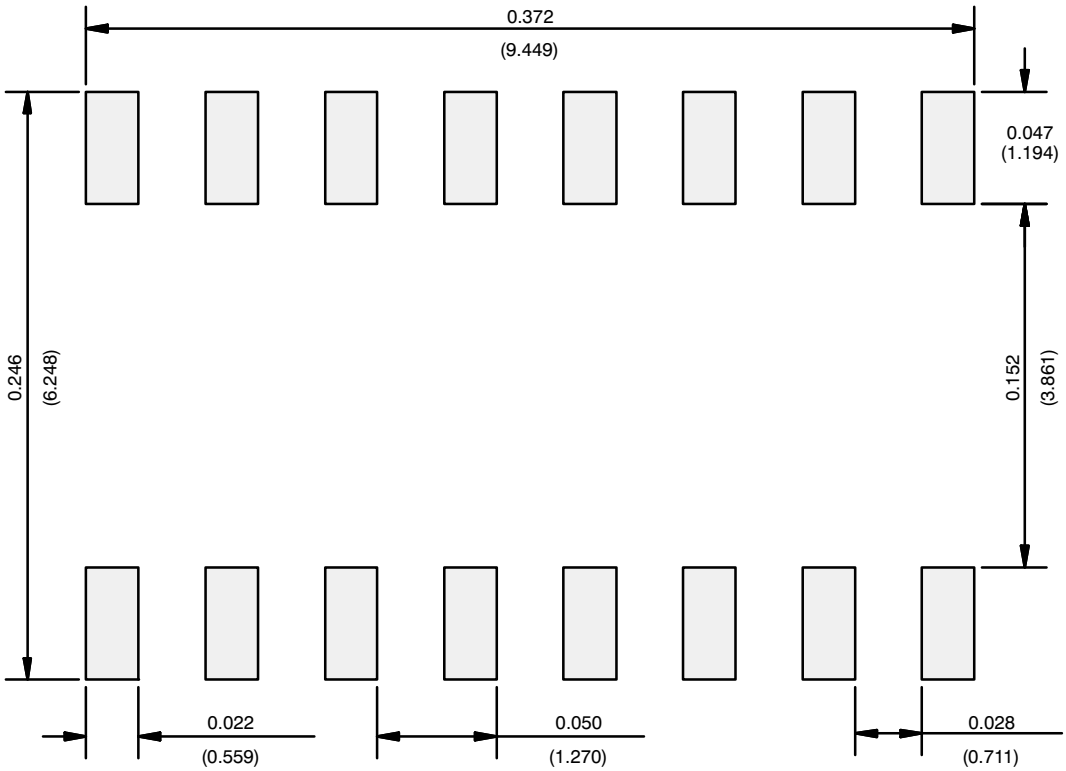
(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

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DWG: 5890

For technical questions, contact: powerictechsupport@vishay.com

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RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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