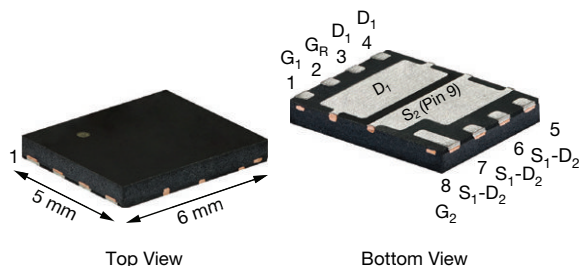


# Symmetric Dual N-Channel 40 V (D-S) MOSFET

## PowerPAIR® 6 x 5FSW



## FEATURES

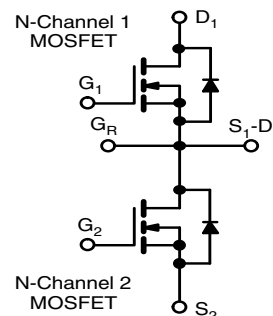
- TrenchFET® Gen IV power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Integrated half-bridge MOSFET power stage
- Wettable flank terminals
- Internally connected switch node
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Buck-boost
- Half-bridge synchronous rectification
- Synchronous buck
- Motor drive control



## PRODUCT SUMMARY

V <sub>DS</sub> (V)	40
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 10 V	0.0015
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 4.5 V	0.0024
I <sub>D</sub> (A) <sup>e</sup>	162
Configuration	Dual

## ORDERING INFORMATION

Package	PowerPAIR 6 x 5FSW
Lead (Pb)-free and halogen-free	SQZF140ELPW-T1_GE3

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V <sub>DS</sub>	40	V
Gate-source voltage	V <sub>GS</sub>	± 20	
Continuous drain current <sup>e</sup>	I <sub>D</sub>	162	A
		93	
Pulsed drain current <sup>e</sup>	I <sub>DM</sub>	543	
Continuous source-drain diode current <sup>e</sup>	I <sub>S</sub>	68	
Single pulse avalanche current	I <sub>AS</sub>	37	mJ
Single pulse avalanche energy	E <sub>AS</sub>	68	
Maximum power dissipation <sup>a, e</sup>	P <sub>D</sub>	75	W
		25	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R <sub>thJA</sub>	30	°C/W
Junction-to-case (exposed pad) <sup>d</sup>	R <sub>thJC</sub>	2.0	

## Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per JESD51-14
- Values based on R<sub>thJC</sub> and T<sub>C</sub> of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		40	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.2	1.7	2.2	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	100	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	500	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 15 A	-	0.00185	0.00240	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A	-	0.00125	0.0015	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C	-	-	0.0024	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C	-	-	0.0030	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 70 A		-	200	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	5042	7059	pF
Output capacitance	C <sub>oss</sub>			-	1096	1535	
Reverse transfer capacitance	C <sub>rss</sub>			-	32	45	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 15 A	-	72	-	nC
Gate-source charge	Q <sub>gs</sub>			-	15	-	
Gate-drain charge	Q <sub>gd</sub>			-	12	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.3	0.9	2.4	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 1.33 Ω I <sub>D</sub> ≅ 15 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	17	26	ns
Rise time	t <sub>r</sub>			-	53	80	
Turn-off delay time	t <sub>d(off)</sub>			-	40	60	
Fall time	t <sub>f</sub>			-	8	12	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 15 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		-	42	84	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	38	76	nC
Reverse recovery fall time	t <sub>a</sub>			-	22		A
Reverse recovery rise time	t <sub>b</sub>			-	22		A
Pulsed current	I <sub>SM</sub>			-	-	300	A
Forward voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V		-	0.75	1.1	V

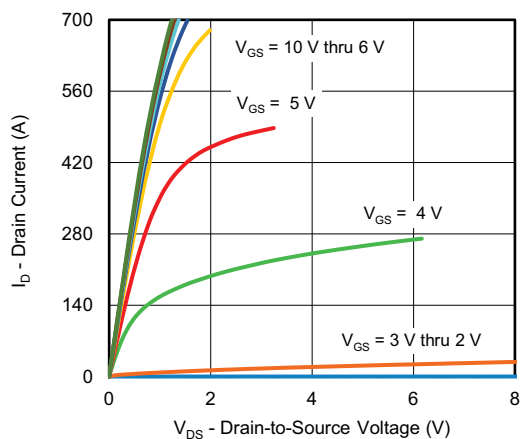
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

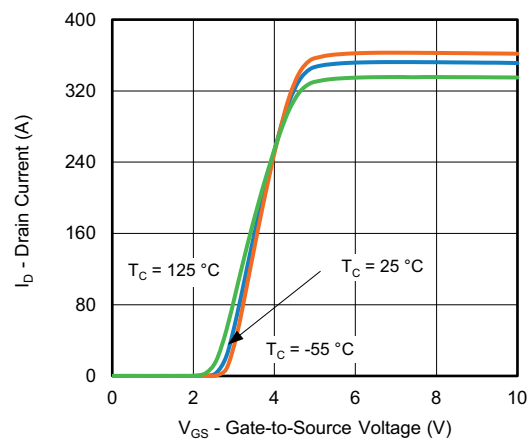
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



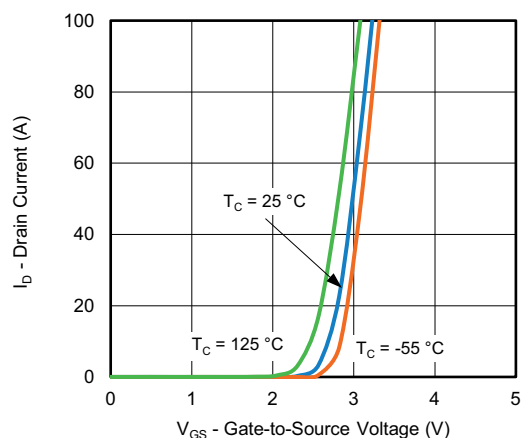
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



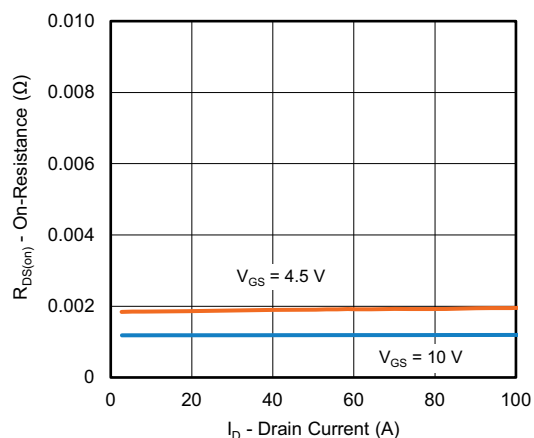
**Output Characteristics**



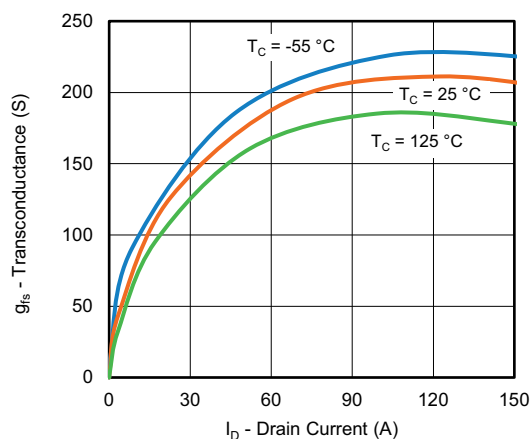
**Transfer Characteristics**



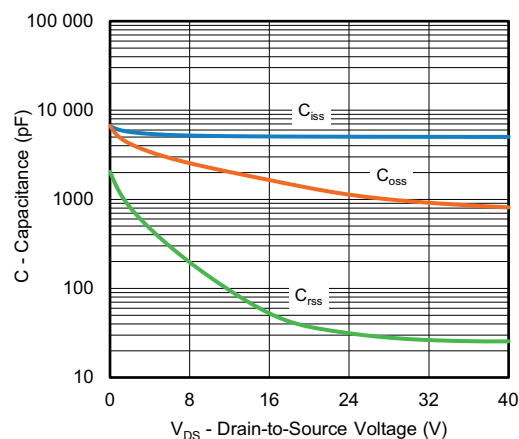
**Transfer Characteristics**



**On-Resistance vs. Drain Current**



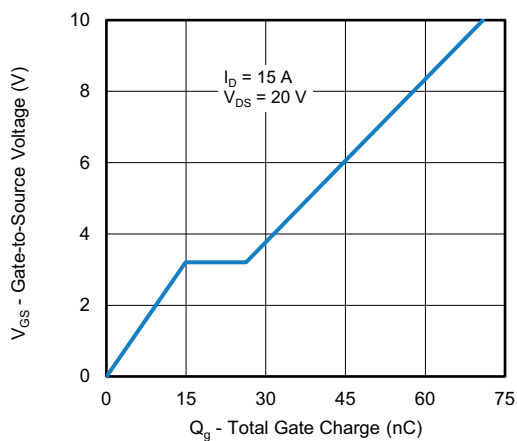
**Transconductance**



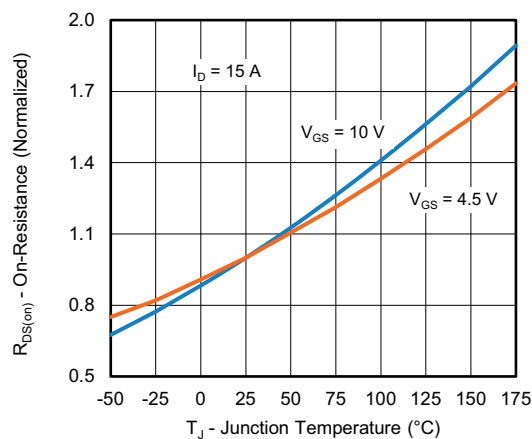
**Capacitance**



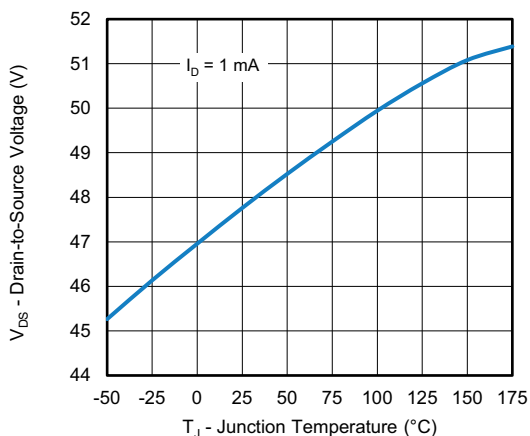
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



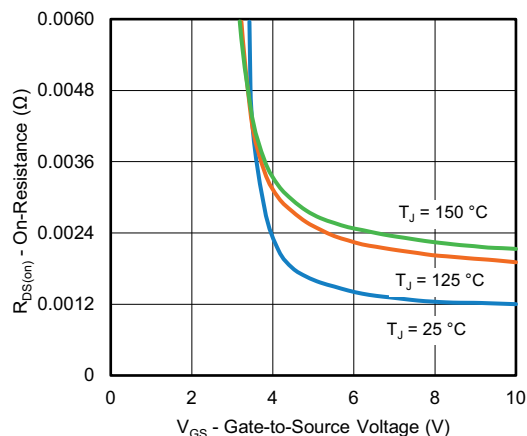
**Gate Charge**



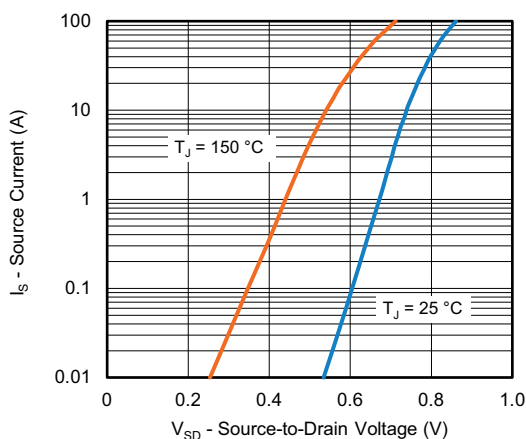
**On-Resistance vs. Junction Temperature**



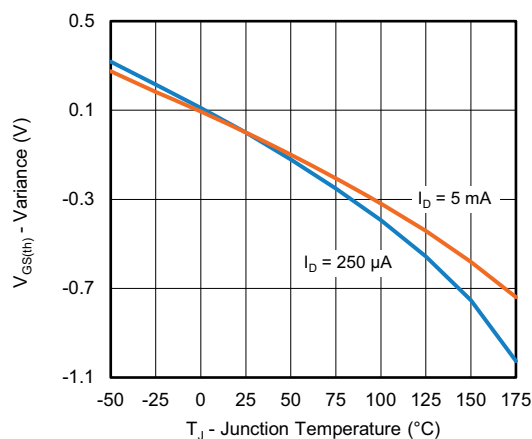
**Drain Source Breakdown vs. Junction Temperature**



**On-Resistance vs. Gate-to-Source Voltage**



**Source-Drain Diode Forward Voltage**



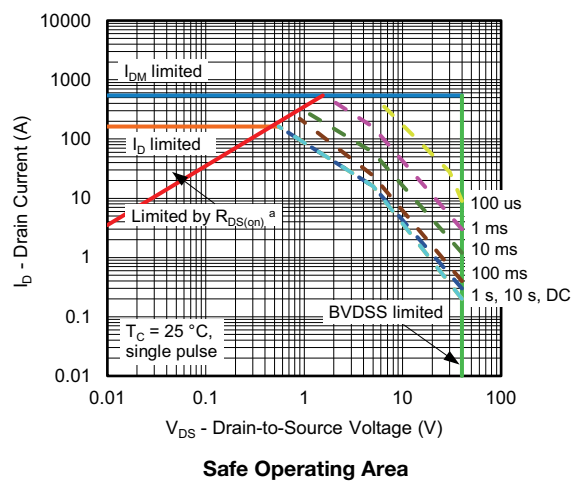
**Threshold Voltage**

**Note**

- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

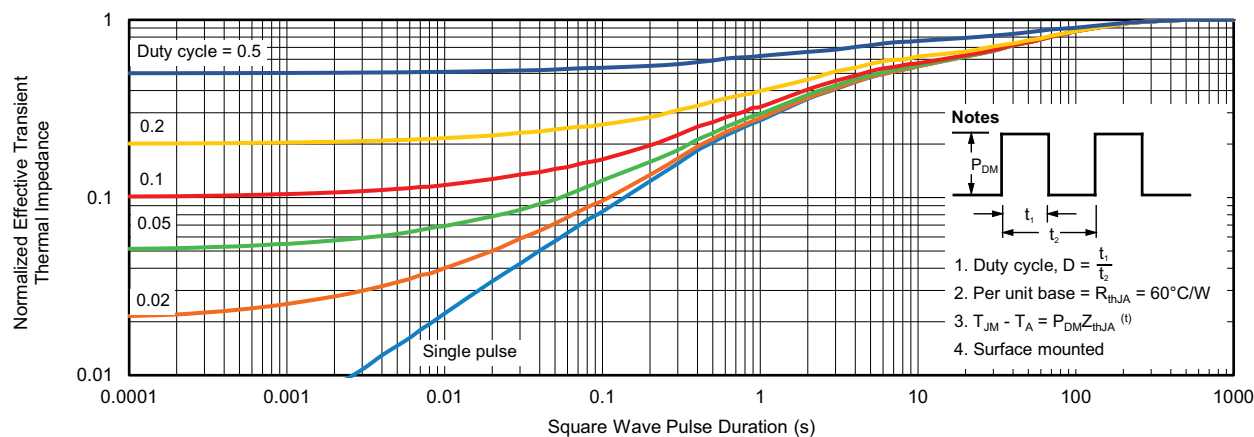


**Note**

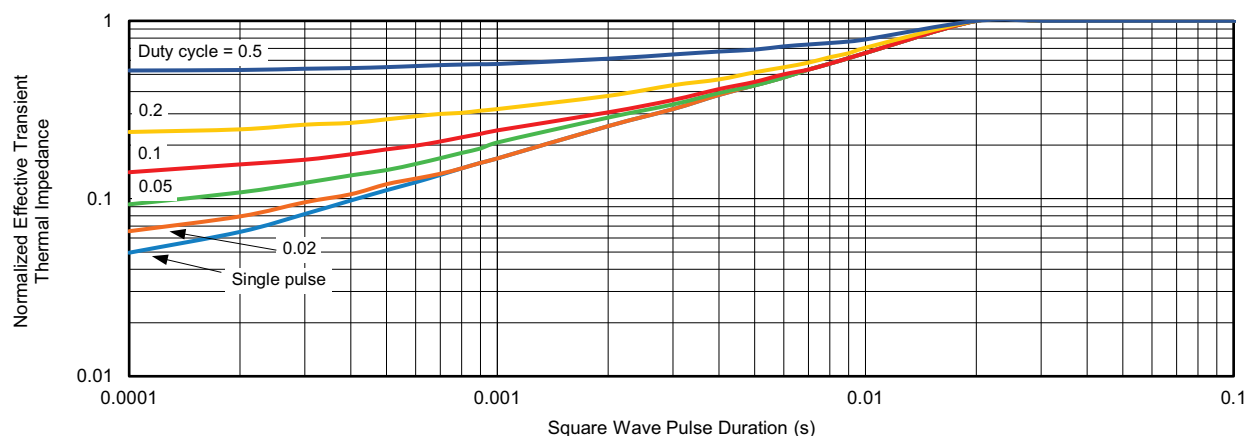
b.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



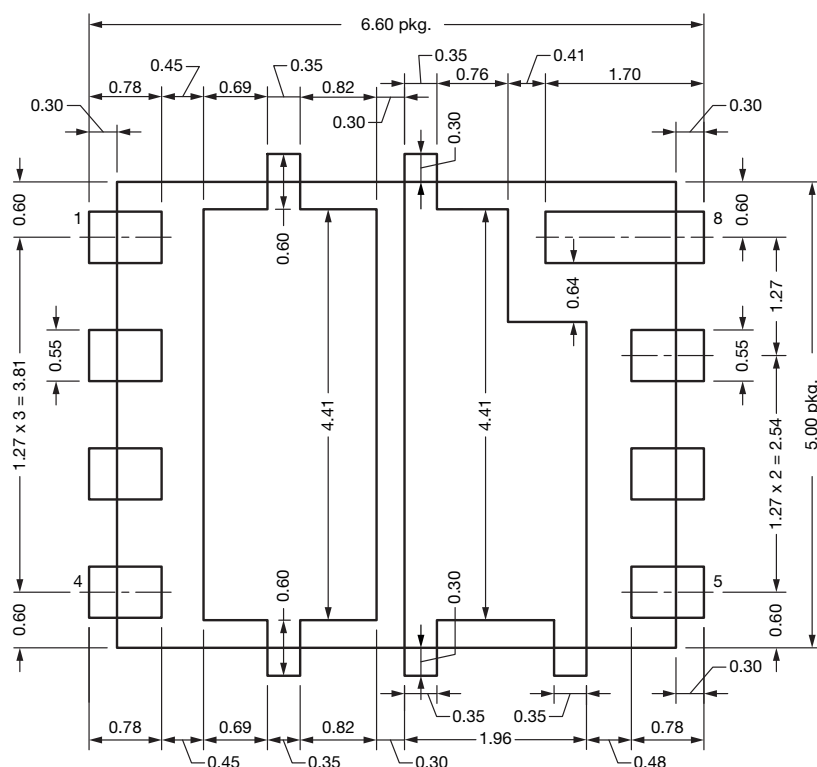
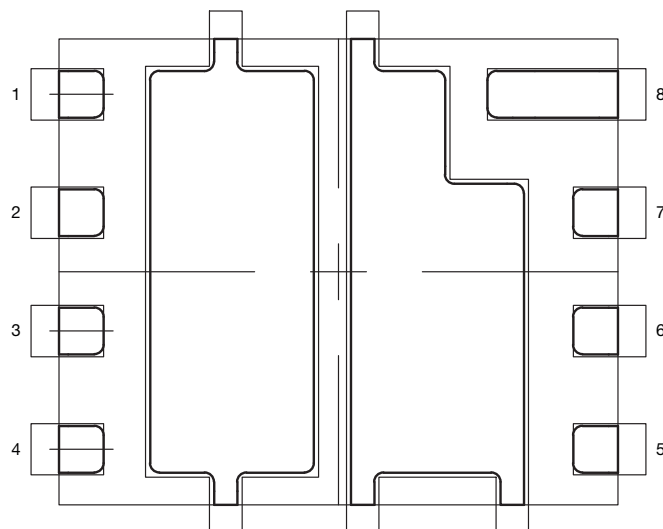
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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## Recommended Land Pattern PowerPAIR® 6 x 5 FS and PowerPAIR® 6 x 5 FSW



### Note

- Dimensions in mm

T24-0311-Rev. A, 09-Sep-2024  
DWG: 3030



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