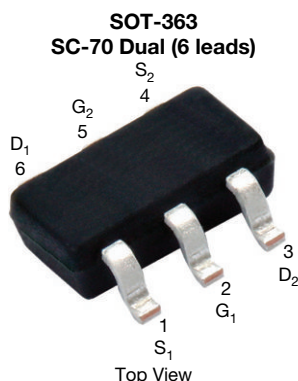


## Dual N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) MAX.	I <sub>D</sub> (A)	Q <sub>g</sub> (nC) TYP.
60	1.4 at V <sub>GS</sub> = 10 V	0.37	0.47
	3 at V <sub>GS</sub> = 4.5 V	0.25	



Marking Code: PD

### Ordering Information:

Si1926DL-T1-E3 (Lead (Pb)-free)

Si1926DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

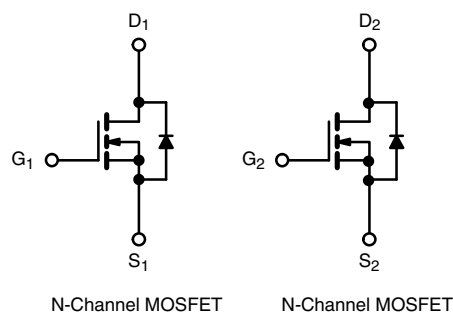
- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> tested
- ESD protected: 1800 V
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Low power load switch



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V <sub>DS</sub>	60	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	0.37	A
	T <sub>C</sub> = 70 °C		0.30	
	T <sub>A</sub> = 25 °C		0.34 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		0.27 <sup>b, c</sup>	
Pulsed Drain Current		I <sub>DM</sub>	0.65	A
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	0.43	
	T <sub>A</sub> = 25 °C		0.25 <sup>b, c</sup>	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	0.51	W
	T <sub>C</sub> = 70 °C		0.33	
	T <sub>A</sub> = 25 °C		0.30 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		0.20 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	360	415
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	300	350

### Notes

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- Maximum under steady state conditions is 400 °C/W.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	56.7	-	mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	-3	-	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	-	2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 10 V	-	-	± 150	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C	-	-	10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 4.5 V	0.50	-	-	A
		V <sub>DS</sub> ≥ 7.5 V, V <sub>GS</sub> = 10 V	0.65	-	-	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.34 A	-	-	1.4	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.23 A	-	-	3	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 0.2 A	-	159	-	ms
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	18.5	-	pF
Output Capacitance	C <sub>oss</sub>		-	7.5	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	4.2	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.34 A	-	0.9	1.4	nC
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.34 A	-	0.5	0.75	
Gate-Source Charge	Q <sub>gs</sub>		-	0.2	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.15	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	-	160	240	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 100 Ω, I <sub>D</sub> ≅ 0.3 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	6.5	10	ns
Rise Time	t <sub>r</sub>		-	12	18	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	13	22	
Fall Time	t <sub>f</sub>		-	14	21	
Drain-Source Body Diode Characteristics						
Continuous Sorce-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	0.43	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		-	-	0.65	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.3 A	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 0.6 A, dI/dt = 100 A/μs	-	16.5	25	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	13	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>		-	13.5	-	ns
Reverse Recovery Rise Time	t <sub>b</sub>		-	3	-	

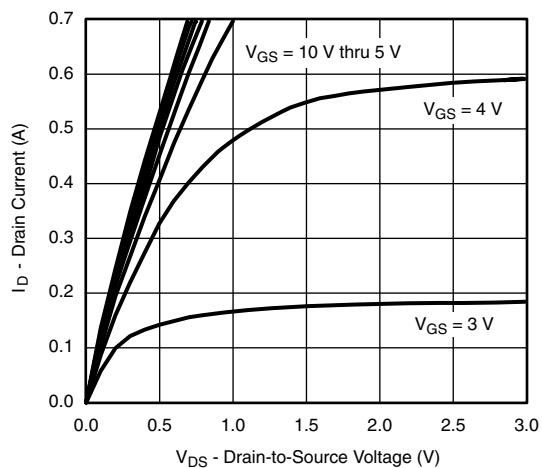
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

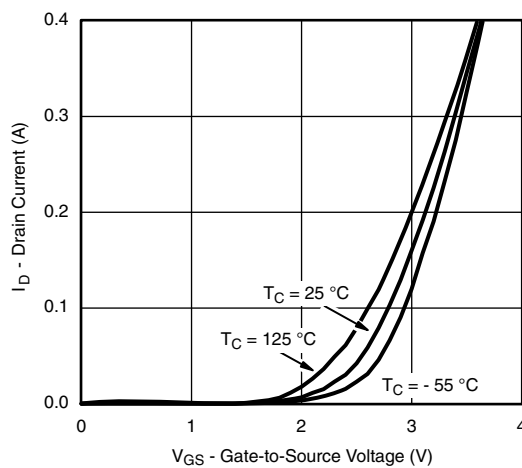
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



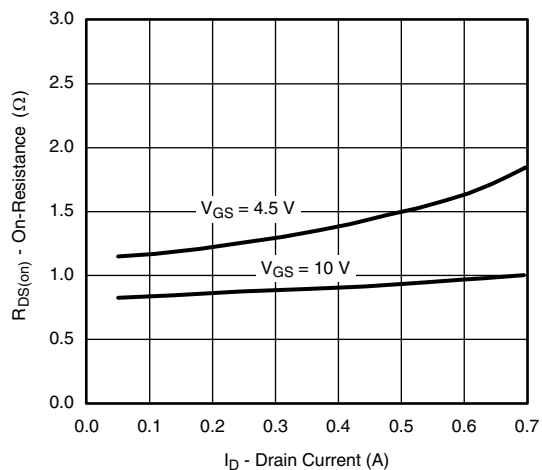
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



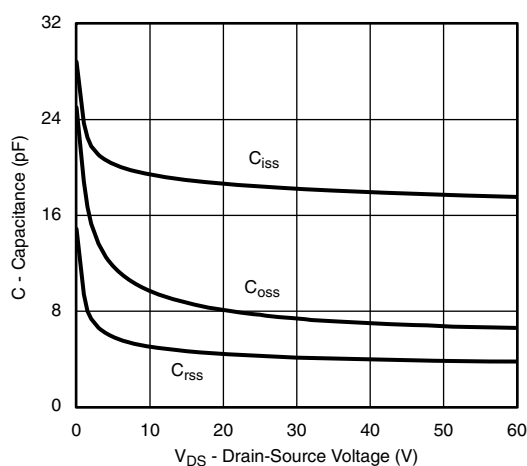
**Output Characteristics**



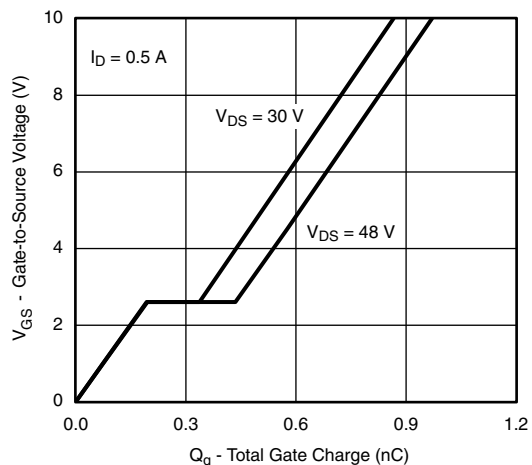
**Transfer Characteristics Curves vs. Temperature**



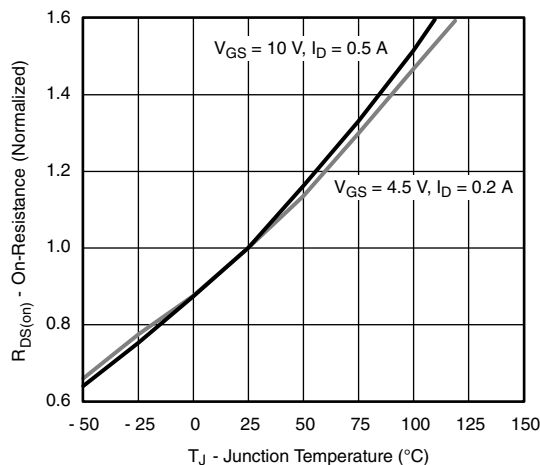
**On-Resistance vs. Drain Current**



**Capacitance**



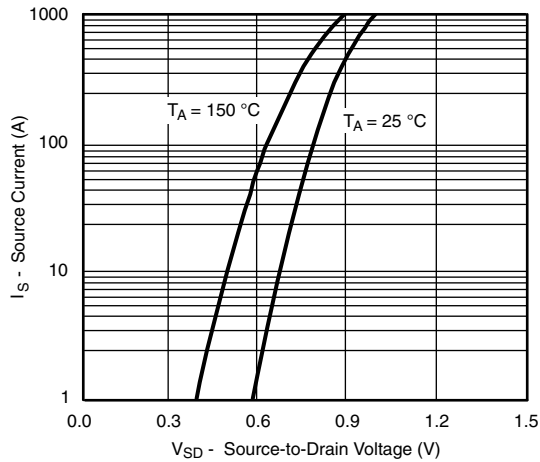
**Gate Charge**



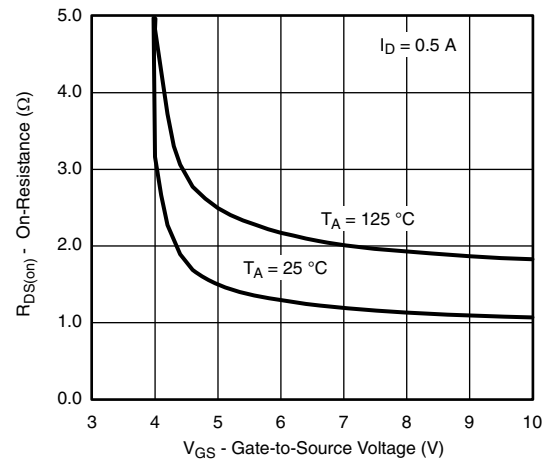
**On-Resistance vs. Junction Temperature**



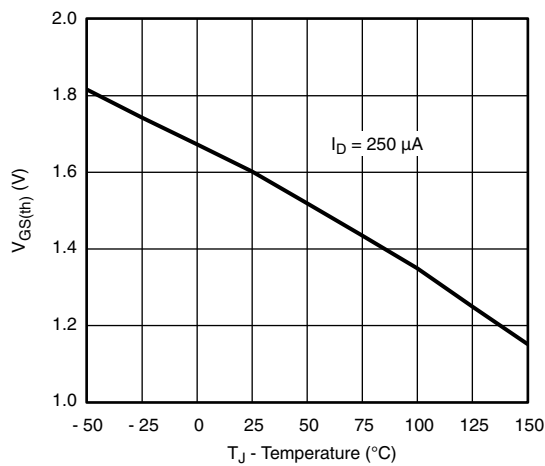
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



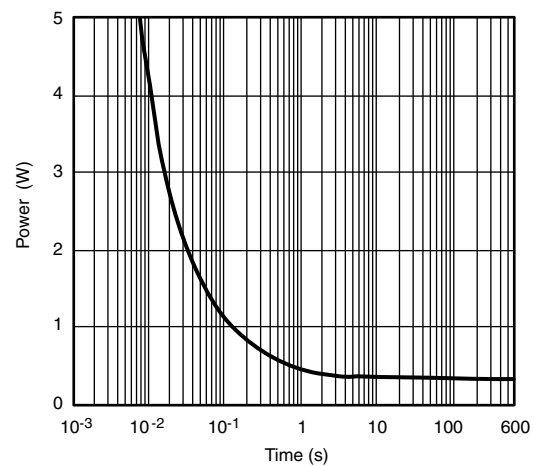
Source-Drain Diode Forward Voltage



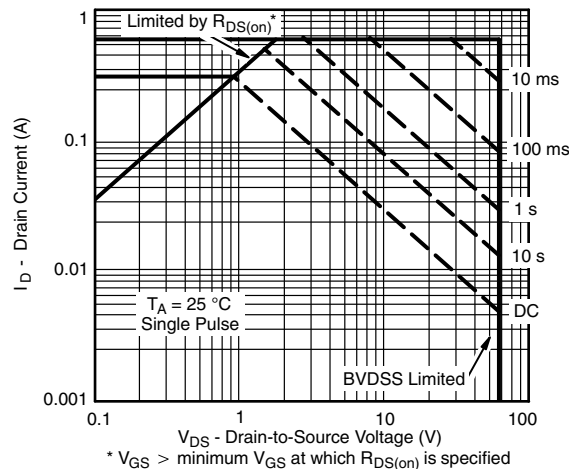
$R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature



Threshold Voltage



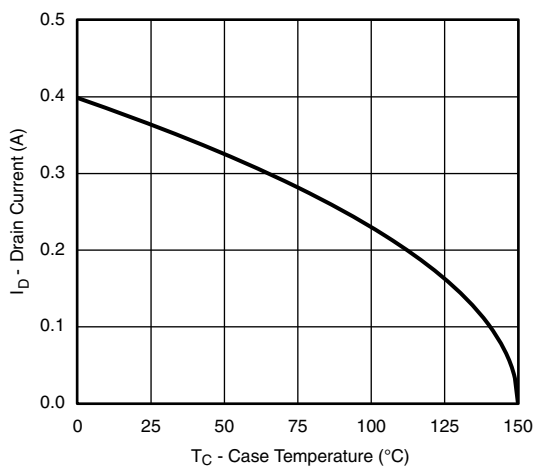
Single Pulse Power



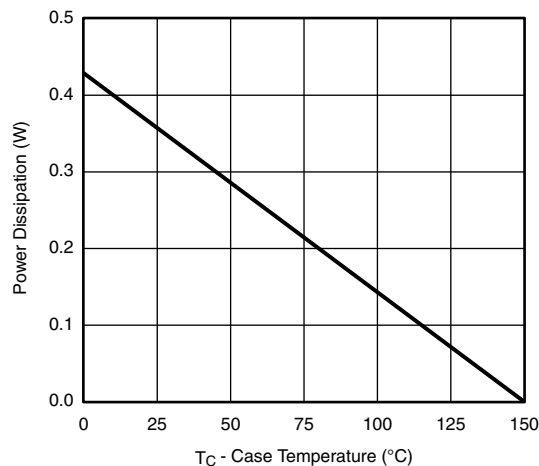
Safe Operating Area



**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Current Derating <sup>a</sup>**



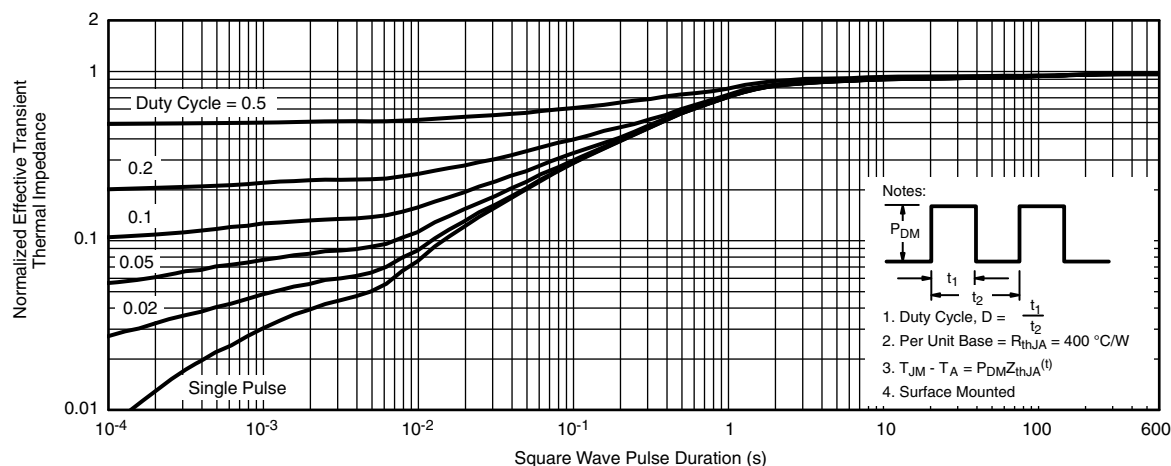
**Power Derating**

**Note**

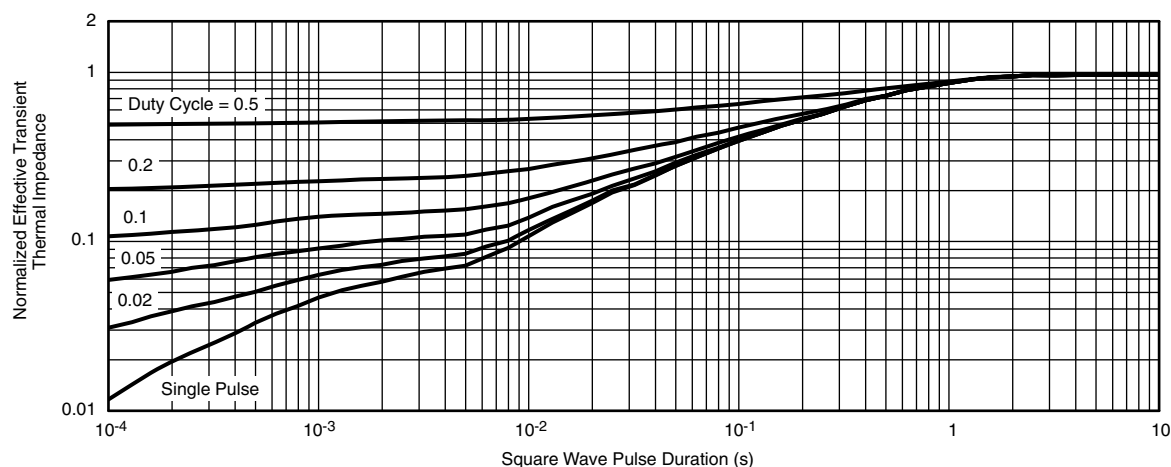
- a. The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ }^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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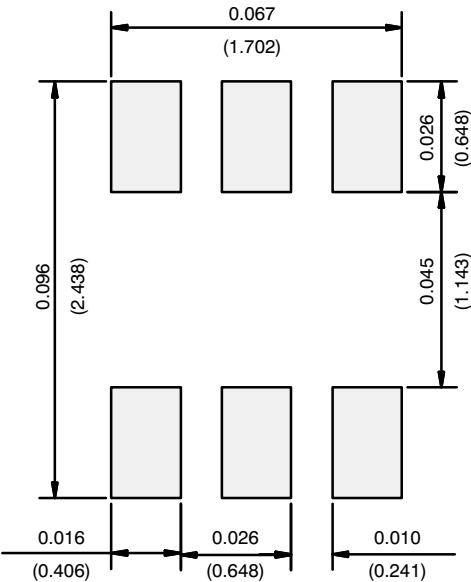


**SC-70: 6-LEADS**



	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	0.90	—	1.10	0.035	—	0.043
A <sub>1</sub>	—	—	0.10	—	—	0.004
A <sub>2</sub>	0.80	—	1.00	0.031	—	0.039
b	0.15	—	0.30	0.006	—	0.012
c	0.10	—	0.25	0.004	—	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01						
DWG: 5550						

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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