SQS180ELNW

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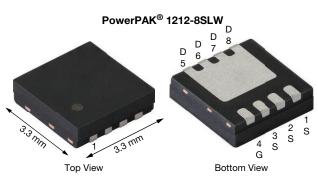
Vishay Siliconix

RoHS

COMPLIANT HALOGEN

FREE

Automotive N-Channel 80 V (D-S) 175 °C MOSFET

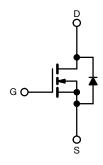


Marking code: Q066

PRODUCT SUMMARY	
V _{DS} (V)	80
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0071
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.0083
I _D (A) ^e	82
Configuration	Single

FEATURES

- TrenchFET[®] Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Wettable flank terminals
- Low thermal resistance with 0.75 mm profile
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK [®] 1212-8SLW
Lead (Pb)-free and halogen-free	SQS180ELNW (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless	otherwise noted	(k		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	80	V	
Gate-source voltage		V _{GS}	± 20		
Continuous drain current ^e	T _C = 25 °C	- I _D -	82		
	T _C = 125 °C		47		
Continuous source current (diode conduction) e		I _S	108	А	
Pulsed drain current ^{a, e}		I _{DM}	189		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	28		
Single pulse avalanche energy	L = 0.1 MH	E _{AS}	40	mJ	
Maximum power dissipation ^{a, e}	T _C = 25 °C	D	119	w	
	T _C = 125 °C	P _D	39		
Operating junction and storage temperature range Soldering recommendations (peak temperature) ^c		T _J , T _{stg}	-55 to +175	°C	
			260	U	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount ^b	R _{thJA}	54	°C/W	
Junction-to-case (drain) ^d		R _{thJC}	1.3	0/10	

Notes

- a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
 b. When mounted on 1" square PCB (FR4 material)
 c. See solder profile (<u>www.vishay.com/doc?73257</u>). A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- d. As per on JESD51-14
- Values based on RthJC and TC of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system e.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \ \mu A$		80	-	-	v	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		1.4	1.9	2.5	v	
Gate-source leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 80 V	-	-	1		
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V _{DS} = 80 V, T _J = 175 °C	-	-	150		
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	15	-	-	Α	
		V _{GS} = 10 V	I _D = 10 A	-	0.0053	0.0071	-	
5	-	V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0150	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0185		
		V _{GS} = 4.5 V	I _D = 10 A	-	0.0065	0.0083		
Forward transconductance b	g _{fs}	V _{DS}	= 15 V, I _D = 10 A	-	65	-	S	
Dynamic ^b		1						
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	2635	3689	pF	
Output capacitance	C _{oss}			-	360	504		
Reverse transfer capacitance	C _{rss}			-	25	35		
Total gate charge ^c	Qg			-	45	68	nC	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 40 \text{ V}, \text{ I}_{D} = 4 \text{ A}$	-	8	-		
Gate-drain charge ^c	Q _{gd}				8	-	-	
Gate resistance	R _g		f = 1 MHz	0.4	1.0	2.0	Ω	
Turn-on delay time ^c	t _{d(on)}			-	12	18		
Rise time ^c	t _r	- V:	= 40 V, R _I = 16 Ω	-	4	8	ns	
Turn-off delay time ^c	t _{d(off)}		$V_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	33	50		
Fall time ^c	t _f			-	14	21	1	
Source-Drain Diode Ratings and Charac	teristic ^b							
Pulsed current ^a	I _{SM}			-	-	350	Α	
Forward voltage	V _{SD}	I _F = 10 A, V _{GS} = 0 V		-	0.82	1.1	V	
Body diode reverse recovery time	t _{rr}	V _{DD} = 64 V, I _F = 3.5 A, di/dt = 100 A/μs, R = 10 Ω, L = 0.3 mH, pulse width = 2 μs		-	37	74	ns	
Body diode reverse recovery charge	Q _{rr}			-	48	96	nC	
Reverse recovery fall time	t _a			-	25	-		
Reverse recovery rise time	t _b			-	12	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}	1		-	-2.2	_	А	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

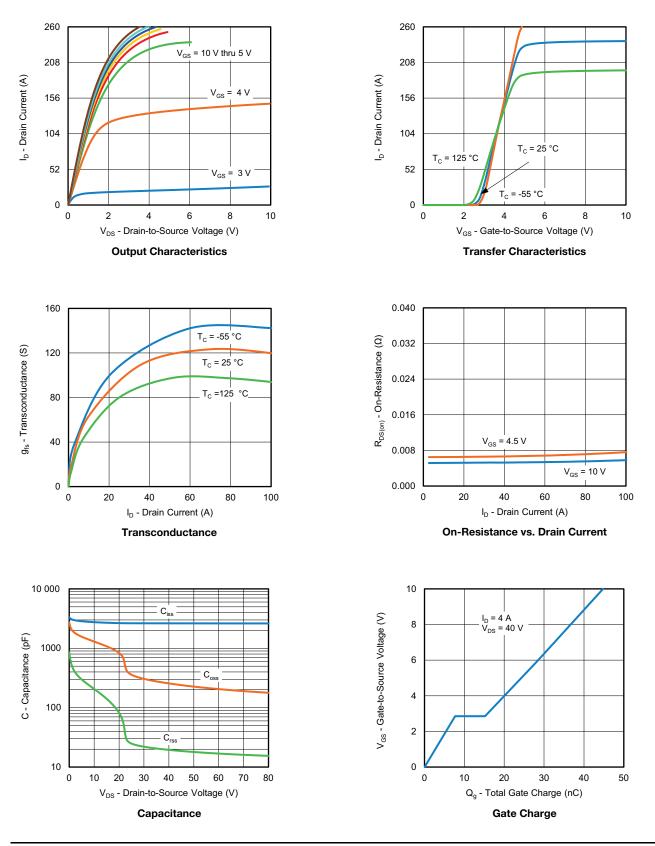
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



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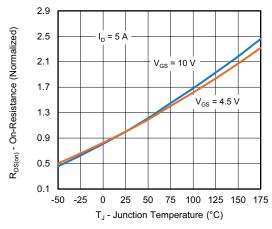
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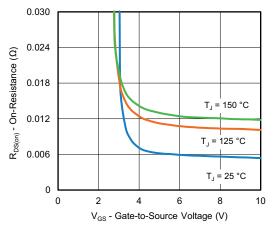


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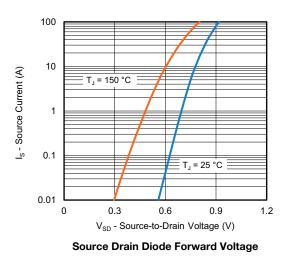
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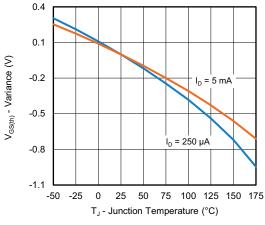


On-Resistance vs. Junction Temperature

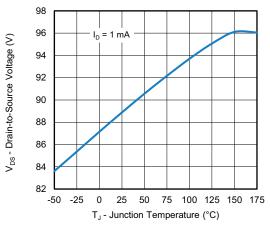


On-Resistance vs. Gate-to-Source Voltage

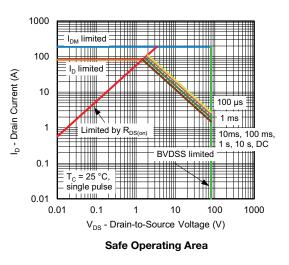




Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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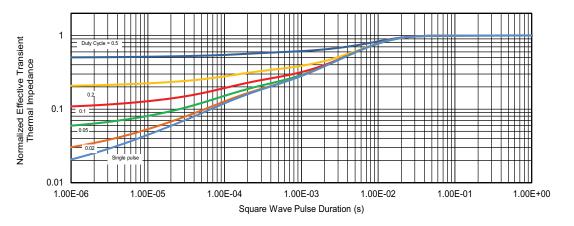
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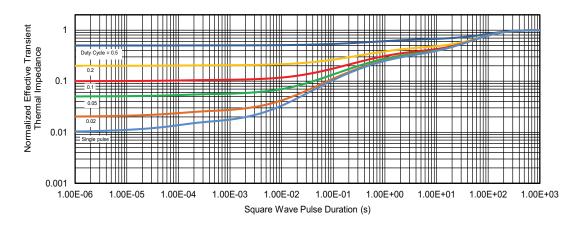


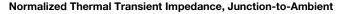
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case





Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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