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Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY							
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^{a, e}	Q _g (TYP.)				
	0.047 at V _{GS} = -4.5 V	-4					
-20	0.080 at $V_{GS} = -2.7 \text{ V}$	-4	9 nC				
	0.090 at V _{GS} = -2.5 V	-4					

TSOP-6 Single Top View

• TrenchFET® power MOSFET

PWM optimized

FEATURES

• 100 % R_q tested

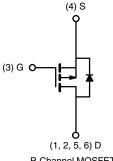
• Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT HALOGEN **FREE**

APPLICATIONS

- · Hard disk drives
- DC/DC converter
- · Load switch
- · Portable devices



P-Channel MOSFET

Marking Code: BN **Ordering Information:**

Si3443DDV-T1-GE3 (Lead (Pb)-free and Halogen-free)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	-20		
Gate-Source Voltage		V_{GS}	± 12	V
	T _C = 25 °C		-4 e	
Continuous Dunin Comment (T. 150 °C)	T _C = 70 °C	T . [-4 ^e	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	l _D	_4 b, c, e	
	T _A = 70 °C	Ī	-3.9 b, c	Α
Pulsed Drain Current (t = 300 μs)		I _{DM}	-20	
Ocalia de Ocala Designata Ocala	T _C = 25 °C		-2.25	
Continuous Source-Drain Diode Current	T _A = 25 °C	ls -	-1.42 ^{b, c}	
	T _C = 25 °C		2.7	
	T _C = 70 °C	1 _ [1.7	
Maximum Power Dissipation	T _A = 25 °C	P _D	1.7 ^{b, c}	W
	T _A = 70 °C	†	1.1 ^{b, c}	
Operating Junction and Storage Temperature	T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum Junction-to-Ambient b, d	t ≤ 5 s	R_{thJA}	61	74	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	38	46	G/ VV		

Notes

- a. Based on $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- d. Maximum under steady state conditions is 120 °C/W.
- e. Package limited.

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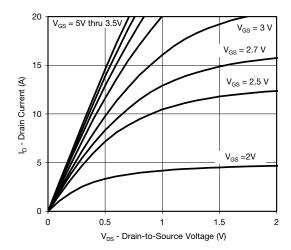
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						•
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	-15	-	mV/°C
V _{GS(th}) Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	2.8	-	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = -250 \ \mu A$	-0.6	-	-1.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	± 100	nA
Zava Cata Valtaga Dvain Cuwant	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μΑ
Zero Gate Voltage Drain Current		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20	-	-	Α
		$V_{GS} = -4.5 \text{ V}, I_D = -4.7 \text{ A}$	-	0.039	0.047	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -2.7 V, I _D = -1.4 A	-	0.057	0.080	
		V _{GS} = -2.5 V, I _D = -1.2 A	-	0.064	0.090	
Forward Transconductance ^a g _{fs}		V _{DS} = -10 V, I _D = -4.7 A	-	14	-	S
Dynamic ^b						
Input Capacitance	C _{iss}		-	970	-	pF
Output Capacitance	Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	125	-	
Reverse Transfer Capacitance	C _{rss}		-	111	-	
Total Cata Charge	Q_g	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -4.9 \text{ A}$	-	20	30	nC
Total Gate Charge			-	9	18	
Gate-Source Charge	Q _{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -4.9 \text{ A}$	-	1.9	-	
Gate-Drain Charge	Q _{gd}		-	1.7	-	
Gate Resistance	R_g	f = 1 MHz	2.5	12.3	24.6	Ω
Turn-On Delay Time	t _{d(on)}		-	27	41	
Rise Time	t _r	$V_{DD} = -10 \text{ V}, R_L = 2.56 \Omega$	-	25	38	- ns
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -3.9 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	43	65	
Fall Time	t _f		-	18	27	
Drain-Source Body Diode Characteristic	s					
Continuous Source-Drain Diode Current	Is	T _C = 25 °C	-	=.	-2.25	Α
Pulse Diode Forward Current ^a	I _{SM}		-	-	-20	
Body Diode Voltage	V_{SD}	I _S = -3.9 A	-	-0.85	-1.2	V
Body Diode Reverse Recovery Time	t _{rr}		-	11	20	ns
Body Diode Reverse Recovery Charge Q _{rr}		L 2 0 A dl/dt _ 100 A/:: T	-	3	6	nC
Reverse Recovery Fall Time	t _a	$I_F = -3.9 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 °C$	-	6	-	ne
Reverse Recovery Rise Time	t _b	7		5		ns

Notes

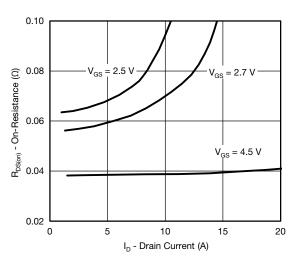
- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

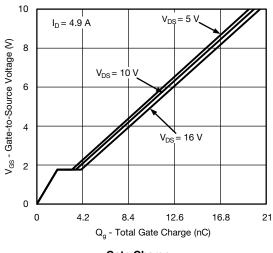




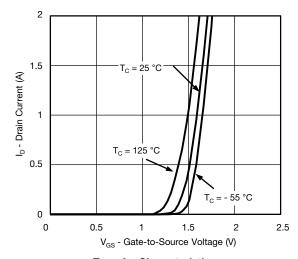
Output Characteristics



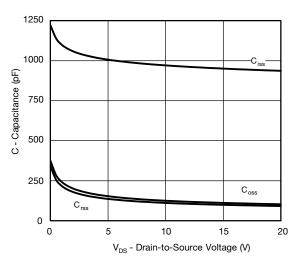
On-Resistance vs. Drain Current



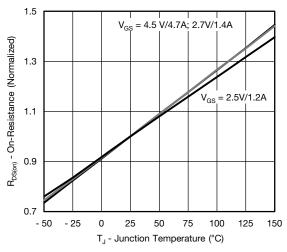
Gate Charge



Transfer Characteristics

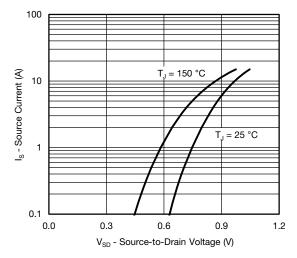


Capacitance

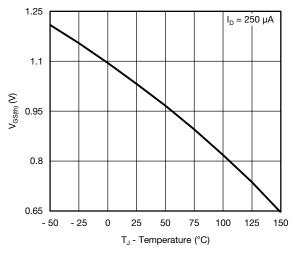


On-Resistance vs. Junction Temperature

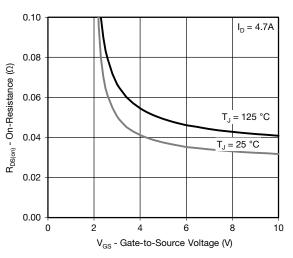




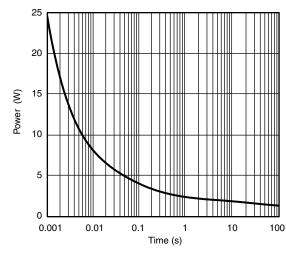
Source-Drain Diode Forward Voltage



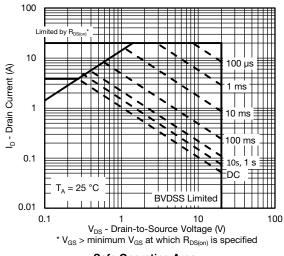
Threshold Voltage



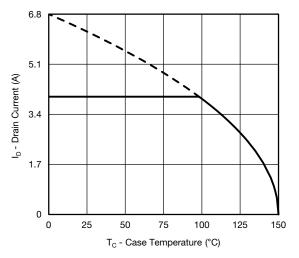
On-Resistance vs. Gate-to-Source Voltage



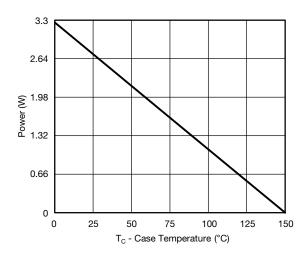
Single Pulse Power, Junction-to-Ambient

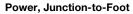


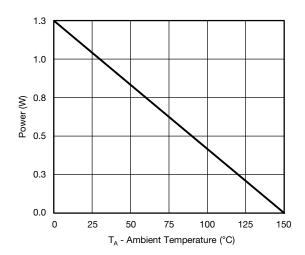




Current Derating*



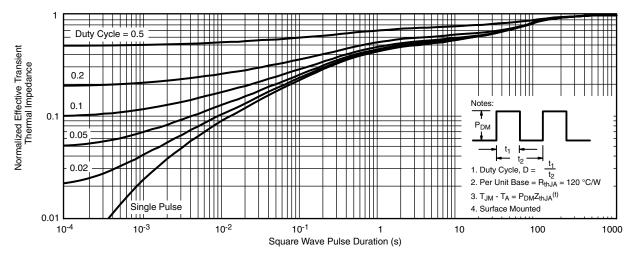




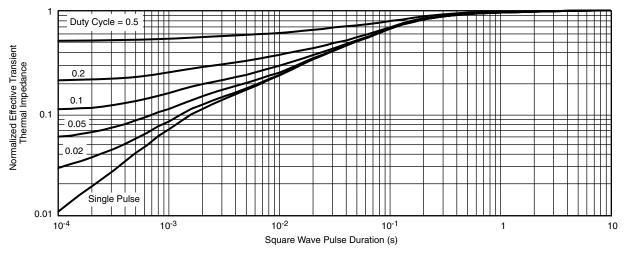
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J \text{ (max.)}} = 150 \,^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

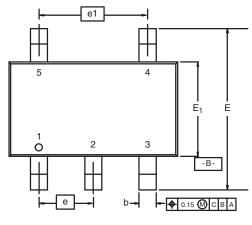
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62956.

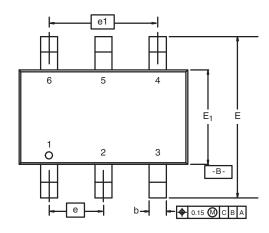




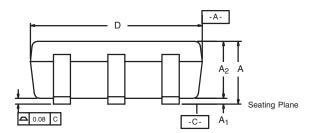
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C

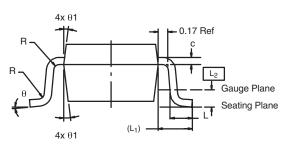




5-LEAD TSOP







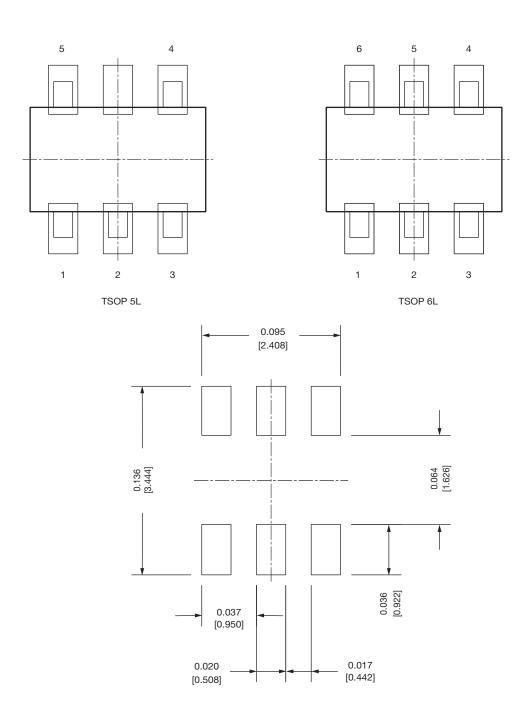
	MILLIMETERS INCHES						
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.008		
D	2.95	3.05	3.10	0.116	0.116 0.120		
E	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е	0.95 BSC			0.0374 BSC			
e ₁	1.80	1.90	2.00	0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L ₁	0.60 Ref			0.024 Ref			
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

DWG: 5540

Document Number: 71200 18-Dec-06



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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