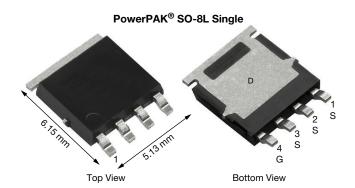
www.vishay.com

Vishay Siliconix

Automotive P-Channel 60 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	-60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.018			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.024			
I _D (A)	-52			
Configuration	Single			

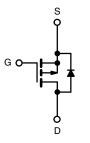
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified ^c
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





COMPLIANT HALOGEN **FREE**



P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ459EP (for detailed order number please see www.vishay.com/doc?79771)

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	-60	V	
Gate-source voltage		V _{GS}	± 20	V	
Continuous dusin suurent	T _C = 25 °C	1	-52	A	
Continuous drain current	T _C = 125 °C	I _D	-30		
Continuous source current (diode conductio	n)	I _S	-75		
Pulsed drain current ^a		I _{DM}	-200		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	-40		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	80	mJ	
Manian and displaying a	T _C = 25 °C	Б	83	W	
Maximum power dissipation ^a	T _C = 125 °C	P_{D}	27		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e			260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction to ambient	PCB mount b	R_{thJA}	65	°C/W
Junction to case (drain)		R_{thJC}	1.8	C/VV

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. When mounted on 1" square PCB (FR4 material)
- c. Parametric verification ongoing
- d. See solder profile (www.vishav.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



Vishay Siliconix

SPECIFICATIONS ($T_C = 25$ °C,	unless otherv	vise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	1					L	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0, I _D = -250 μA	-60	-	-	.,,
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = -250 μA	-1.5	-2.0	-2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = -60 V	-	-	-1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = -60 V, T _J = 125 °C	-	-	-50	μΑ
		V _{GS} = 0 V	V _{DS} = -60 V, T _J = 175 °C	-	-	-150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} £ -5 V	-30	-	-	Α
		V _{GS} = -10 V	I _D = -3.5 A	-	0.0155	0.0180	
Drain-Source On-State Resistance a	В	V _{GS} = -4.5 V	I _D = -3.1 A	=.	0.0206	0.0240	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -3.5 A, T _J = 125 °C	-	0.0255	-	Ω
		V _{GS} = -10 V	I _D = -3.5 A, T _J = 175 °C	-	0.0310	-	
Forward Transconductance b	9 _{fs}	V _{DS} =	= -30 V, I _D = -15 A	-	40	-	S
Dynamic ^b							
Input Capacitance	C _{iss}			=.	3448	4586	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = -30 \text{ V, f} = 1 \text{ MHz}$	=.	374	497	pF
Reverse Transfer Capacitance	C _{rss}			-	234	312	
Total Gate Charge c	Qg			=.	73	108	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = -10 V	$V_{DS} = -40 \text{ V}, I_{D} = -15 \text{ A}$	=.	10	-	nC
Gate-Drain Charge ^c	Q _{gd}	1		-	20	-	
Gate Resistance	R _g		f = 1 MHz	0.5	1.1	2	Ω
Turn-On Delay Time ^c	t _{d(on)}			=.	12	17	
Rise Time ^c	t _r	V _{DD} =	= -30 V, $R_L = 30 \Omega$	-	19	26	
Turn-Off Delay Time c	t _{d(off)}	$I_D \cong -1 A$,	$V_{GEN} = -10 \text{ V}, R_g = 6 \Omega$	-	88	117	ns
Fall Time ^c	t _f]		-	45	60	
Source-Drain Diode Ratings and Charact	teristics ^b						
Pulsed Current ^a	I _{SM}			=.	-	-200	Α
Forward Voltage	V _{SD}	l _F =	-2.5 A, V _{GS} = 0	-	-0.8	-1.2	V

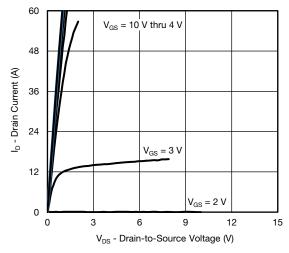
Notes

- f. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- g. Guaranteed by design, not subject to production testing.
- h. Independent of operating temperature.

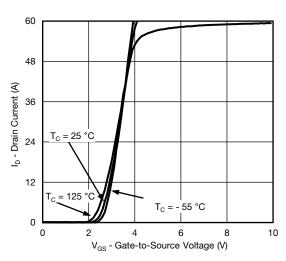
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



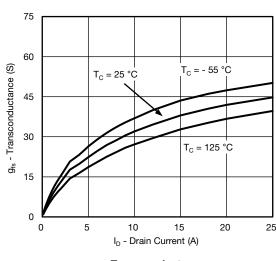
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



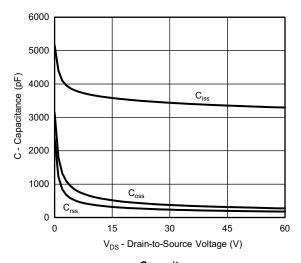
Output Characteristics



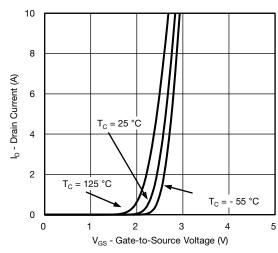
Transfer Characteristics



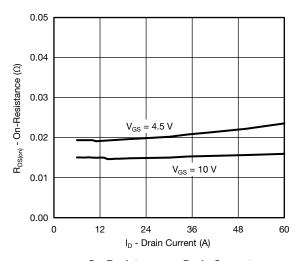
Transconductance



Capacitance



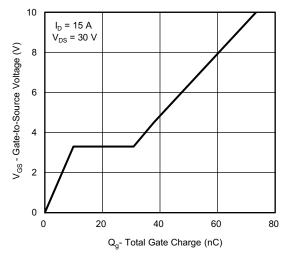
Transfer Characteristics



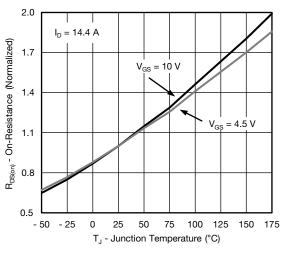
On-Resistance vs. Drain Current



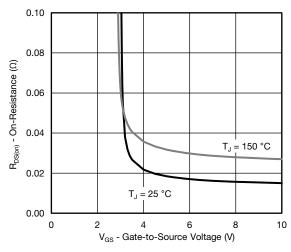
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



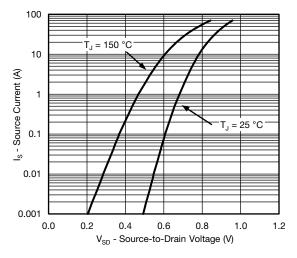
Gate Charge



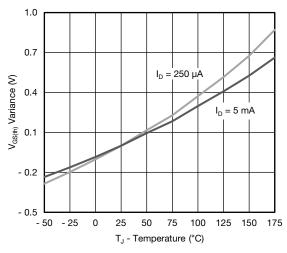
On-Resistance vs. Junction Temperature



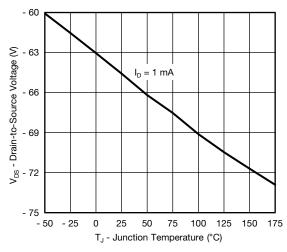
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage



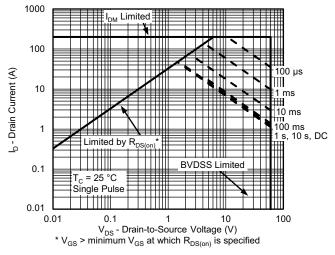
Threshold Voltage



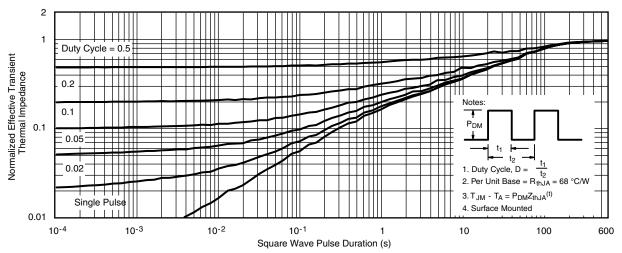
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



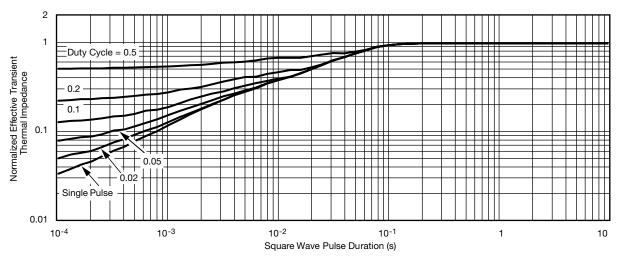
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

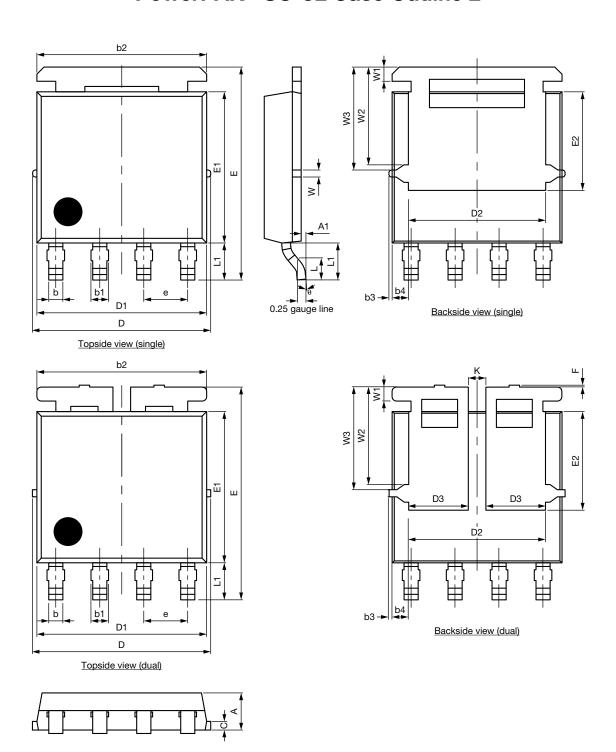
can widely vary depending on actual application parameters and operating conditions.

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg266963.



PowerPAK® SO-8L Case Outline 2



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DIM.		MILLIMETERS			INCHES			
DIN.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
А	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	-	0.127	0.00	-	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3		0.094			0.004			
b4		0.47			0.019			
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D3	1.63	1.73	1.83	0.064	0.068	0.072		
е		1.27 BSC			0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	2.75	2.85	2.95	0.108	0.112	0.116		
F	-	-	0.15	-	-	0.006		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
K		0.51			0.020			
W	0.23		0.009					
W1	0.41				0.016			
W2	2.82			0.111				
W3		2.96			0.117			
θ	0°	-	10°	0°	-	10°		

ECN: C21-1498-Rev. C, 01-Nov-2021

DWG: 6044

Note

• Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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