

Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Advanced process technology
- Ultra low on-resistance
- Dynamic dV/dt rating
- 175 °C operating temperature
- Fast switching
- Fully avalanche rated
- Drop in replacement of the IRFZ44, SiHFZ44 for linear / audio applications
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Advanced power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.028
Q_g (Max.) (nC)	67	
Q_{gs} (nC)	18	
Q_{gd} (nC)	25	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFZ44RPbF
Lead (Pb)-free and halogen-free	IRFZ44RPbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	200	
Linear derating factor		1.0	W/°C
Single pulse avalanche energy ^b	E_{AS}	100	mJ
Maximum power dissipation	P_D	150	W
Peak diode recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 44\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 51\text{ A}$ (see fig. 12)
- $I_{SD} \leq 51\text{ A}$, $dV/dt \leq 250\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$
- 1.6 mm from case
- Current limited by the package, (die current = 51 A)

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

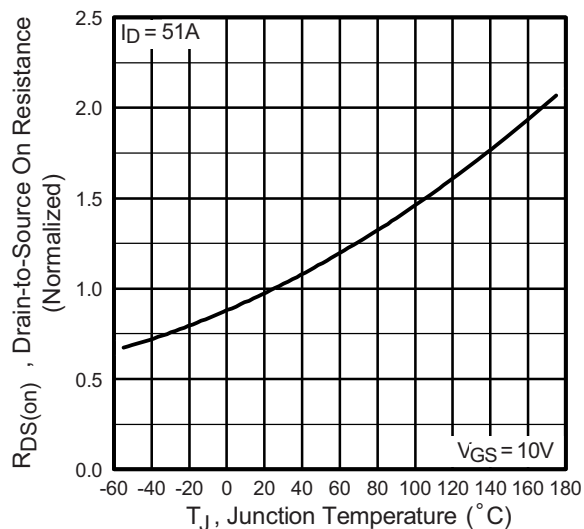
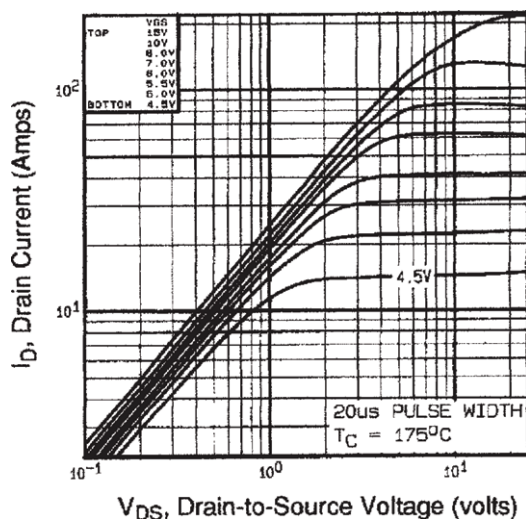
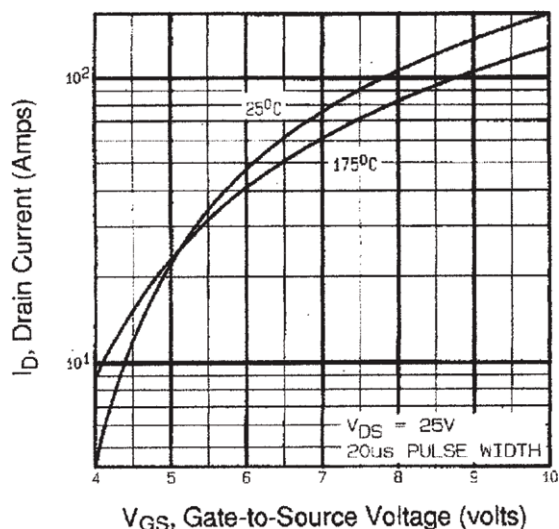
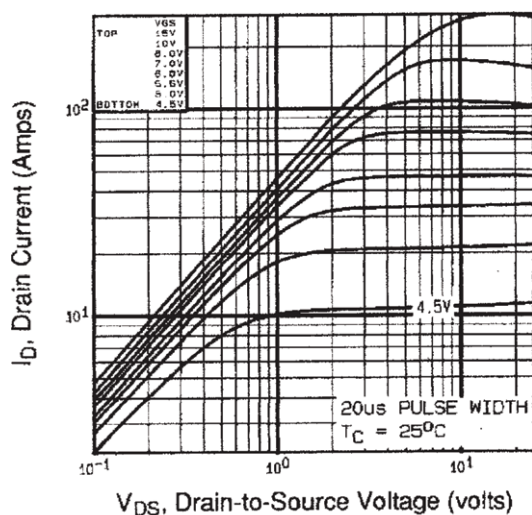
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.060	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 31 A ^b	-	-	0.028	Ω
Forward transconductance	g _{fs}	V _{DS} = 25 V, I _D = 31 A ^b		15	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1900	-	pF
Output capacitance	C _{oss}			-	920	-	
Reverse transfer capacitance	C _{rss}			-	170	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 51 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	67	nC
Gate-source charge	Q _{gs}			-	-	18	
Gate-drain charge	Q _{gd}			-	-	25	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, I _D = 51 A, R _g = 9.1 Ω, R _D = 0.55 Ω, see fig. 10 ^b		-	14	-	ns
Rise time	t _r			-	110	-	
Turn-off delay time	t _{d(off)}			-	45	-	
Fall time	t _f			-	92	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50 ^c	A
Pulsed diode forward current ^a	I _{SM}			-	-	200	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 51 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 51 A, dI/dt = 100 A/μs ^b		-	120	180	ns
Body diode reverse recovery charge	Q _{rr}			-	0.53	0.80	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- Current limited by the package (die current = 51 A)

TYPICAL CHARACTERISTICS ($25\text{ }^{\circ}\text{C}$, unless otherwise noted)



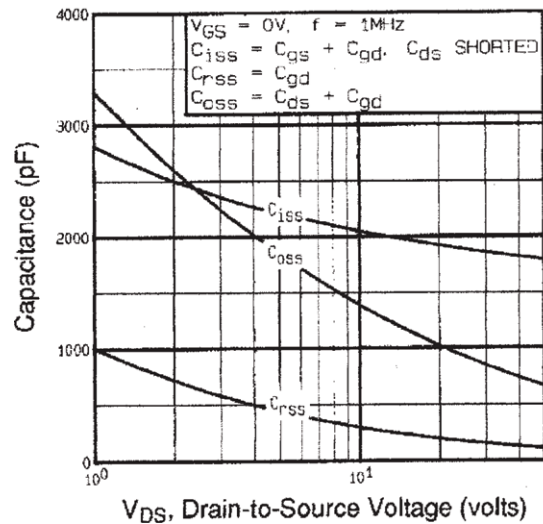


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

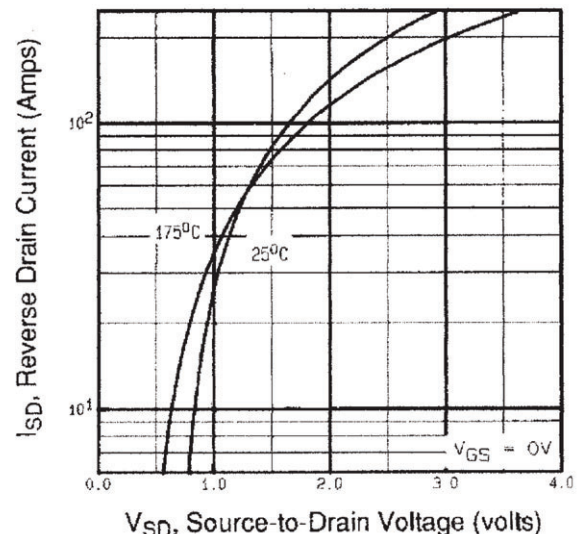


Fig. 7 - Typical Source-Drain Diode Forward Voltage

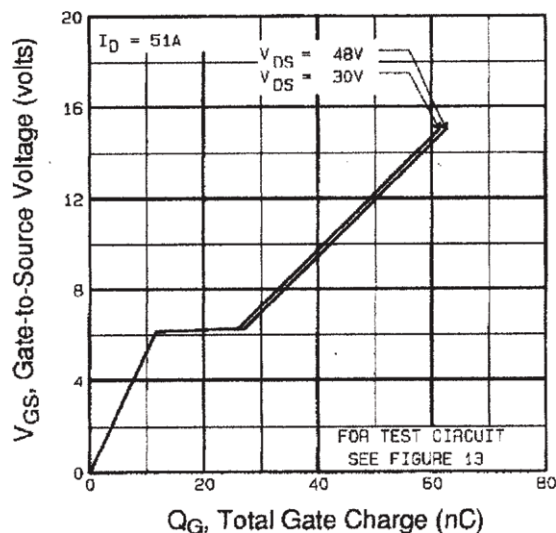


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

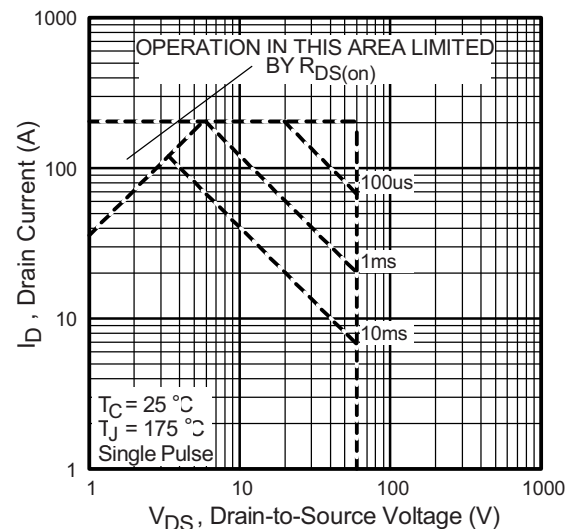


Fig. 8 - Maximum Safe Operating Area

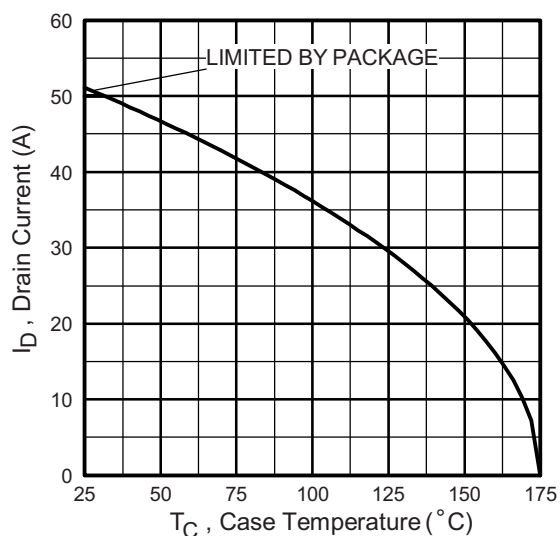
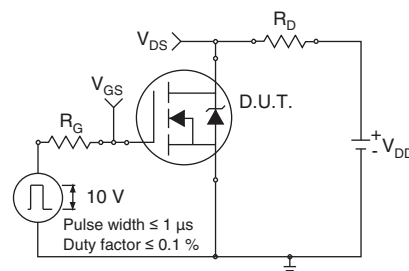
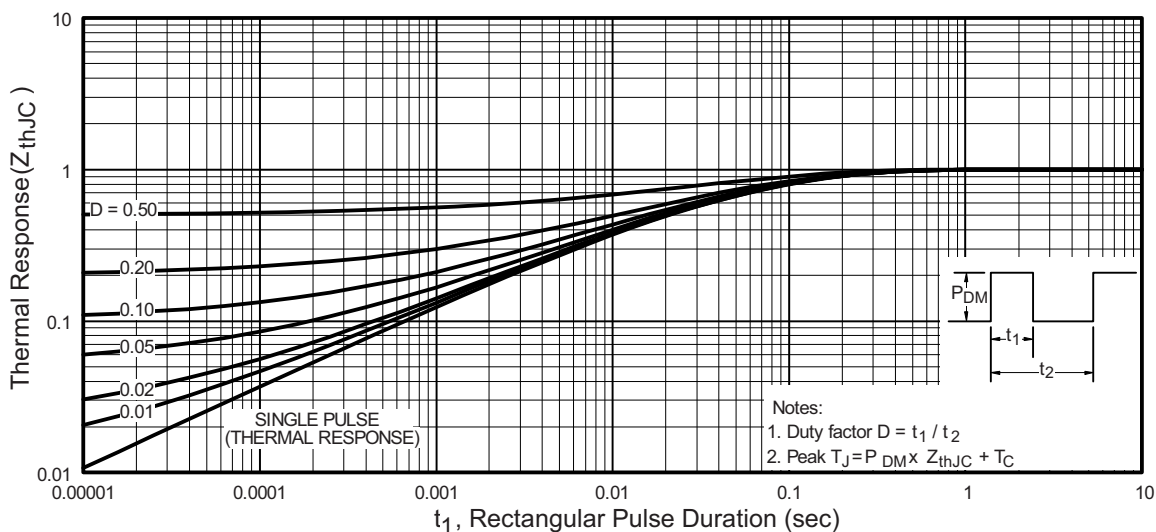
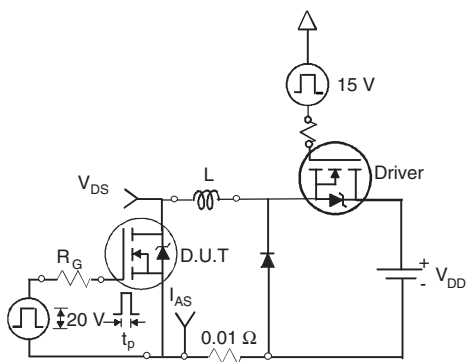
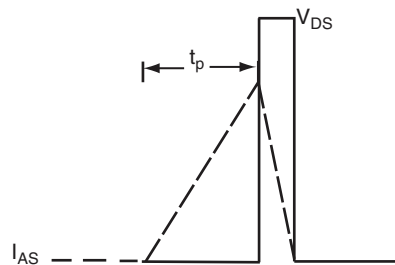
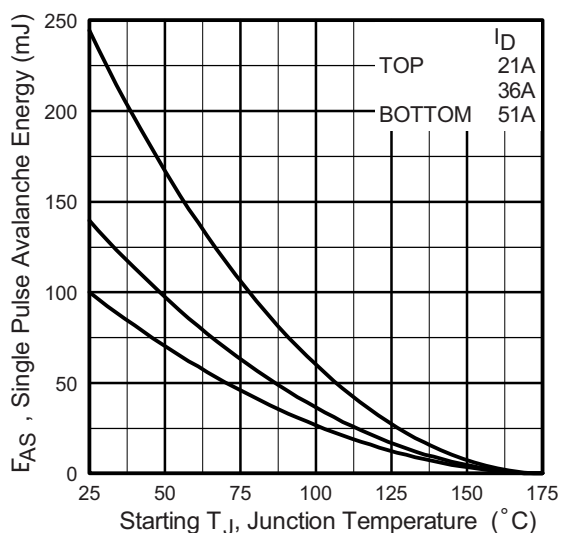
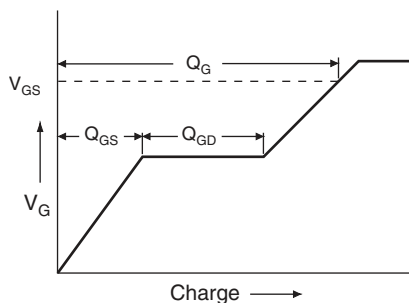
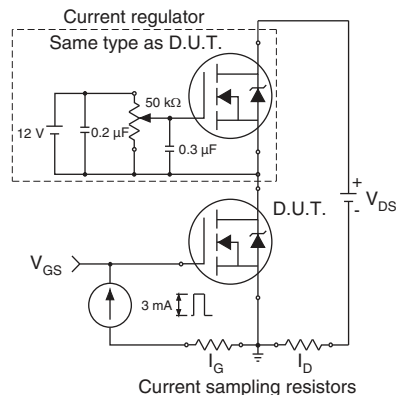
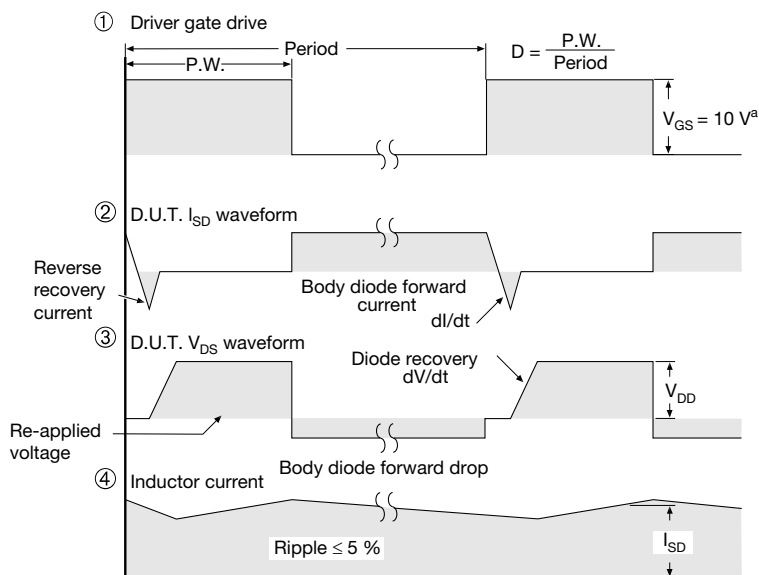
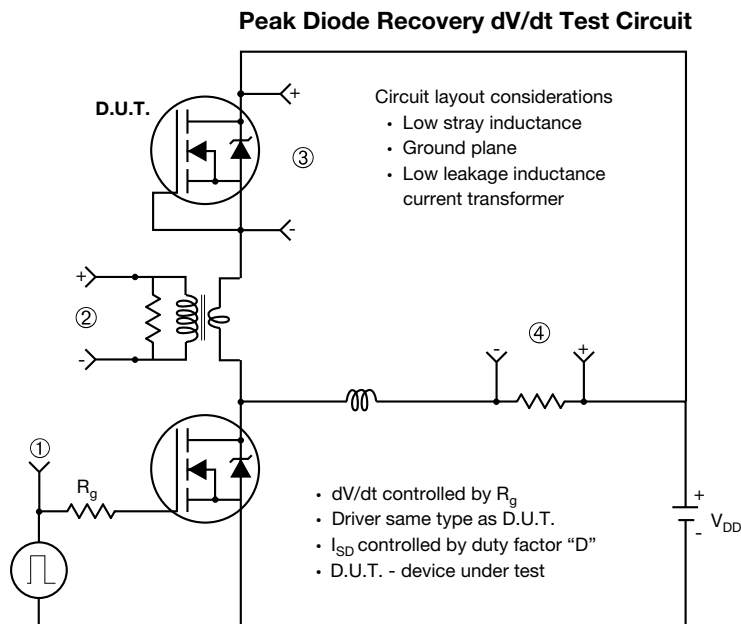

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

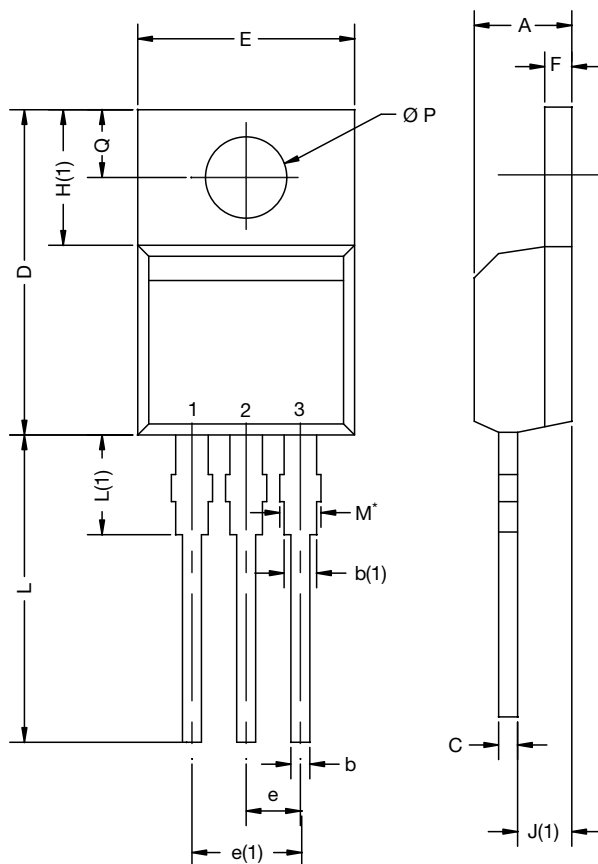

Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 11 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M^* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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