IRFBC40

Vishay Siliconix



TO-220AB

PRODUCT SUMMARY

V_{DS} (V)

R_{DS(on)} (Ω)

Q_{gs} (nC)

Q_{gd} (nC)

Q_a max. (nC)

Configuration

Power MOSFET

S

N-Channel MOSFET

1.2

600

60

8.3

30

Single

 $V_{GS} = 10 V$

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION				
Package	TO-220AB			
Lead (Pb)-free	IRFBC40PbF			
Lead (Pb)-free and halogen-free	IRFBC40PbF-BE3			

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	600	v	
Gate-source voltage			V _{GS}	± 20	V	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C		6.2		
		T _C = 100 °C	I _D	3.9	А	
Pulsed drain current ^a			I _{DM}	25		
Linear derating factor				1.0	W/°C	
Single pulse avalanche energy ^b			E _{AS}	570	mJ	
Repetitive avalanche current ^a			I _{AR}	6.2	А	
Repetitive avalanche energy ^a			E _{AR}	13	mJ	
Maximum power dissipation	T _C = 25 °C		PD	125	W	
Peak diode recovery dV/dt ^c			dV/dt	3.0	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^d	For 10 s			300		
Mounting torque	6-32 or M3 screw			10	lbf ∙ in	
Mounting torque				1.1	N · m	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 27 mH, R_g = 25 Ω , I_{AS} = 6.2 A (see fig. 12)

c. $I_{SD} \le 6.2$ A, dI/dt ≤ 80 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C

S21-0868-Rev. C, 16-Aug-2021

1



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THERMAL RESISTANCE RATI	NGS							
PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum junction-to-ambient	R _{thJA}	-		62				
Case-to-sink, flat, greased surface	R _{thCS}	0.50 -			°C/W			
Maximum junction-to-case (drain)	R _{thJC}	-		1.0		-		
	•	·						
SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$, u	Inless otherwi	ise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	I							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0	V, I _D = 2	50 µA	600	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference t			-	0.7	-	V/°C
Gate-source threshold voltage	V _{GS(th)}		_{3S} , I _D = 2		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	-	$s_{3} = \pm 20$	-	-	-	± 100	nA
		$V_{DS} = 600 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$		-	-	100		
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V, V			-	-	500	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V		₀ = 3.7A ^b	-	-	1.2	Ω
Forward transconductance	9fs	V _{DS} = 10	0 V, I _D =	3.7 A ^b	4.7	-	-	S
Dynamic						1	1	
Input capacitance	C _{iss}	$V_{GS} = 0 V$,		-	1300	-		
Output capacitance	C _{oss}		$V_{GS} = 0.V,$ $V_{DS} = 25 V,$ f = 1.0 MHz, see fig. 5		-	160	-	рF
Reverse transfer capacitance	C _{rss}	f = 1.0 M			-	30	-	
Total gate charge	Qg				-	-	60	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V} \qquad \begin{array}{c} I_{D} = 6.2 \text{ A}, V_{DS} = 360 \text{ V},\\ \text{see fig. 6 and } 13^{\text{ b}} \end{array}$		-	-	8.3	nC
Gate-drain charge	Q _{gd}				-	-	30	
Turn-on delay time	t _{d(on)}		•		-	13	-	
Rise time	t _r	V _{DD} = 30	0 V, I _D =	6.2 A,	-	18	-	
Turn-off delay time	t _{d(off)}		$R_{g} = 9.1 \ \Omega, R_{D} = 47 \ \Omega, \text{ see fig. 10}^{b}$		-	55	-	ns
Fall time	t _f			-	20	-	1	
Gate input resistance	R _g	f = 1 M	Hz, open	drain	0.3	-	3.9	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-		
Internal source inductance	Ls			-	7.5	-	nH	
Drain-Source Body Diode Characteristic	cs							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.2	Δ	
Pulsed diode forward current ^a	I _{SM}			-	-	25	A	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S	= 6.2 A,	V _{GS} = 0 V ^b	-	-	1.5	V
Body diode reverse recovery time	t _{rr}	- T _J = 25 °C, I _F = 6.2 A, dl/dt = 100 A/µs ^b		-	450	940	ns	
Body diode reverse recovery charge	Q _{rr}			-	3.8	7.9	μC	
Forward turn-on time	t _{on}	Intrinsic turn-	on time i	s negligible (turn	-on is doi	minated b	y L _S and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

2



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

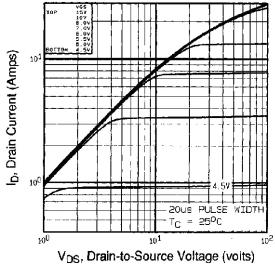


Fig. 1 - Typical Output Characteristics, $T_C = 25 \ ^{\circ}C$

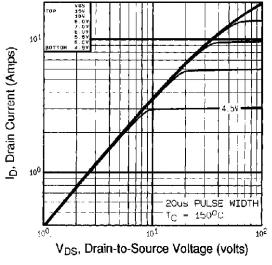
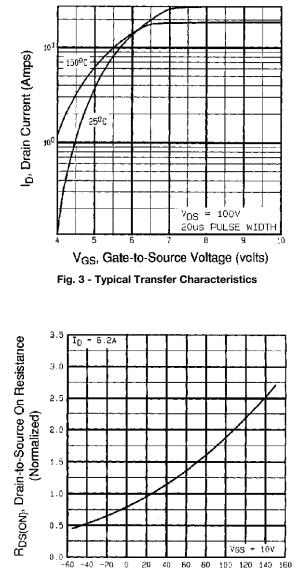


Fig. 2 - Typical Output Characteristics, T_C = 150 °C



T_.I, Junction Temperature (°C)

Fig. 4 - Normalized On-Resistance vs. Temperature

3



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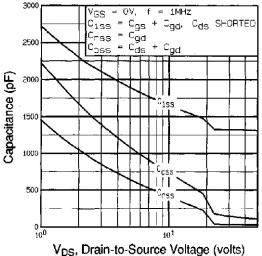


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

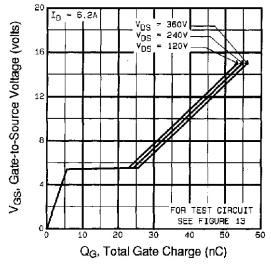


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

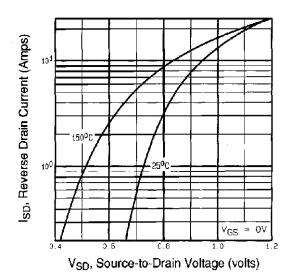


Fig. 7 - Typical Source-Drain Diode Forward Voltage

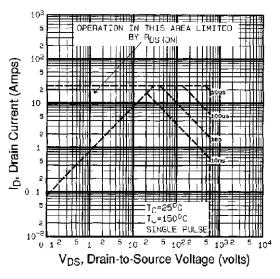


Fig. 8 - Maximum Safe Operating Area

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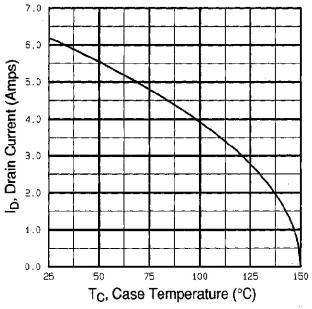


Fig. 9 - Maximum Drain Current vs. Case Temperature

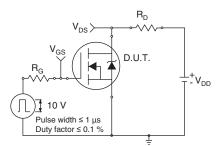


Fig. 10a - Switching Time Test Circuit

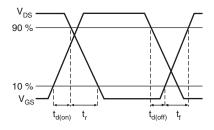


Fig. 10b - Switching Time Waveforms

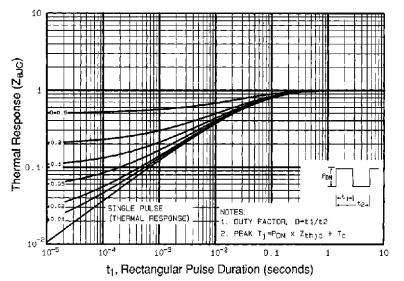


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

5



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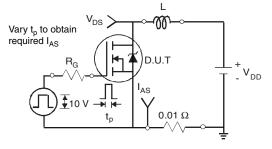


Fig. 12a - Unclamped Inductive Test Circuit

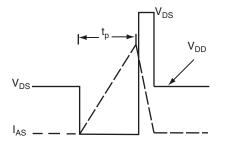


Fig. 12b - Unclamped Inductive Waveforms

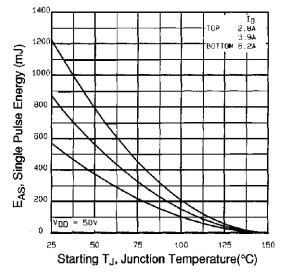


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

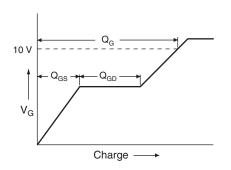


Fig. 13a - Basic Gate Charge Waveform

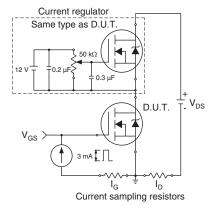


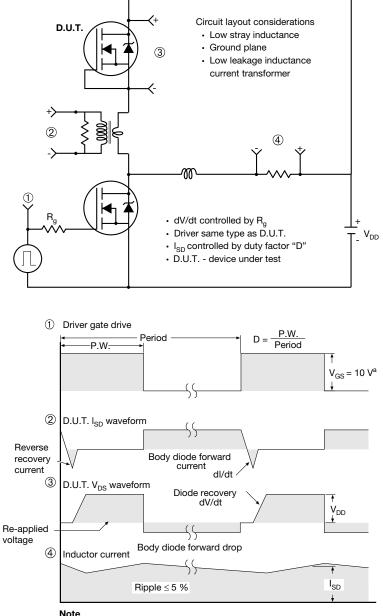
Fig. 13b - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit



a. $V_{GS} = 5$ V for logic level devices

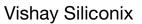
Fig. 14 - For N-Channel

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SHAY

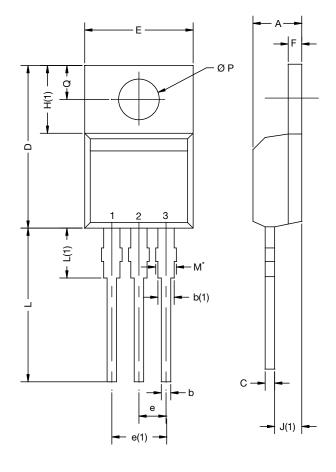
7

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TO-220-1



DIM.	MILLIN	IETERS	INCHES		
DIN.	MIN.	MAX.	MIN.	MAX.	
А	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

- M^{\star} = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture						
AS	3E	Xi'an				
		IRF 9510 744K AB				

Revison: 14-Dec-15

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