Vishay Siliconix



TO-220AB

PRODUCT SUMMARY

V_{DS} (V)

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}\left(\Omega\right)$

Q_{gs} (nC)

Q_{gd} (nC)

Q_q (Max.) (nC)

Configuration

Power MOSFET

FEATURES

Low gate charge Q_g results in simple drive requirement



- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective Coss specified
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Two transistor forward
- Half bridge
- Full bridge

ORDERING INFORMATION				
Package	TO-220AB			
Lead (Pb)-free	IRF820APbF			
Lead (Pb)-free and halogen-free	IRF820APbF-BE3			

ABSOLUTE MAXIMUM RATINGS ($T_c = 25 \degree C$, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	500	V	
Gate-source voltage			V _{GS}	± 30	V	
Continuous drain surrant	V =======	T _C = 25 °C	Ι _D	2.5		
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C		1.6	A	
Pulsed drain current ^a			I _{DM}	10		
Linear derating factor				0.40	W/°C	
Single pulse avalanche energy ^b			E _{AS}	140	mJ	
Repetitive avalanche current ^a			I _{AR}	2.5	А	
Repetitive avalanche energy ^a			E _{AR}	5.0	mJ	
Maximum power dissipation	$T_{\rm C} = 25 ^{\circ}{\rm C}$		PD	50	W	
Peak diode recovery dV/dt ^c			dV/dt	3.4	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^d	For 10 s		Č .	300 ^d	1	
	6-32 or M3 screw			10	lbf ∙ in	
Mounting torque				1.1	N · m	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Starting T_J = 25 °C, L = 45 mH, R_g = 25 $\Omega,$ I_{AS} = 2.5 A (see fig. 12)

c. $I_{SD} \le 2.5$ A, dl/dt ≤ 270 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C

d. 1.6 mm from case

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S

N-Channel MOSFET

3.0

500

17

4.3

8.5

Single

 $V_{GS} = 10 V$

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THERMAL RESISTANCE RATINGS								
PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum junction-to-ambient	R _{thJA}	-		62 - 2.5				
Case-to-sink, flat, greased surface	R _{thCS}	0.50				°C/W		
Maximum junction-to-case (drain)	R _{thJC}	-						
		·						
SPECIFICATIONS (T _J = 25 $^{\circ}$ C, u	unless otherwi	ise noted)						
PARAMETER	SYMBOL	TEST	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static								•
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 2	50 µA	500	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference t	to 25 °C,	I _D = 1 mA	-	0.60	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V	_{GS} , I _D = 2	50 µA	2.0	-	4.5	V
Gate-source leakage	I _{GSS}	V _G	s = ± 30 \	V	-	-	± 100	nA
		$V_{DS} = 5$	00 V, V _{GS}	= 0 V	-	-	25	
Zero gate voltage drain current	IDSS	V _{DS} = 400 V, V	V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	١ _D	₀ = 1.5 A ^b	-	-	3.0	Ω
Forward transconductance	9 _{fs}	V _{DS} = 5	0 V, I _D = ⁻	1.5 A ^b	1.4	-	-	S
Dynamic		•						
Input capacitance	C _{iss}	V	N 0.V		-	340	-	
Output capacitance	C _{oss}	$V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 \text{ MHz}, \text{ see fig. 5}$		-	53	-	pF	
Reverse transfer capacitance	C _{rss}			-	2.7	-		
Output capacitance	C _{oss}				490			
Output capacitance	C _{oss}	$V_{GS} = 0 \text{ V}; V_{DS} = 400 \text{ V}, \text{ f} = 1.0 \text{ MHz}$			15			
Effective output capacitance	C _{oss} eff.	V_{GS} = 0 V; V_{DS} = 0 V to 400 V ^c			28			
Total gate charge	Qg			2.5 A, V _{DS} = 400 V, e fig. 6 and 13 ^b	-	-	17	nC
Gate-source charge	Q _{gs}	$V_{GS} = 10 V$			-	-	4.3	
Gate-drain charge	Q _{gd}		see lig. 6 and 13		-	-	8.5	1
Turn-on delay time	t _{d(on)}				-	8.1	-	
Rise time	tr	Van - 24	50 V In -	254	-	12	-	1
Turn-Off delay time	t _{d(off)}	$V_{DD} = 250 \text{ V}, \text{ I}_D = 2.5 \text{ A},$ $\text{R}_\text{g} = 21 \ \Omega, \text{ R}_\text{D} = 97 \ \Omega, \text{ see fig. } 10^\text{b}$		-	16	-	ns	
Fall time	t _f			-	13	-		
Drain-Source Body Diode Characteristic	cs					•	•	
Continuous source-drain diode current	١ _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.5	А	
Pulsed diode forward current ^a	I _{SM}			-	-	10		
Body diode voltage	V _{SD}	$T_{J} = 25 \text{ °C}, I_{S} = 2.5 \text{ A}, V_{GS} = 0 \text{ V}^{b}$		-	-	1.6	V	
Body diode reverse recovery time	t _{rr}	T 25 °C L - 4	25 A J/	dt - 100 A/uch	-	330	500	ns
Body diode reverse recovery charge	Q _{rr}	- T _J = 25 °C, I _F = 2.5 A, dl/dt = 100 A/µs ^b		-	760	1140	nC	
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-o			-on is do	η is dominated by L _S and L _D)		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

c. $C_{\rm OSS}$ eff. is a fixed capacitance that gives the same charging time as $C_{\rm OSS}$ while $V_{\rm DS}$ is rising from 0 % to 80 % $V_{\rm DS}$

2



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

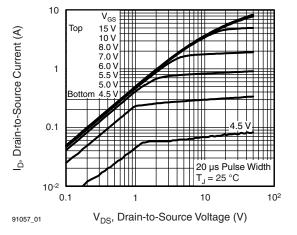


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

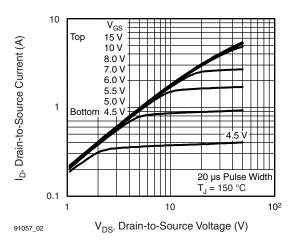


Fig. 2 - Typical Output Characteristics, $T_C = 150 \ ^\circ C$

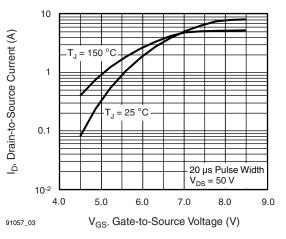


Fig. 3 - Typical Transfer Characteristics

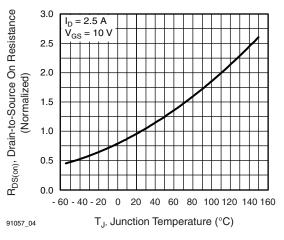


Fig. 4 - Normalized On-Resistance vs. Temperature

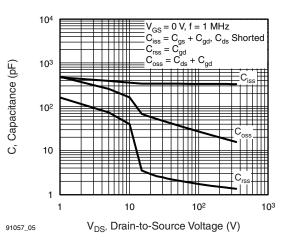


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

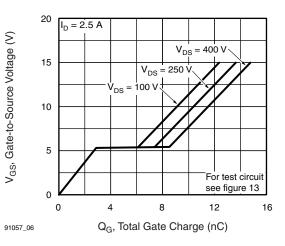


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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3 For technical questions, contact: <u>hvm@vishay.com</u> Document Number: 91057

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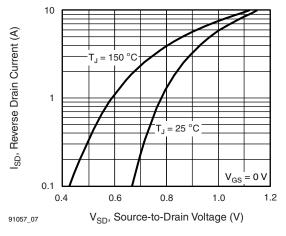


Fig. 7 - Typical Source-Drain Diode Forward Voltage

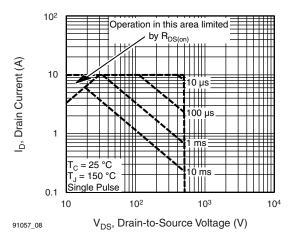


Fig. 8 - Maximum Safe Operating Area

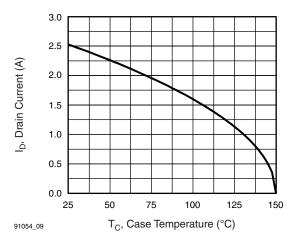


Fig. 9 - Maximum Drain Current vs. Case Temperature

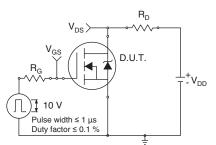


Fig. 10 - Switching Time Test Circuit

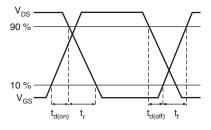


Fig. 11 - Switching Time Waveforms

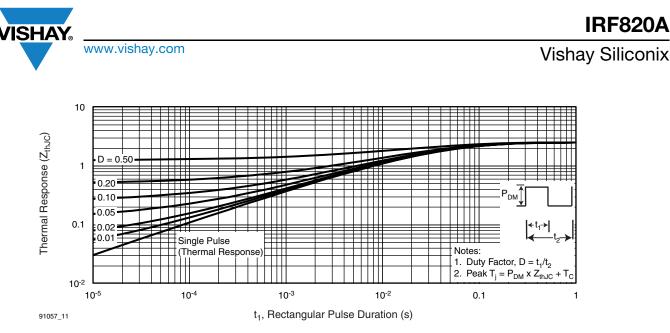


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

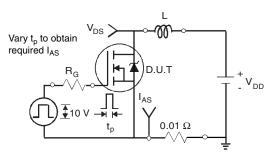


Fig. 13 - Unclamped Inductive Test Circuit

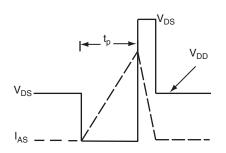


Fig. 14 - Unclamped Inductive Waveforms

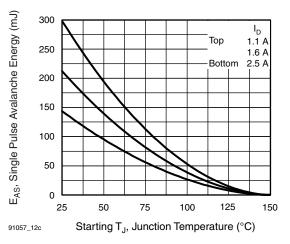


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

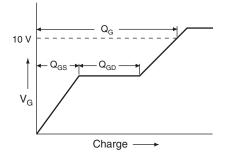
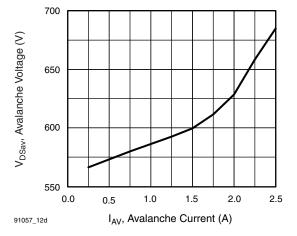


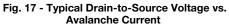
Fig. 16 - Basic Gate Charge Waveform

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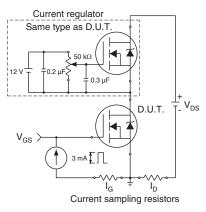
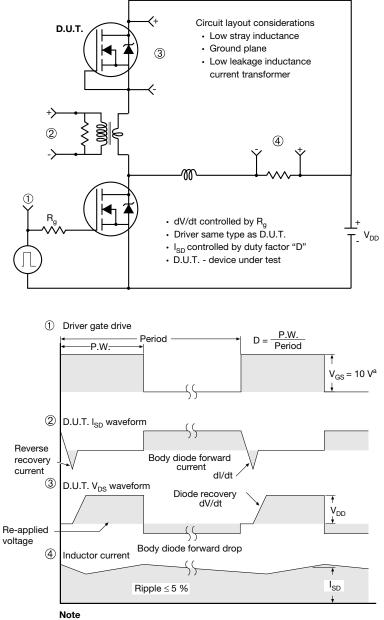


Fig. 18 - Gate Charge Test Circuit





Peak Diode Recovery dV/dt Test Circuit



a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91057.



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TO-220-1



DIM.	MILLIN	IETERS	INCHES		
DIN.	MIN.	MAX.	MIN.	MAX.	
А	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

- M^{\star} = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture						
AS	3E	Xi'an				
		IRF 9510 744K AB				

Revison: 14-Dec-15

1 For technical questions, contact: <u>hvm@vishay.com</u> Document Number: 66542

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