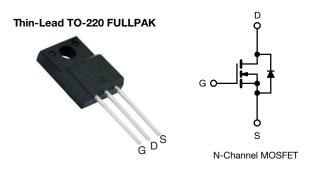
# SiHA22N60AE

**Vishay Siliconix** 



## **E Series Power MOSFET**



PRODUCT SUMMARY					
V <sub>DS</sub> (V) at T <sub>J</sub> max.	650				
R <sub>DS(on)</sub> typ. (Ω) at 25 °C	V <sub>GS</sub> = 10 V 0.156				
Q <sub>g</sub> max. (nC)	96				
Q <sub>gs</sub> (nC)	12				
Q <sub>gd</sub> (nC)	25				
Configuration	Single				

## **FEATURES**

- Low figure-of-merit (FOM) Ron x Qa
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q<sub>q</sub>)
- Avalanche energy rated (UIS)
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

### **APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION				
Package	Thin-Lead TO-220 FULLPAK			
Lead (Pb)-free	SiHA22N60AE-E3			
Lead (Pb)-free and halogen-free	SiHA22N60AE-GE3			

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \text{ °C}$ , unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V <sub>DS</sub>	600	V	
Gate-source voltage			V <sub>GS</sub>	± 30	V	
Continuous drain surrent $(T_{1} - 150 \circ C)^{6}$	V at 10 V	$T_{\rm C} = 25 \ ^{\circ}{\rm C}$ $T_{\rm C} = 100 \ ^{\circ}{\rm C}$		8		
Continuous drain current ( $T_J = 150 \text{ °C}$ ) <sup>e</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	5	A	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	49	1	
Linear derating factor				0.26	W/°C	
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	204	mJ	
Maximum power dissipation			P <sub>D</sub>	33	W	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Drain-source voltage slope	T <sub>J</sub> = 125 °C		d\//d+	70	N//mm	
Reverse diode dV/dt <sup>d</sup>			dV/dt	31	V/ns	
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s			300	°C	
Mounting torque	M3 screw			0.6	Nm	

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

- b.  $V_{DD}$  = 140 V, starting T<sub>J</sub> = 25 °C, L = 28.2 mH, R<sub>q</sub> = 25  $\Omega$ , I<sub>AS</sub> = 3.8 A
- c. 1.6 mm from case
- d.  $I_{SD} \leq I_D$ , dI/dt = 100 A/µs, starting  $T_J = 25 \text{ °C}$

e. Limited by maximum junction temperature

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PARAMETER	SYMBOL	TYP.		MAX.			UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-		65		*CAN		
Maximum junction-to-case (drain)	R <sub>thJC</sub>	- 3.8			- °C/W			
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 $^{\circ}$ C,	unless otherw	ise noted)						
PARAMETER	SYMBOL	TES	T CONDITIO	NS	MIN.	TYP.	MAX.	UNI
Static								
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	: 0 V, I <sub>D</sub> = 250	) μA	600	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I <sub>D</sub> :	= 250 μA	-	0.72	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 25	0 μΑ	2	-	4	V
Gate-source leakage	1		$V_{GS} = \pm 20 V$		-	-	± 100	nA
Gale-Source leakage	I <sub>GSS</sub>		$V_{GS} = \pm 30 V$		-	-	± 1	μA
Zere gete veltage drein ourrent	I	V <sub>DS</sub> =	= 600 V, V <sub>GS</sub> =	= 0 V	-	-	1	μA
Zero gate voltage drain current	IDSS	V <sub>DS</sub> = 480 \	/, V <sub>GS</sub> = 0 V, <sup>-</sup>	Г <sub>Ј</sub> = 125 °С	-	-	10	
Drain-source on-state resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	I <sub>D</sub> =	= 11 A	-	0.156	0.180	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub>	= 30 V, I <sub>D</sub> = 1	1 A	-	4.8	-	S
Dynamic	•	•			•	•	•	
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 V,$ $V_{DS} = 100 V,$ f = 1 MHz		-	1451	-	pF	
Output capacitance	C <sub>oss</sub>			-	73	-		
Reverse transfer capacitance	C <sub>rss</sub>			-	5	-		
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	$V_{DS} = 0$ V to 480 V, $V_{GS} = 0$ V		-	50	-		
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	258	-		
Total gate charge	Qg				-	48	96	1
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V I <sub>D</sub> = 11 A, V <sub>DS</sub> = 480 V		-	12	-	nC	
Gate-drain charge	Q <sub>gd</sub>				-	25	-	1
Turn-on delay time	t <sub>d(on)</sub>				-	19	38	
Rise time	t <sub>r</sub>		-		-	33	66	1
Turn-off delay time	t <sub>d(off)</sub>	$V_{DD} = 480 \text{ V}, \text{ I}_D = 11 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_g = 9.1 \Omega$		-	45	90	- ns	
Fall time	t <sub>f</sub>			-	21	42		
Gate input resistance	Rg	f = 1 MHz, open drain		0.3	0.6	1.2	Ω	
Drain-Source Body Diode Characterist								
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20		
Pulsed diode forward current	I <sub>SM</sub>			-	-	49	A	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 11 A, V <sub>GS</sub> = 0 V		-	-	1.2	V	
Reverse recovery Time	t <sub>rr</sub>	$T_{J} = 25 \text{ °C}, I_{F} = I_{S} = 11 \text{ A},$ dl/dt = 100 A/µs, V <sub>R</sub> = 25 V		-	319	638	ns	
Reverse recovery charge	Q <sub>rr</sub>			-	4.9	9.8	μC	
,	-11			L	28		A	

#### Notes

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ 

b. Coss(tr) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 % to 80 % VDSS



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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

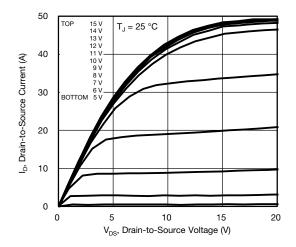


Fig. 1 - Typical Output Characteristics

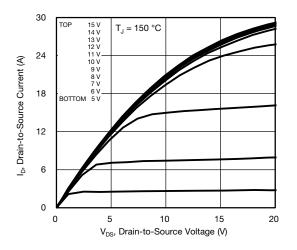


Fig. 2 - Typical Output Characteristics

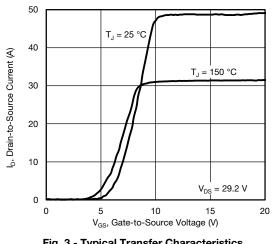


Fig. 3 - Typical Transfer Characteristics

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3.0 = 11 A R<sub>DS(on)</sub>, Drain-to-Source On-Resistance 2.5 2.0 (Normalized) 1.5 1.0 10 \ GS 0.5 0 -20 -60 -40 20 40 60 80 100 120 140 160 0 T<sub>J</sub>, Junction Temperature (°C)

Fig. 4 - Normalized On-Resistance vs. Temperature

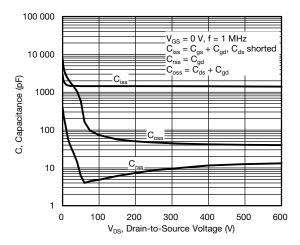


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

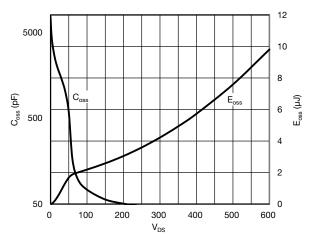


Fig. 6 - Coss and Eoss vs. VDS

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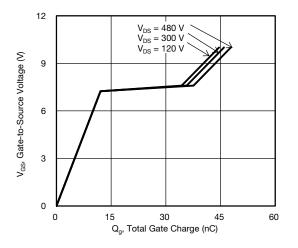


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

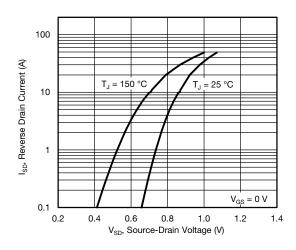


Fig. 8 - Typical Source-Drain Diode Forward Voltage

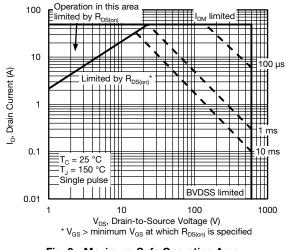


Fig. 9 - Maximum Safe Operating Area

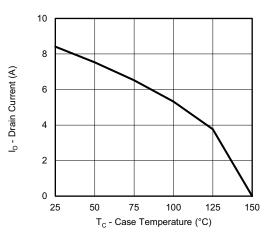


Fig. 10 - Maximum Drain Current vs. Case Temperature

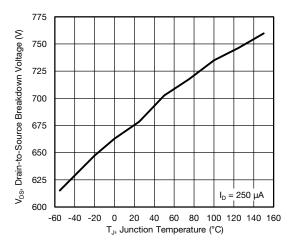
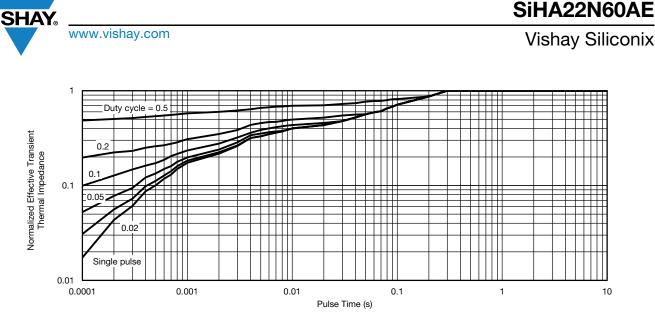


Fig. 11 - Temperature vs. Drain-to-Source Voltage

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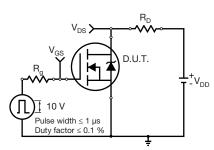


Fig. 13 - Switching Time Test Circuit

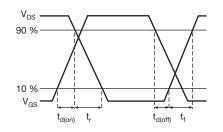


Fig. 14 - Switching Time Waveforms

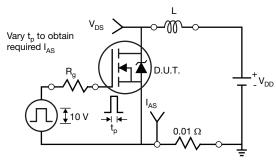


Fig. 15 - Unclamped Inductive Test Circuit

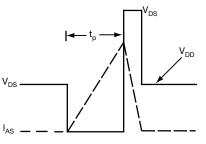


Fig. 16 - Unclamped Inductive Waveforms

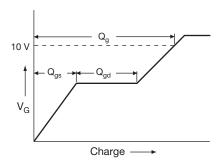


Fig. 17 - Basic Gate Charge Waveform

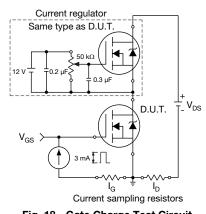
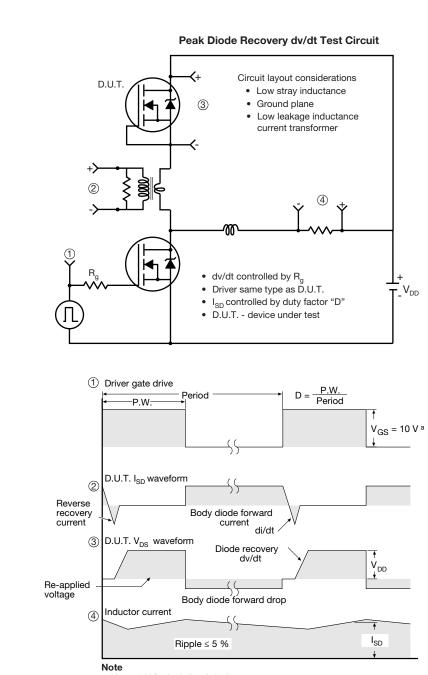


Fig. 18 - Gate Charge Test Circuit

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a.  $V_{GS} = 5$  V for logic level devices

Fig. 19 - For N-Channel

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# **TO-220 FULLPAK Thin Lead**





	DIMENSIONS						
SYMBOL	MILLIN	METERS	INC	HES			
	MIN.	MAX.	MIN.	MAX.			
А	4.30	4.70	0.169	0.185			
A1	2.50	2.90	0.098	0.114			
A2	2.40	2.80	0.094	0.110			
b	0.60	0.80	0.024	0.031			
b2	0.60	0.90	0.024	0.035			
С	-	0.60	-	0.024			
D	8.30	8.70	0.327	0.342			
d1	14.70	15.30	0.579	0.602			
d2	2.90	3.10	0.114	0.122			
d3	3.30	3.70	0.130	0.146			
E	9.70	10.30	0.382	0.406			
е	2.50	2.70	0.098	0.106			
L	13.40	13.80	0.528	0.543			
L1	1.00	2.80	0.039	0.110			
ØP	3.00	3.40	0.118	0.134			
ECN: E20-0684-Rev. D, 28 DWG: 6021	3-Dec-2020	·	·				

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