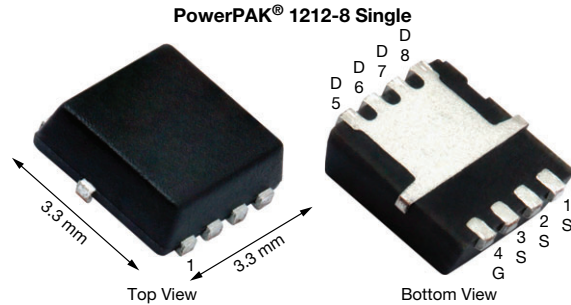


## N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	30
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0075
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0124
$Q_g$ typ. (nC)	6.9
$I_D$ (A) <sup>f</sup>	38.3
Configuration	Single

### FEATURES

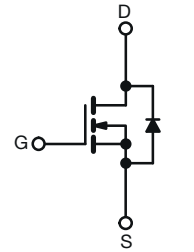
- TrenchFET<sup>®</sup> Gen IV power MOSFET
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- DC/DC power supplies
- High current power rails in computing
- Telecom POL and bricks
- Battery protection



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiS472BDN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	30	V
Gate-source voltage		$V_{GS}$	+20, -16	
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	38.3	A
	$T_C = 70$ °C		30.6	
	$T_A = 25$ °C		15.3 <sup>a, b</sup>	
	$T_A = 70$ °C		12.1 <sup>a, b</sup>	
Pulsed drain current ( $t = 300$ $\mu$ s)		$I_{DM}$	70	A
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	18	
	$T_A = 25$ °C		2.9 <sup>a, b</sup>	
Single pulse avalanche current	L = 0.1 mH	$I_{AS}$	10	mJ
Single pulse avalanche energy		$E_{AS}$	5	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	19.8	W
	$T_C = 70$ °C		12.7	
	$T_A = 25$ °C		3.2 <sup>a, b</sup>	
	$T_A = 70$ °C		3 <sup>a, b</sup>	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c, d</sup>			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a, e</sup>	$t \leq 10$ s	$R_{thJA}$	31	39	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	5	6.3	

### Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 81 °C/W
- Based on  $T_C = 25$  °C



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	18.5	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.2	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2	-	2.4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.0060	0.0075	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$	-	0.0096	0.0124	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	-	54	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{ISS}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1000	-	pF
Output capacitance	$C_{OSS}$		-	287	-	
Reverse transfer capacitance	$C_{RSS}$		-	34	-	
$C_{RSS}/C_{ISS}$ ratio			-	0.034	0.068	
Total gate charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	14.3	21.5	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	6.9	10.5	
Gate-source charge	$Q_{gs}$		-	2.8	-	
Gate-drain charge	$Q_{gd}$		-	1.6	-	
Output charge	$Q_{OSS}$		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	-	7.8	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.4	1.6	3.2	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	15	30	ns
Rise time	$t_r$		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	$t_f$		-	7	14	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	11	22	
Rise time	$t_r$		-	9	18	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	$t_f$		-	5	10	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	18	A
Pulse diode forward current	$I_{SM}$		-	-	70	
Body diode voltage	$V_{SD}$	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	-	0.77	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	19	35	ns
Body diode reverse recovery charge	$Q_{rr}$		-	7	14	nC
Reverse recovery fall time	$t_a$		-	10	-	ns
Reverse recovery rise time	$t_b$		-	9	-	

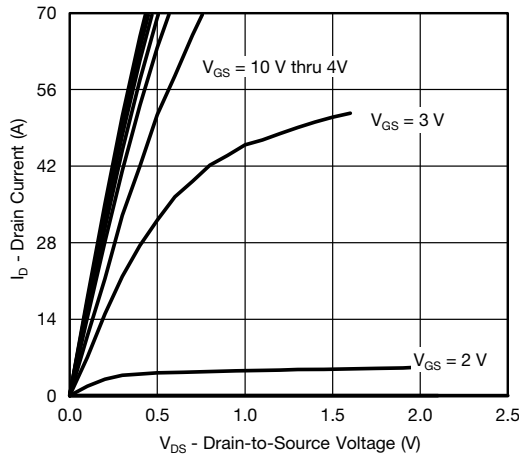
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

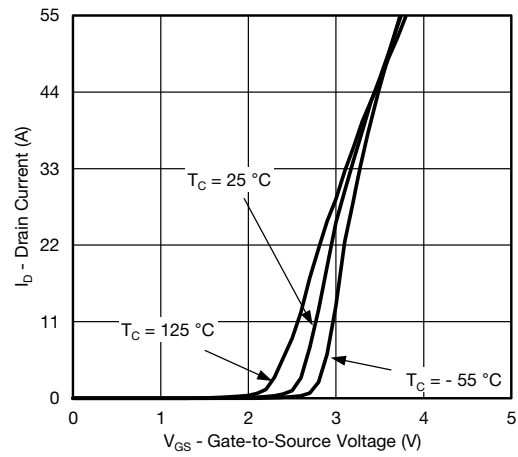
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



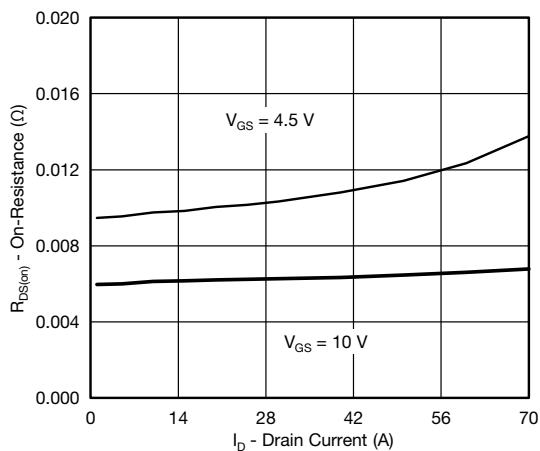
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



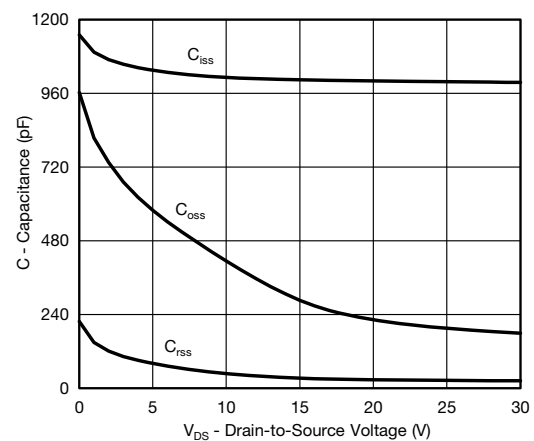
Output Characteristics



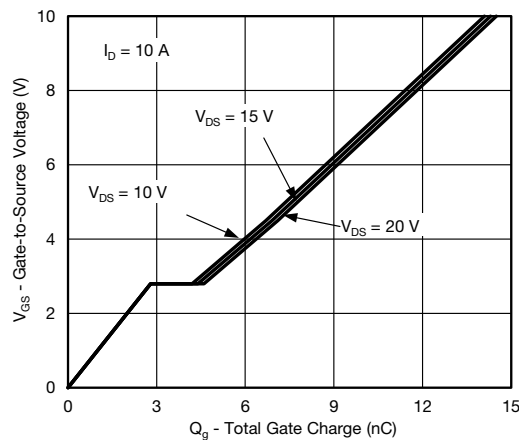
Transfer Characteristics



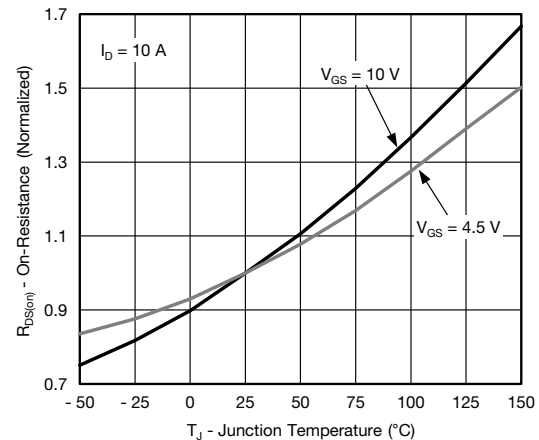
On-Resistance vs. Drain Current



Capacitance



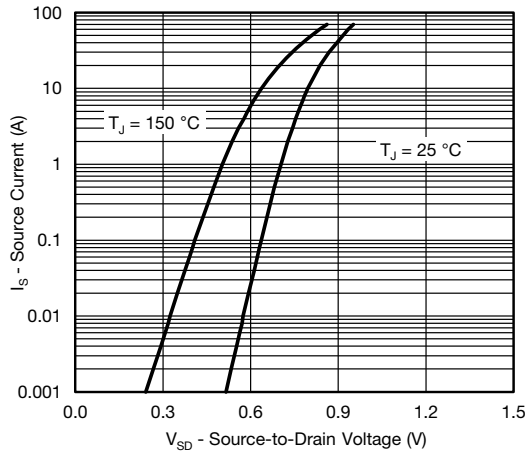
Gate Charge



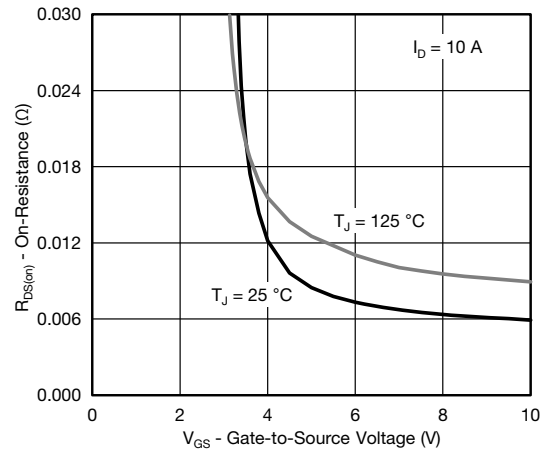
On-Resistance vs. Junction Temperature



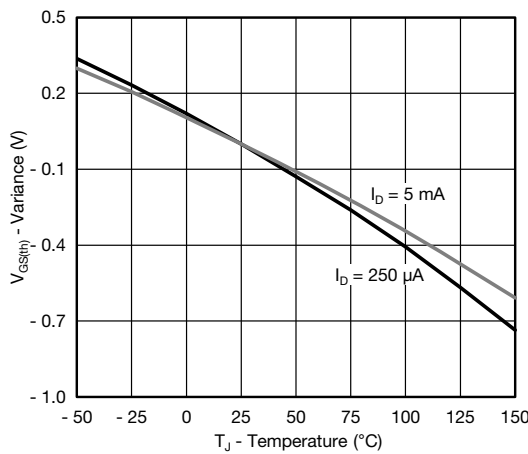
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



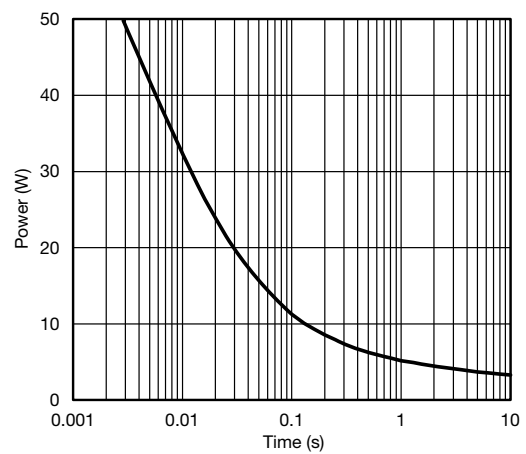
Source-Drain Diode Forward Voltage



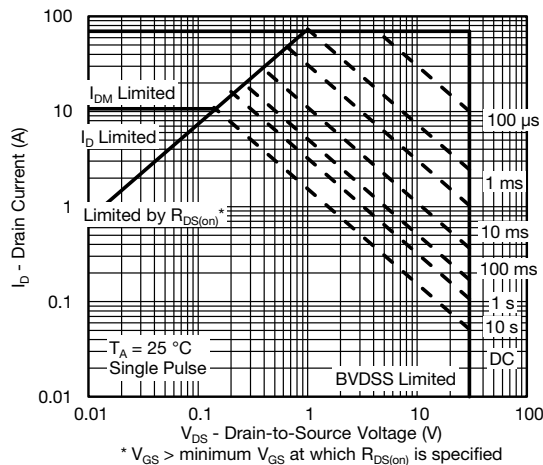
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



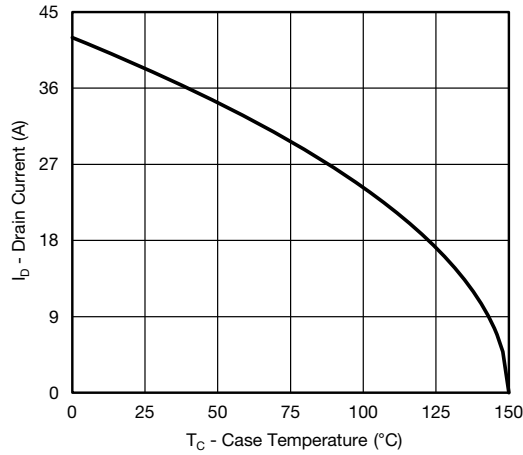
Single Pulse Power, Junction-to-Ambient



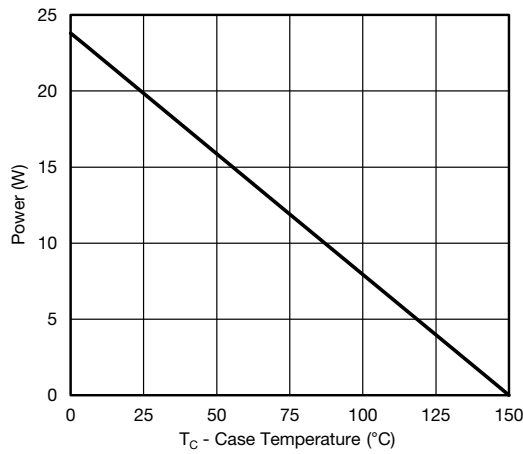
Safe Operating Area, Junction-to-Ambient



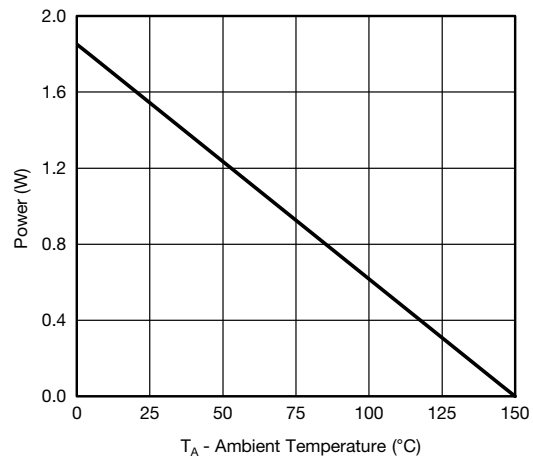
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**

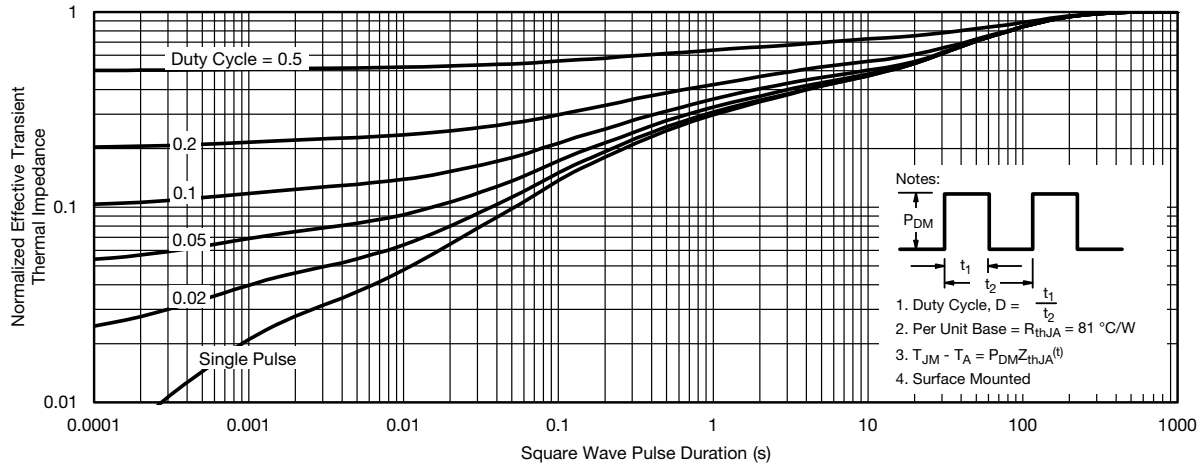


**Power, Junction-to-Ambient**

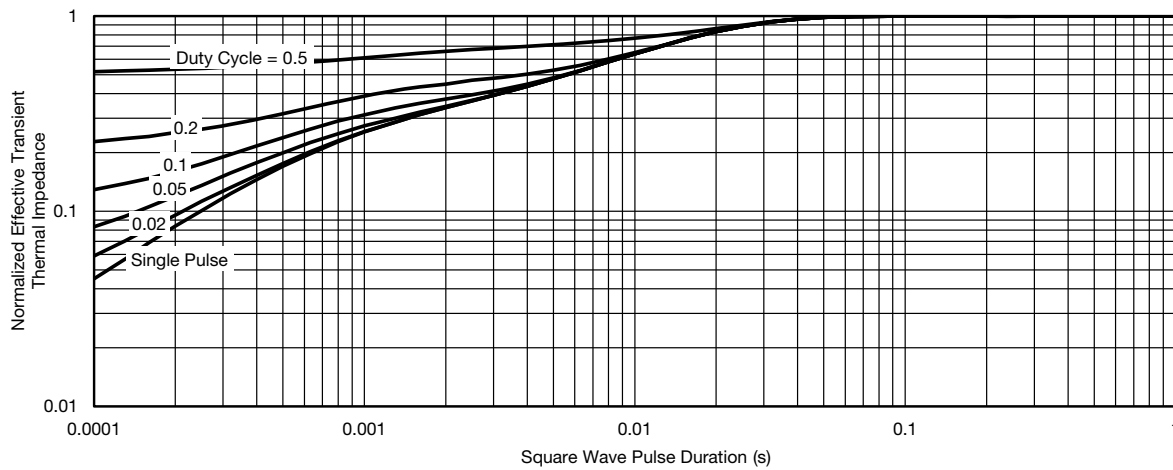
**Note**

- a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

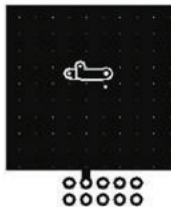
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**



a. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 130 °C/W when mounted on minimum pad of 2 oz copper.

**Notes**

- $R_{thJA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 in. x 1.5 in. board of FR4 material.  $R_{thJC}$  is guaranteed by design while  $R_{thCA}$  is determined by the user's board design.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75537](http://www.vishay.com/ppg?75537).



PowerPAK® 1212-8, (Single / Dual)



- Notes**  
 1. Inch will govern  
 [2] Dimensions exclusive of mold gate burrs  
 3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S16-2667-Rev. M, 09-Jan-17  
 DWG: 5882

## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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