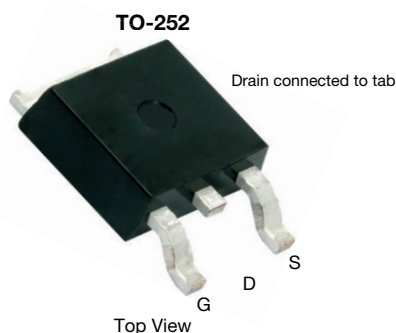


P-Channel 60 V (D-S) MOSFET



FEATURES

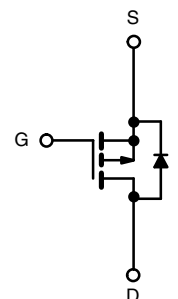
- TrenchFET® power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch



P-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.015
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.020
I_D (A) ^d	-50
Configuration	Single

ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and halogen-free	SUD50P06-15-GE3
	SUD50P06-15-T4-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_J = 175^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	-50 ^d
	$T_C = 125^\circ\text{C}$		-27.5
Pulsed drain current	I_{DM}	-80	A
Avalanche current	I_{AS}	-50	A
Single pulse avalanche energy ^a	$L = 0.1$ mH	E_{AS}	125
Power dissipation	$T_C = 25^\circ\text{C}$	P_D	113 ^c
	$T_A = 25^\circ\text{C}$		2.5 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-ambient ^b	R_{thJA}	$t \leq 10$ s	15	$^\circ\text{C/W}$
		Steady state	40	
Junction-to-case	R_{thJC}	0.82	1.1	

Notes

- Duty cycle $\leq 1\%$
- When mounted on 1" square PCB (FR4 material)
- See SOA curve for voltage derating
- Package limited



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-60	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	-3	
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 125 °C	-	-	-50	
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 150 °C	-	-	-100	
On-state drain current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-50	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -17 A	-	0.012	0.015	Ω
		V _{GS} = -10 V, I _D = -50 A, T _J = 125 °C	-	-	0.025	
		V _{GS} = -10 V, I _D = -50 A, T _J = 150 °C	-	-	0.028	
		V _{GS} = -4.5 V, I _D = -14 A	-	-	0.020	
Forward transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -17 A	-	61	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1 MHz	-	4950	-	pF
Output capacitance	C _{oss}		-	480	-	
Reverse transfer capacitance	C _{rss}		-	405	-	
Total gate charge ^c	Q _g	V _{DS} = -30 V, V _{GS} = -10 V, I _D = -50 A	-	110	165	nC
Gate-source charge ^c	Q _{gs}		-	19	-	
Gate-drain charge ^c	Q _{gd}		-	28	-	
Turn-on delay time ^c	t _{d(on)}	V _{DD} = -30 V, R _L = 0.6 Ω I _D ≅ -50 A, V _{GEN} = -10 V, R _G = 6 Ω	-	15	23	ns
Rise time ^c	t _r		-	70	105	
Turn-off delay time ^c	t _{d(off)}		-	175	260	
Fall time ^c	t _f		-	175	260	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous current	I _S		-	-	-50	A
Pulsed current	I _{SM}		-	-	-80	
Forward voltage ^a	V _{SD}	I _F = -50 A, V _{GS} = 0 V	-	-1	-1.6	V
Reverse recovery time	t _{rr}	I _F = -50 A, di/dt = 100 A/μs	-	45	70	ns

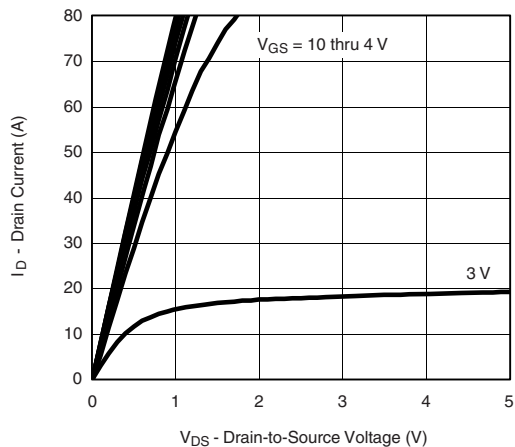
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

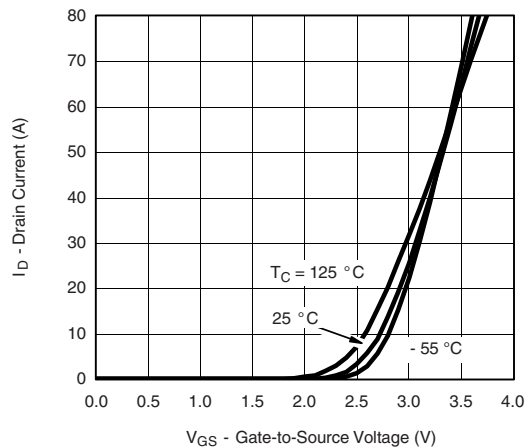
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



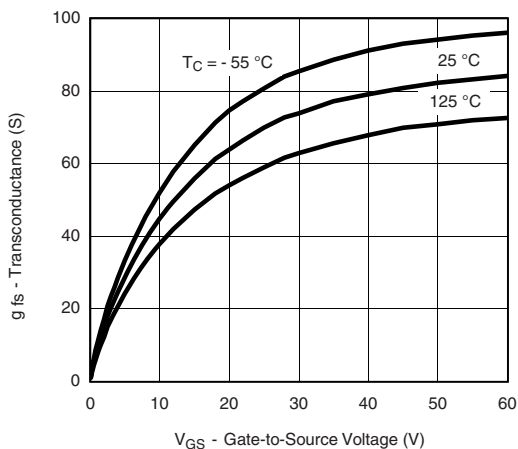
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



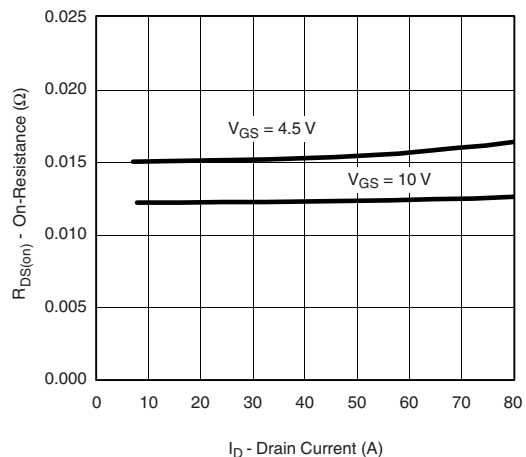
Output Characteristics



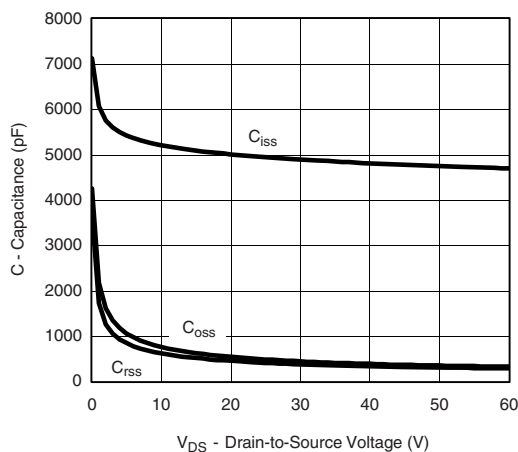
Transfer Characteristics



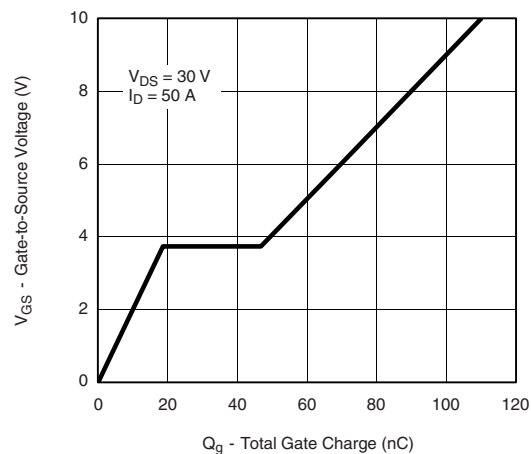
Transconductance



On-Resistance vs. Drain Current



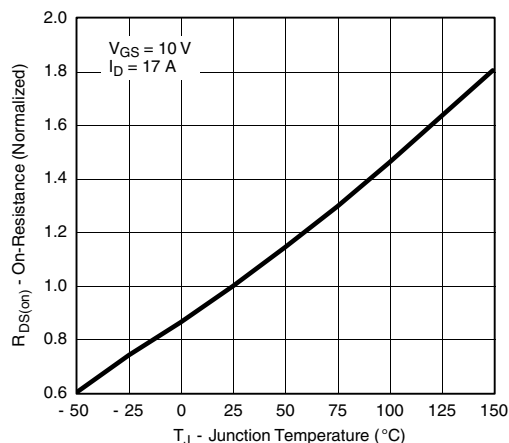
Capacitance



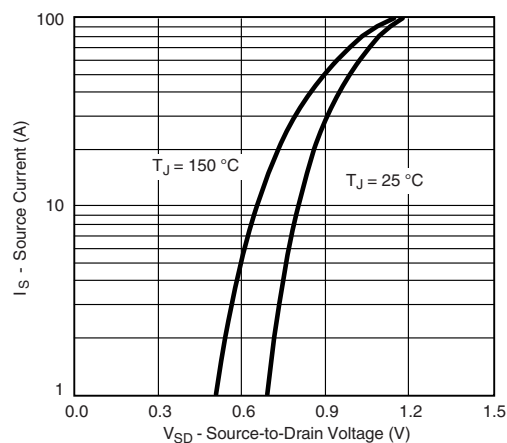
Gate Charge



TYPICAL CHARACTERISTICS

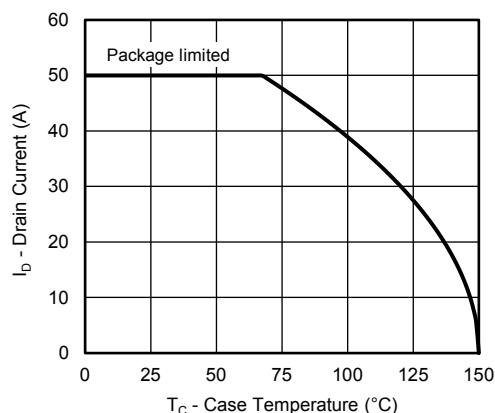


On-Resistance vs. Junction Temperature

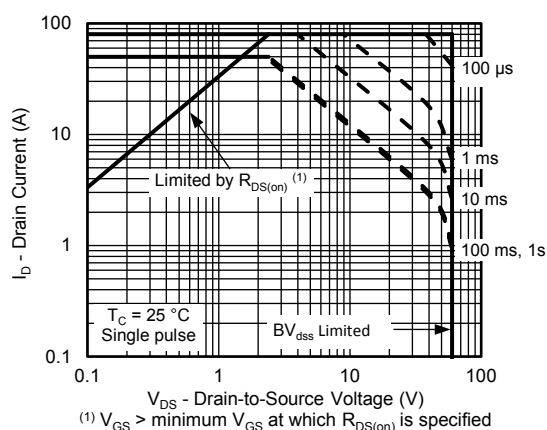


Source-Drain Diode Forward Voltage

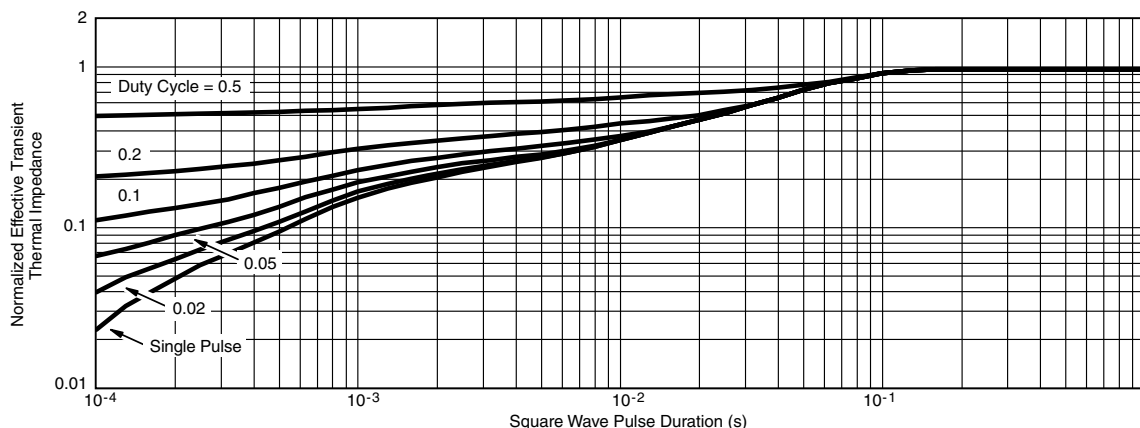
THERMAL RATINGS (25 $^{\circ}\text{C}$, unless otherwise noted)



Drain Current vs. Case Temperature



Safe Operating Area

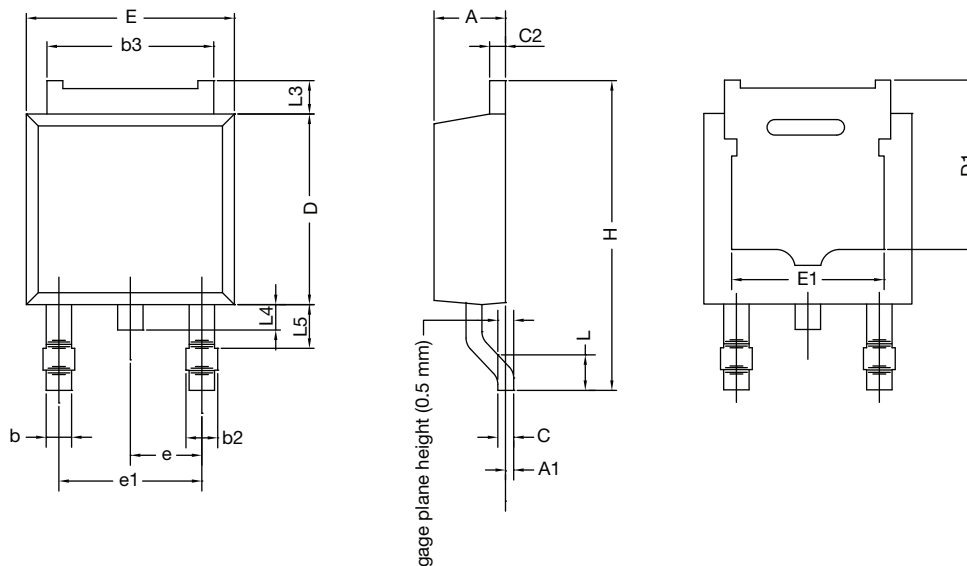


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68940.

TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



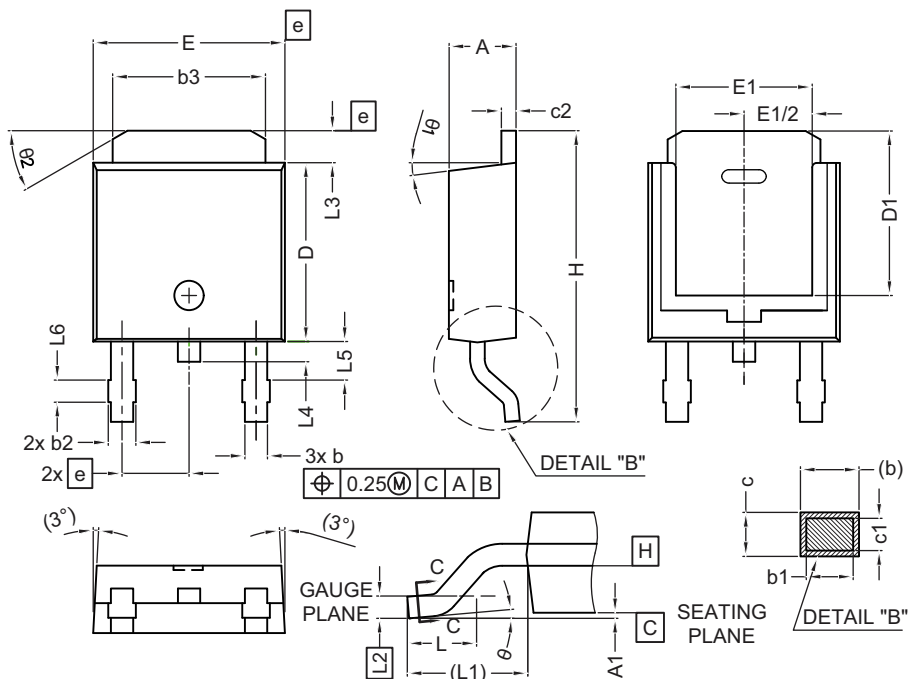
MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

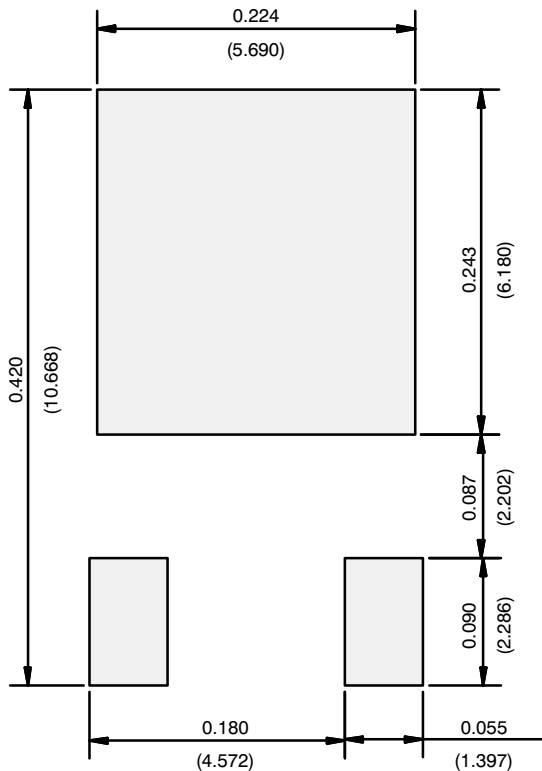
DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ_1	0°	15°
θ_2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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