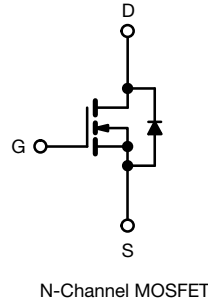
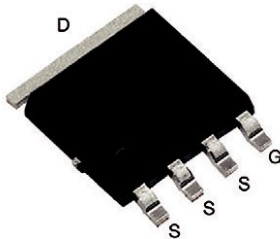


E Series Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	650
$R_{DS(on)}$ typ. at 25 °C (Ω)	$V_{GS} = 10\text{ V}$ 0.45
Q_g max. (nC)	44
Q_{gs} (nC)	5
Q_{gd} (nC)	10
Configuration	Single

PowerPAK® SO-8L Single



FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Switch mode power supplies (SMPS)
- Flyback converter
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Consumer
 - Wall adaptors


ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SiHJ8N60E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150\text{ °C}$)	V_{GS} at 10 V	$T_C = 25\text{ °C}$	8
		$T_C = 100\text{ °C}$	5
Pulsed Drain Current ^a	I_{DM}	18	A
Linear Derating Factor		0.71	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	88	mJ
Maximum Power Dissipation	P_D	89	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	$T_J = 125\text{ °C}$	70
Reverse Diode dV/dt ^d		17	V/ns

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.5\text{ A}$
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ °C}$

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1	1.4	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.71	-	V/ $^\circ\text{C}$	
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA	
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA	
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	10		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$	-	0.45	0.52	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 4\text{ A}$	-	2.4	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	754	-	pF	
Output Capacitance	C_{oss}		-	46	-		
Reverse Transfer Capacitance	C_{rss}		-	5	-		
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$		$V_{DS} = 0\text{ V to } 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	40		-
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	130		-
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$, $V_{DS} = 480\text{ V}$	-	22	44	nC	
Gate-Source Charge	Q_{gs}		-	5	-		
Gate-Drain Charge	Q_{gd}		-	10	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	14	28	ns	
Rise Time	t_r		-	15	30		
Turn-Off Delay Time	$t_{d(off)}$		-	29	58		
Fall Time	t_f		-	14	28		
Gate Input Resistance	R_g		$f = 1\text{ MHz}$	0.5	0.93		2
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8	A	
Pulsed Diode Forward Current	I_{SM}		-	-	18		
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 4\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.85	1.2	V	
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = I_S = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	-	258	516	ns	
Reverse Recovery Charge	Q_{rr}		-	2.4	4.8	μC	
Reverse Recovery Current	I_{RRM}		-	16	-	A	

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

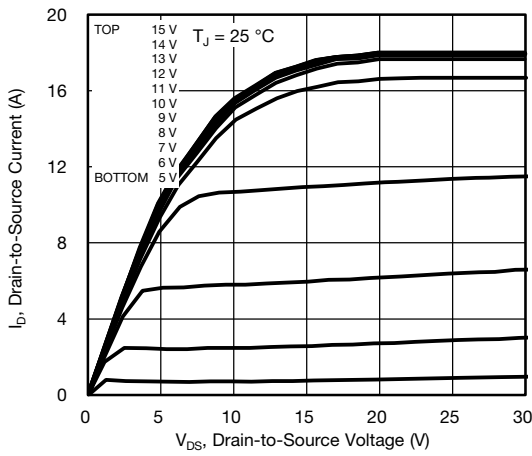


Fig. 1 - Typical Output Characteristics

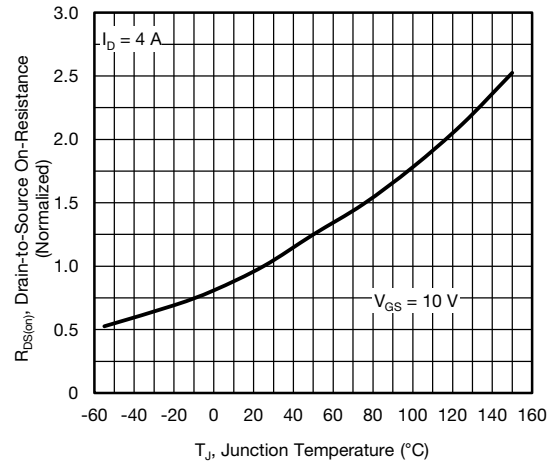


Fig. 4 - Normalized On-Resistance vs. Temperature

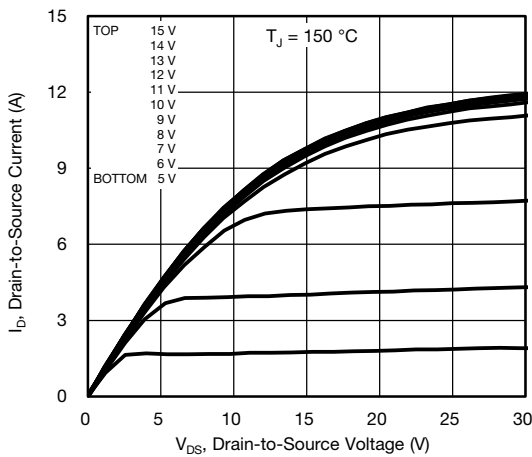


Fig. 2 - Typical Output Characteristics

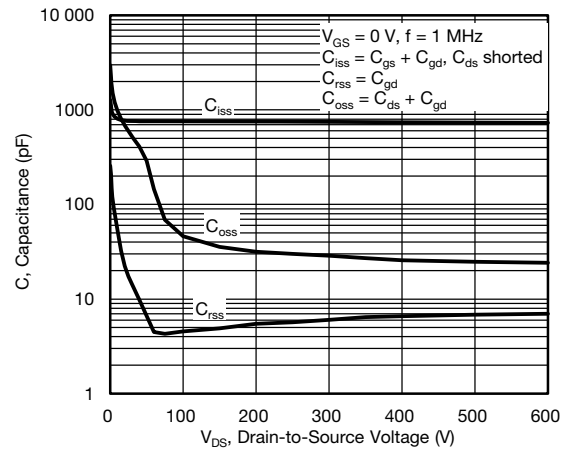


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

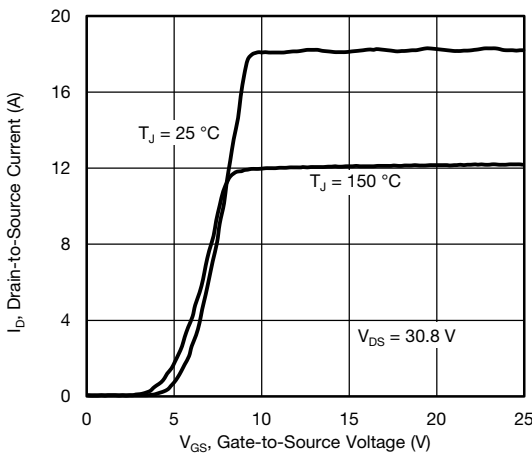


Fig. 3 - Typical Transfer Characteristics

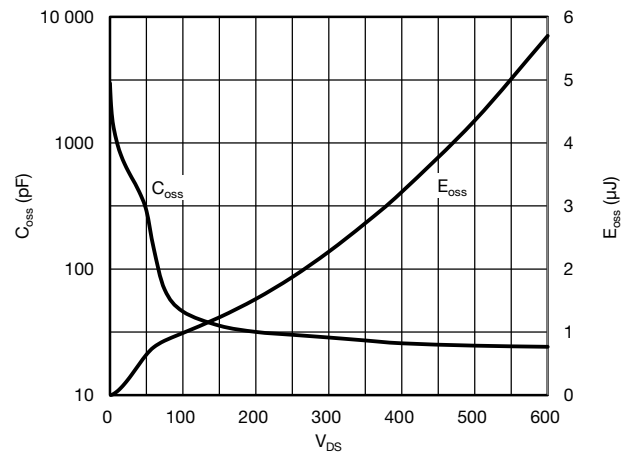


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

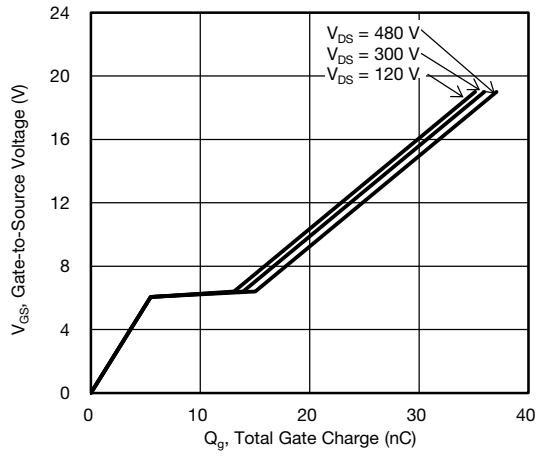


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

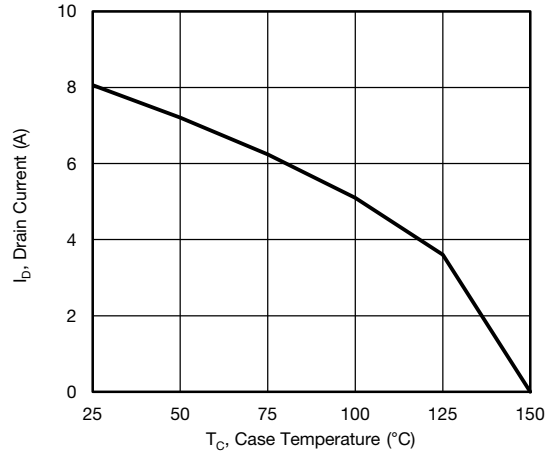


Fig. 10 - Maximum Drain Current vs. Case Temperature

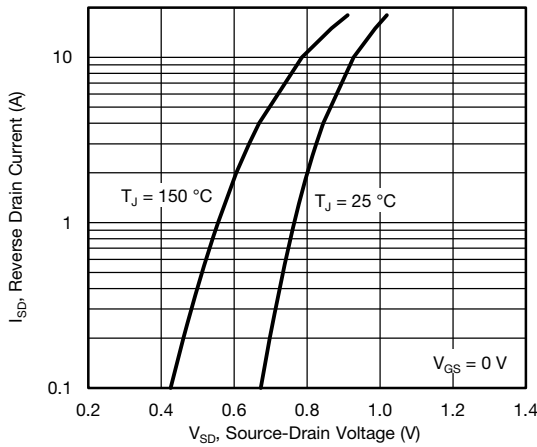


Fig. 8 - Typical Source-Drain Diode Forward Voltage

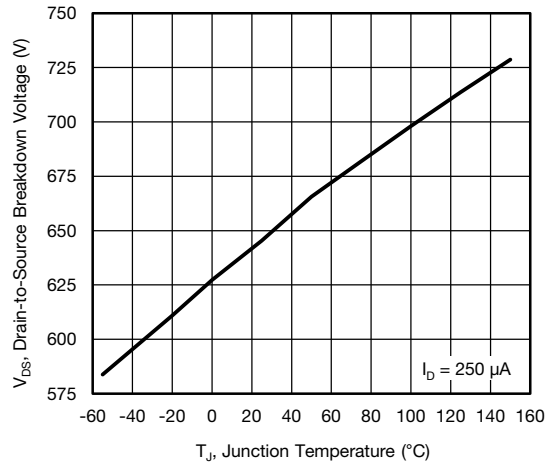


Fig. 11 - Temperature vs. Drain-to-Source Voltage

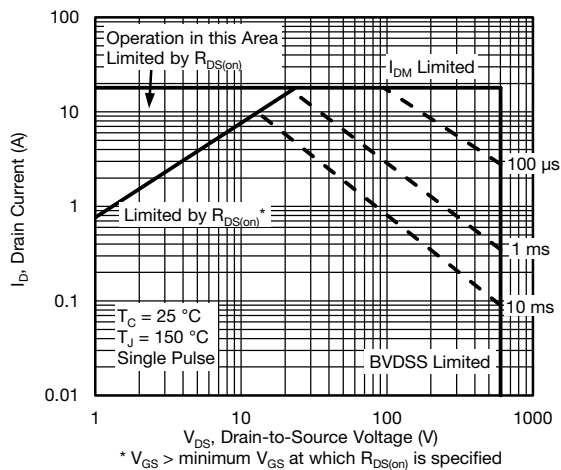


Fig. 9 - Maximum Safe Operating Area

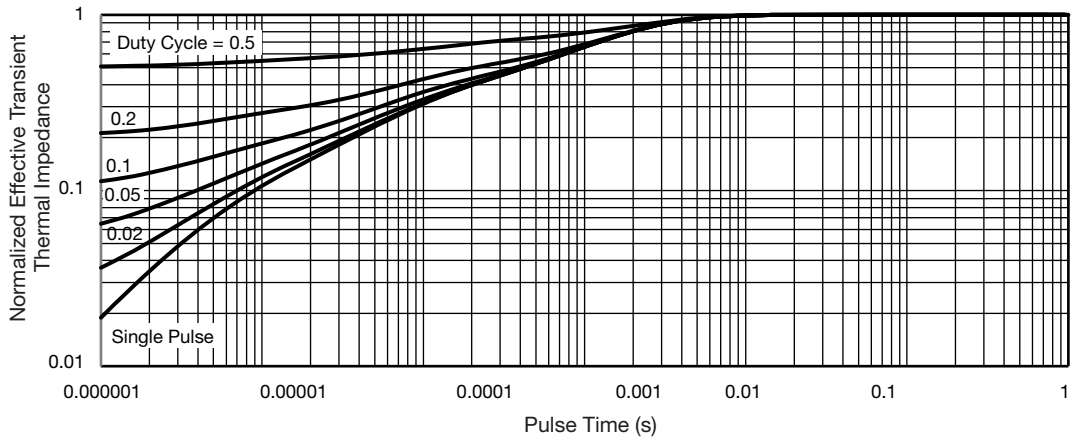


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

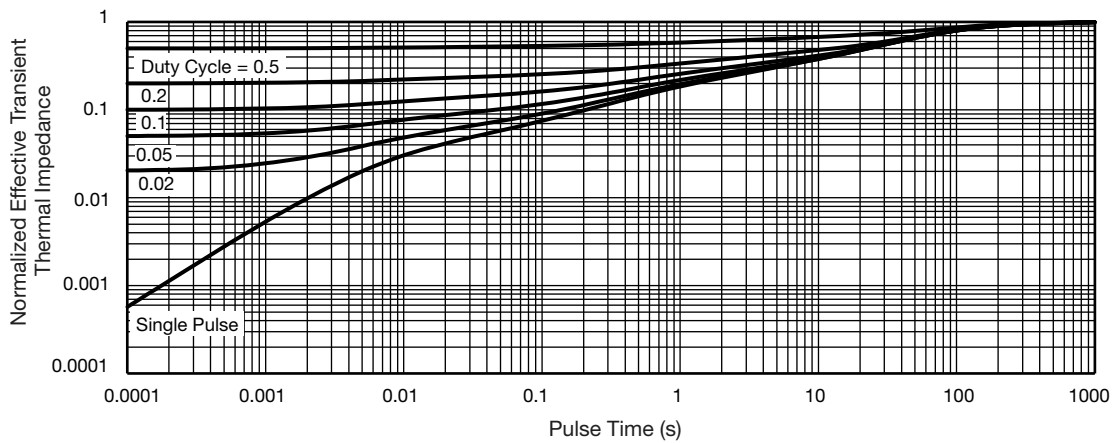


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

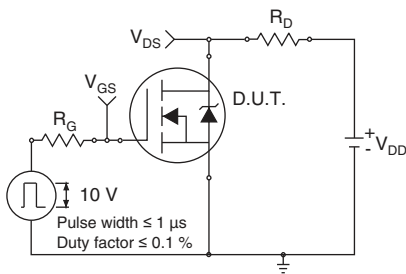


Fig. 14 - Switching Time Test Circuit

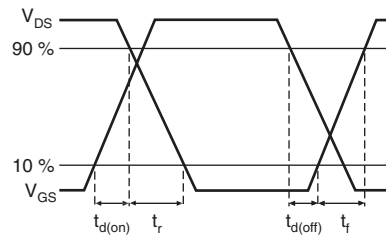


Fig. 15 - Switching Time Waveforms

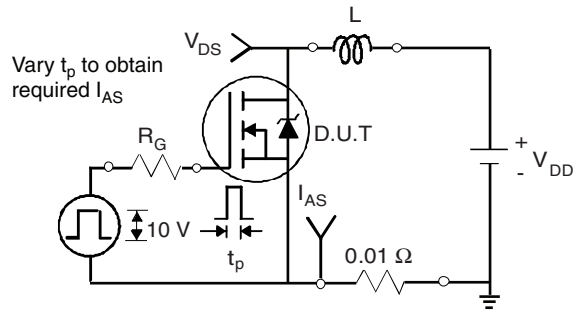


Fig. 16 - Unclamped Inductive Test Circuit

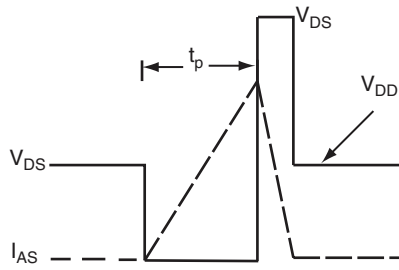


Fig. 17 - Unclamped Inductive Waveforms

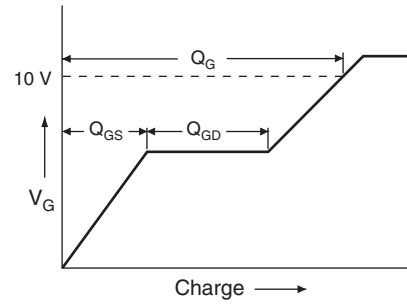


Fig. 18 - Basic Gate Charge Waveform

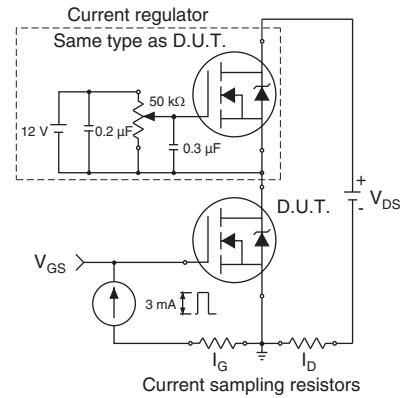
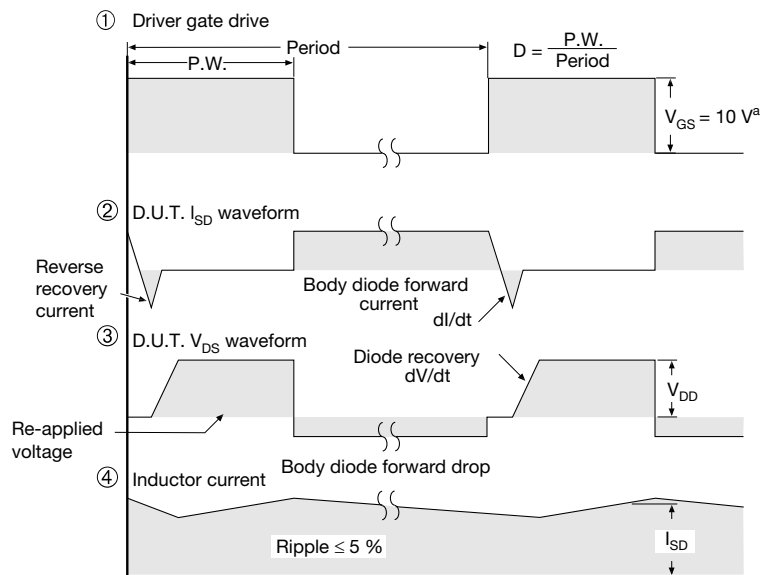
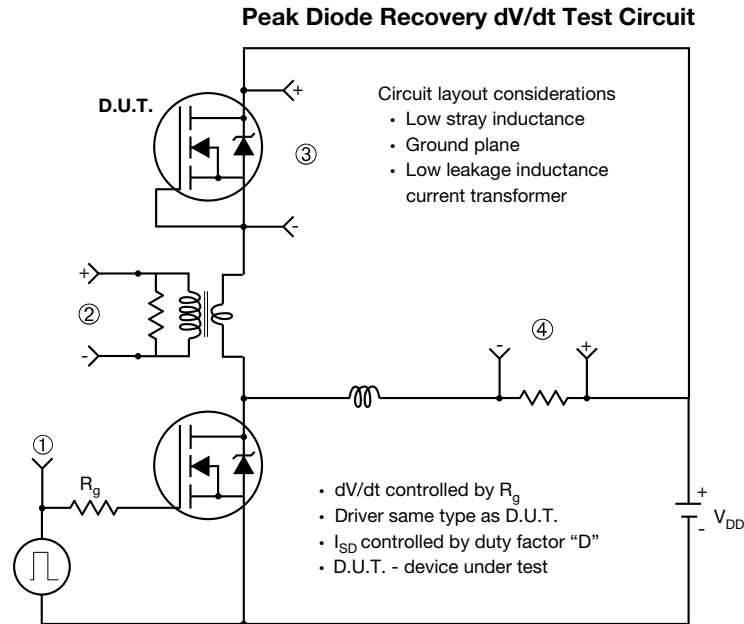


Fig. 19 - Gate Charge Test Circuit



Note

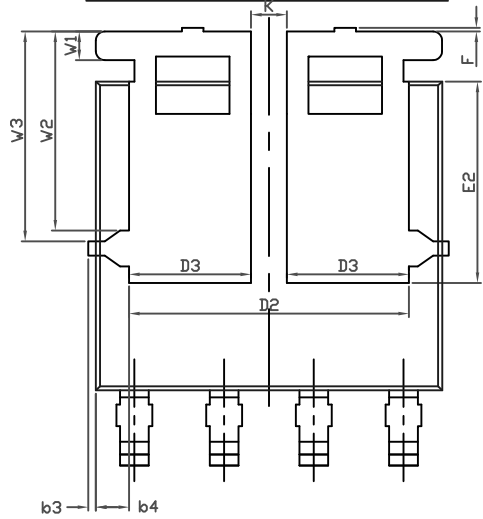
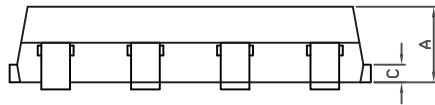
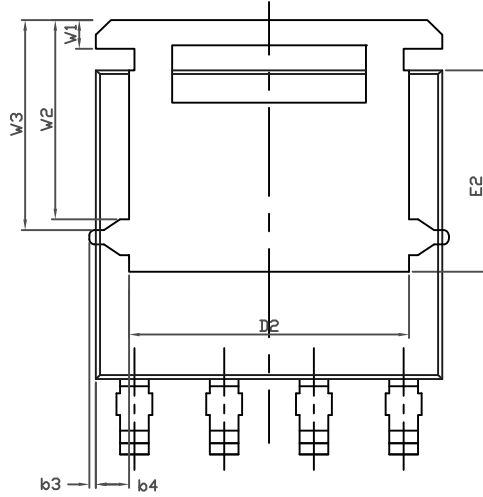
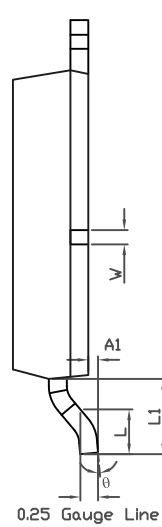
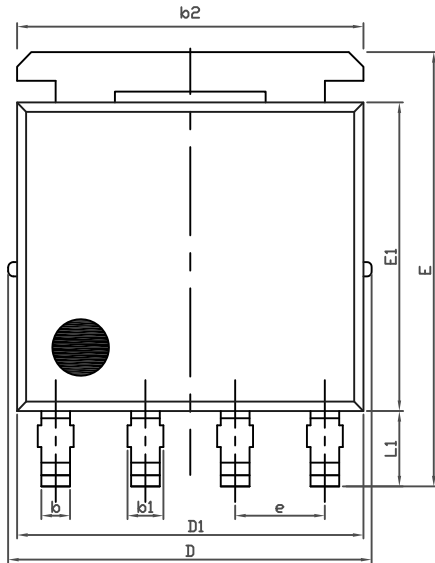
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 20 - For N-Channel

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PowerPAK[®] SO-8L Case Outline 2





DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
q	0°	-	10°	0°	-	10°
ECN: S19-0643-Rev. B, 05-Aug-2019 DWG: 6044						

Note

- Millimeters will govern



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