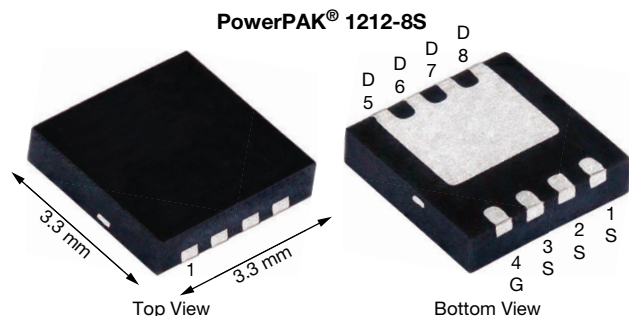


N-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0045
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0054
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 6$ V	0.0078
Q_g typ. (nC)	15.5
I_D (A)	60 ^{a, g}
Configuration	Single

FEATURES

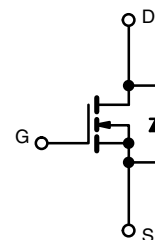
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS} - Q_g$ figure-of-merit (FOM)
- Tuned for the lowest $R_{DS} - Q_{oss}$ FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Solar micro inverter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS26DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	60 ^a	A
	$T_C = 70$ °C	60 ^a	
	$T_A = 25$ °C	23.3 ^{b, c}	
	$T_A = 70$ °C	18.4 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	150	
Continuous source-drain diode current	$T_C = 25$ °C	51.8	
	$T_A = 25$ °C	4.3 ^{b, c}	
Single pulse avalanche current	I_{AS}	25	
Single pulse avalanche energy	E_{AS}	31.2	mJ
Maximum power dissipation	$T_C = 25$ °C	57	W
	$T_C = 70$ °C	36	
	$T_A = 25$ °C	4.8 ^{b, c}	
	$T_A = 70$ °C	3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	21	26	°C/W
Maximum junction-to-case (drain)	R_{thJC}	1.7	2.2	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- $T_C = 25$ °C



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	32	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-6.7	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	3.6	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	40	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.0037	0.0045	Ω
		V _{GS} = 7.5 V, I _D = 10 A	-	0.0043	0.0054	
		V _{GS} = 6 V, I _D = 10 A	-	0.0060	0.0078	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	-	54	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	-	1710	-	pF
Output capacitance	C _{oss}		-	445	-	
Reverse transfer capacitance	C _{rss}		-	29	-	
Total gate charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 10 A	-	24.5	37	nC
Gate-source charge	Q _{gs}	V _{DS} = 30 V, V _{GS} = 6 V, I _D =10 A	-	15.5	24	
Gate-drain charge	Q _{gd}		-	6.5	-	
Output charge	Q _{oss}		-	4.5	-	
Gate resistance	R _g	V _{DS} = 30 V, V _{GS} = 0 V	-	27.5	-	Ω
Turn-on delay time	t _{d(on)}	f = 1 MHz	0.3	0.85	1.5	
Rise time	t _r	V _{DD} = 30 V, R _L = 3 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	20	ns
Turn-off delay time	t _{d(off)}		-	22	44	
Fall time	t _f		-	14	28	
Turn-on delay time	t _{d(on)}		-	9	18	
Rise time	t _r	V _{DD} = 30 V, R _L = 3 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	11	22	
Turn-off delay time	t _{d(off)}		-	23	46	
Fall time	t _f		-	13	26	
Fall time	t _f		-	9	18	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	25.1	A
Pulse diode forward current	I _{SM}		-	-	150	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.77	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	44	88	ns
Body diode reverse recovery charge	Q _{rr}		-	42	84	nC
Reverse recovery fall time	t _a		-	20	-	ns
Reverse recovery rise time	t _b		-	24	-	

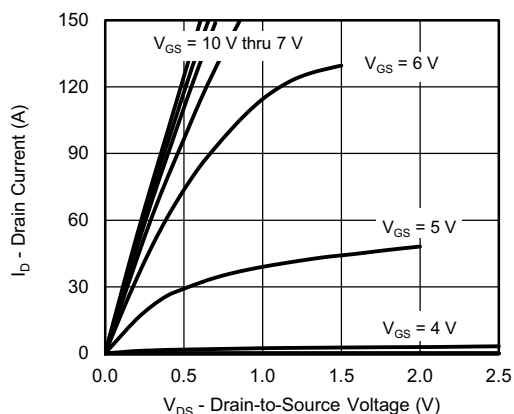
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

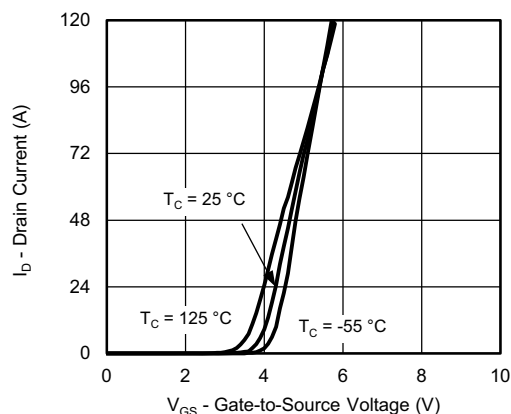
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



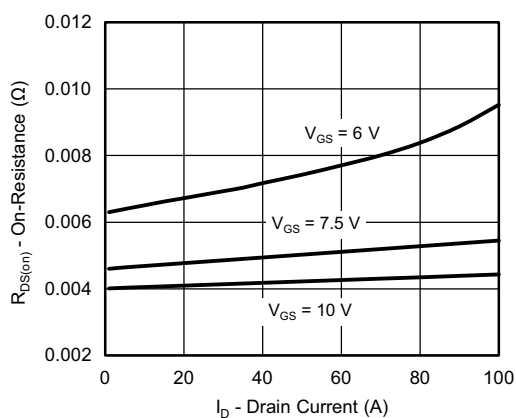
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



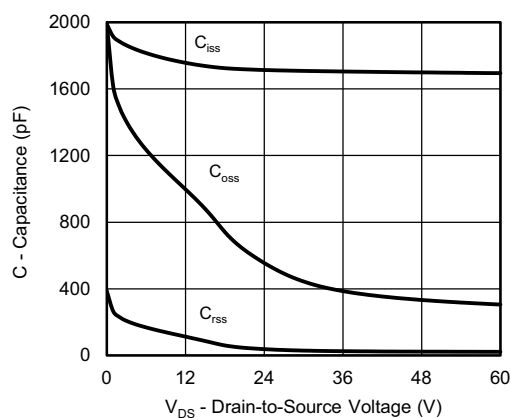
Output Characteristics



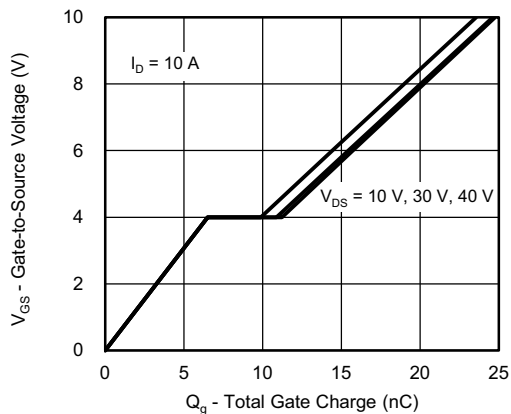
Transfer Characteristics



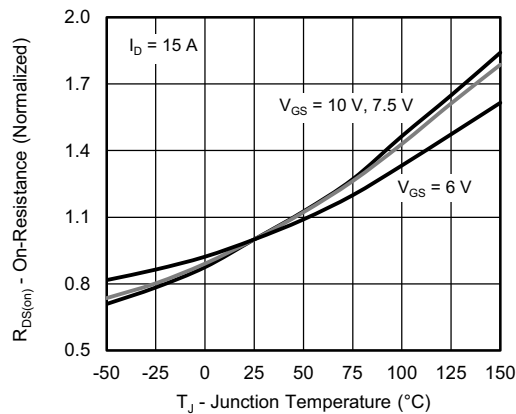
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



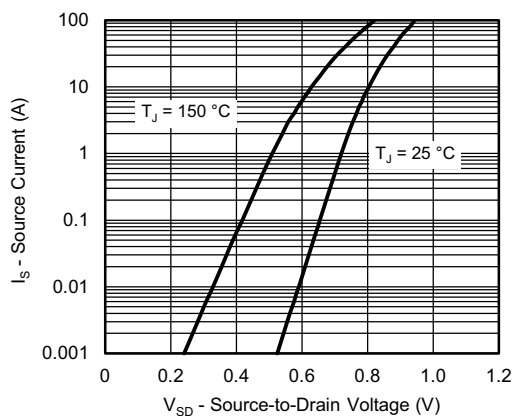
Gate Charge



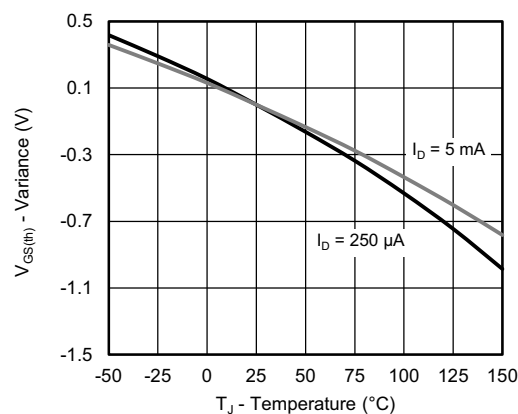
On-Resistance vs. Junction Temperature



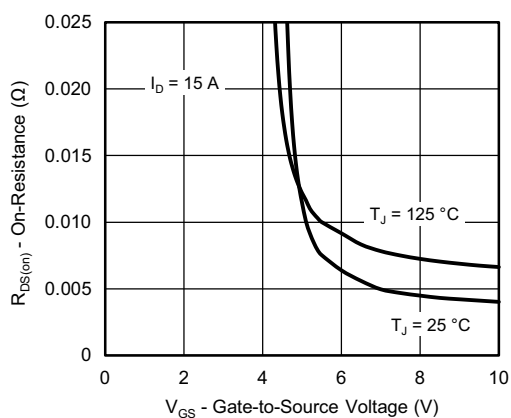
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



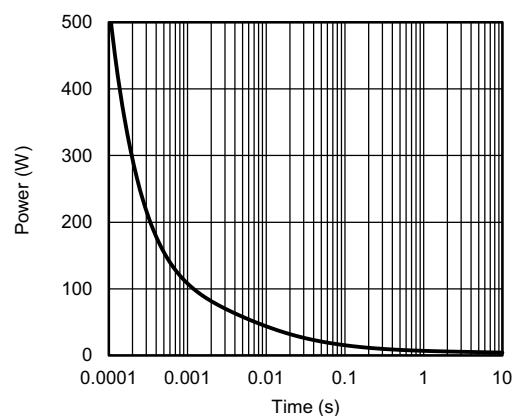
Source-Drain Diode Forward Voltage



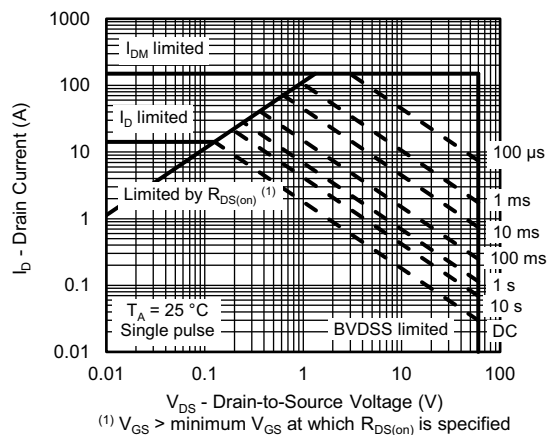
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



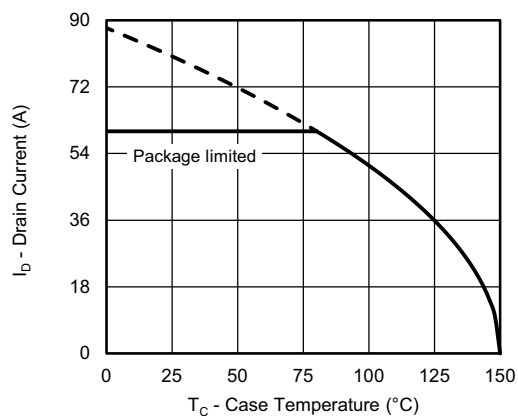
Single Pulse Power, Junction-to-Ambient



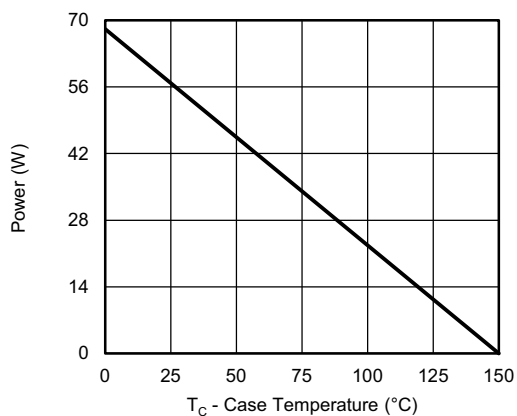
Safe Operating Area, Junction-to-Ambient



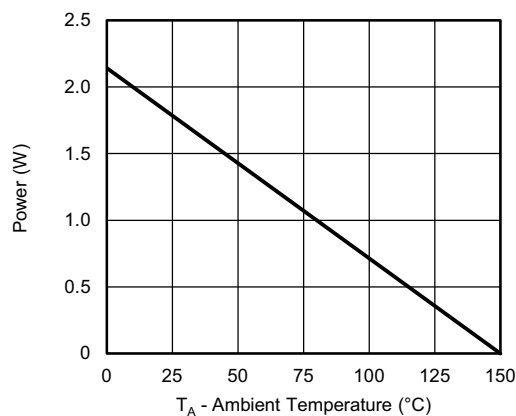
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



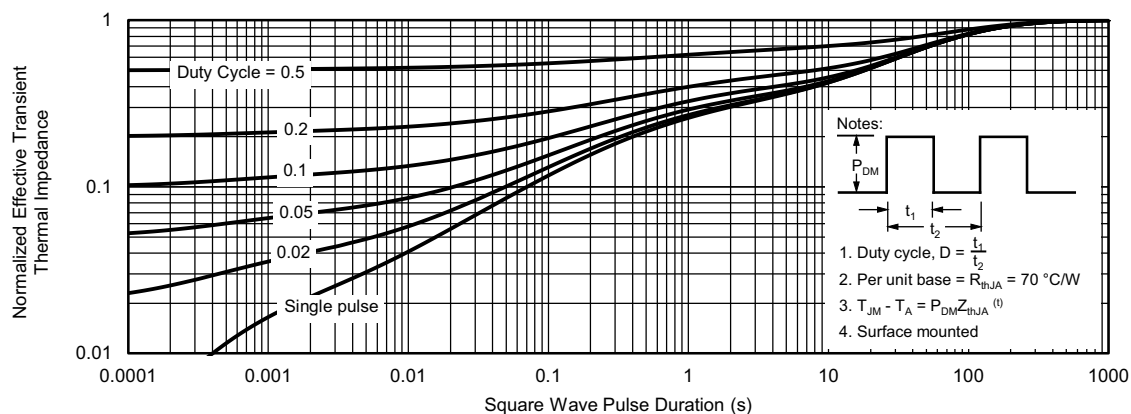
Power, Junction-to-Ambient

Note

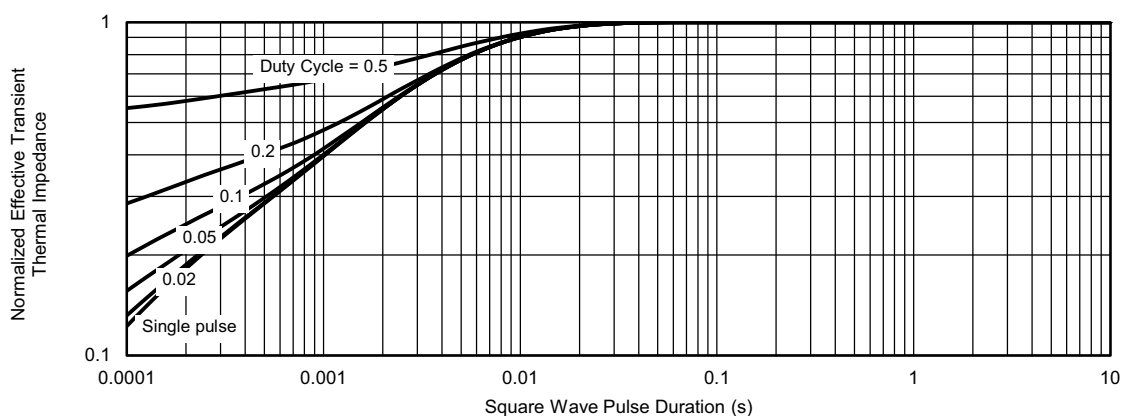
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75501.

Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.027	0.030	0.033
A1	0	-	0.05	0	-	0.002
A3	0.20 REF			0.008 REF		
b	0.30 BSC			0.012 BSC		
D	3.30 BSC			0.130 BSC		
D1	2.15	2.25	2.35	0.084	0.088	0.092
E	3.30 BSC			0.130 BSC		
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 BSC			0.026 BSC		
K	0.76 TYP			0.030 TYP		
K1	0.41 TYP			0.016 TYP		
L	0.43 BSC			0.017 BSC		
z	0.525 TYP			0.021 TYP		
ECN: C12-0200-Rev. A, 12-Mar-12 DWG: 6008						

Note

- Millimeters will govern.

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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