



Vishay Siliconix

N-Channel 150 V (D-S) MOSFET

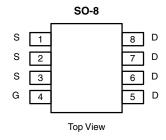
PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
150	0.050 at $V_{GS} = 10 \text{ V}$	5		

FEATURES

- TrenchFET® Power MOSFETs
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

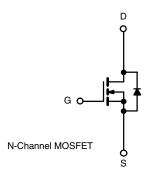


HALOGEN FREE



Ordering Information: Si4488DY-T1-E3 (Lead (Pb)-free)

Si4488DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	150		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Proin Current /T 150 °C\a	T _A = 25 °C	I_	5	3.5	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	- I _D	4	2.8	
Pulsed Drain Current	I _{DM}	50		Α	
Avalanche Current	L = 0.1 mH	I _{AS}	25		
Continuous Source Current (Diode Conduction) ^a	I _S	2.8	1.4		
Marian ma Damar Dissination	T _A = 25 °C	P _D	3.1	1.56	W
Maximum Power Dissipation ^a	T _A = 70 °C	' D	2	1	, vv
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Manifestor Londing to Applicate	t ≤ 10 s	R _{thJA}	33	40	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	65	80	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

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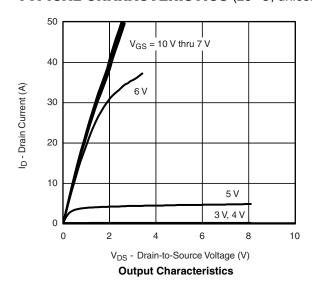
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	mbol Test Conditions		Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtana Busin Comment	_	V _{DS} = 120 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 120 V, V _{GS} = 0 V, T _J = 55 °C			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	50			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		0.041	0.050	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 5 A		18		S	
Diode Forward Voltage ^a	V _{SD}	I _S = 2.8 A, V _{GS} = 0 V		0.75	1.1	V	
Dynamic ^b							
Total Gate Charge	Q_g			30	45		
Gate-Source Charge	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		8.5		nC	
Gate-Drain Charge	Q_{gd}			8.5			
Gate Resistance	R _g		0.2	0.85	1.2	Ω	
Turn-On Delay Time	t _{d(on)}			12	18		
Rise Time	t _r	V_{DD} = 75 V, R_L = 15 Ω		7	11		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 5$ A, V_{GEN} = 10 V, R_g = 6 Ω		22	33	ns	
Fall Time	t _f			10	15		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.8 A, dl/dt = 100 A/μs		40	70		

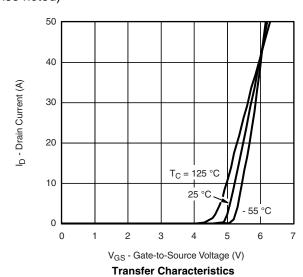
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

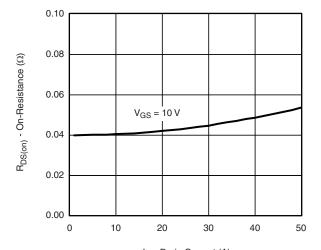






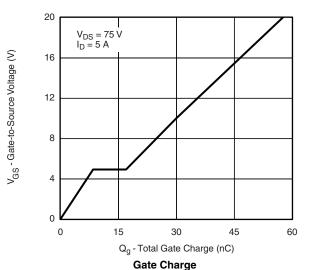


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



I_D - Drain Current (A)

On-Resistance vs. Drain Current



T_J = 150 °C

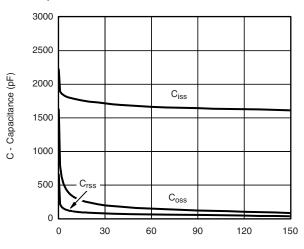
T_J = 150 °C

T_J = 25 °C

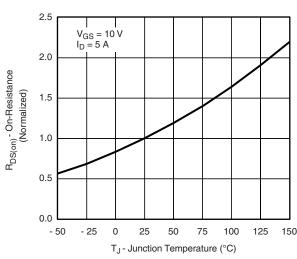
T_J = 25 °C

V_{SD} - Source-to-Drain Voltage (V)

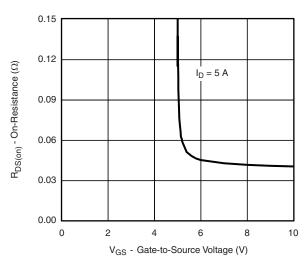
Source-Drain Diode Forward Voltage



V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



On-Resistance vs. Junction Temperature



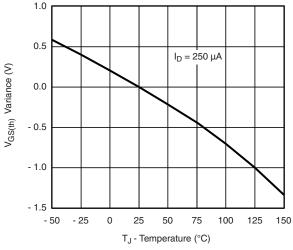
On-Resistance vs. Gate-to-Source Voltage

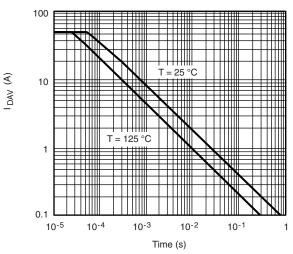
I_S - Source Current (A)

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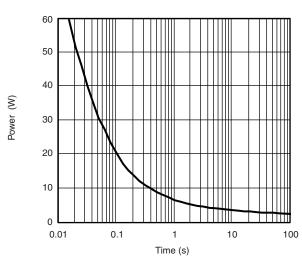
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



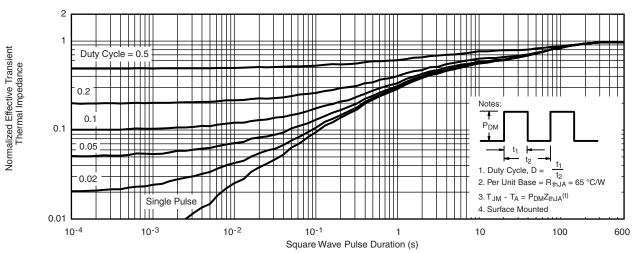


Threshold Voltage

Avalanche Current vs. Time



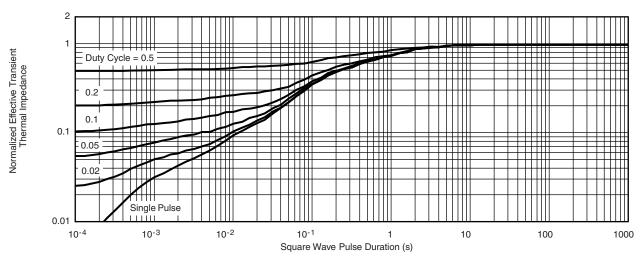
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71240.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Bey 11-Sen-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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