Dual N-Channel 80-V (D-S) MOSFET

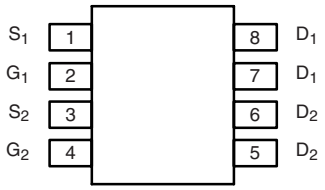
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
80	0.075 at V_{GS} = 10 V	3.7
	0.095 at V_{GS} = 6.0 V	3.2

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC

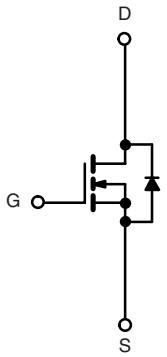
Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

SO-8



Top View

Ordering Information: Si4980DY-T1-E3 (Lead (Pb)-free)
Si4980DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	3.7	A
	T_A = 70 °C		2.9	
Pulsed Drain Current		I_{DM}	30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.0	W
	T_A = 70 °C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

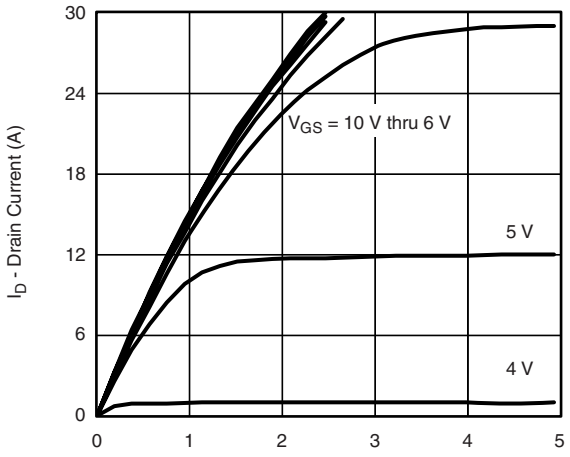
Notes:
a. Surface Mounted on FR4 board, t ≤ 10 s.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 80$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			20	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = 5$ V, $V_{GS} = 10$ V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.7$ A		0.062	0.075	Ω
		$V_{GS} = 6.0$ V, $I_D = 3.2$ A		0.071	0.095	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15$ V, $I_D = 3.7$ A		12		S
Diode Forward Voltage[a]	V_{SD}	$I_S = 1.7$ A, $V_{GS} = 0$ V			1.2	V
Dynamic[b]						
Gate Charge	Q_g	$V_{DS} = 40$ V, $V_{GS} = 10$ V, $I_D = 3.7$ A		15	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3.2		
Gate Resistance	R_g		1		5.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40$ V, $R_L = 40\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_g = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7$ A, dI/dt = 100 A/µs		75	110	

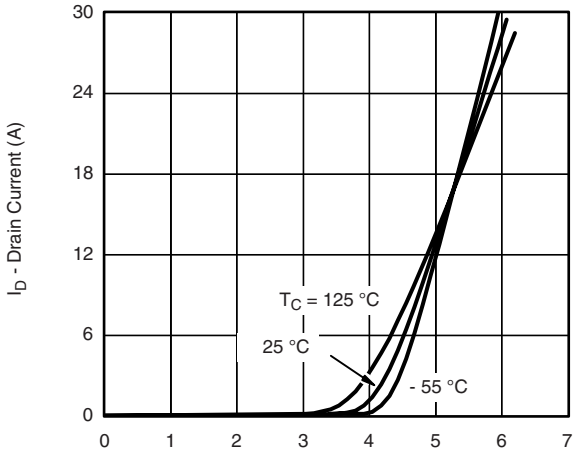
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. For design aid only; not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

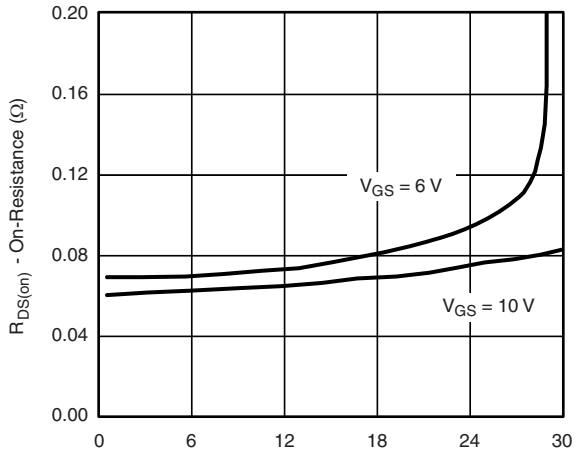
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



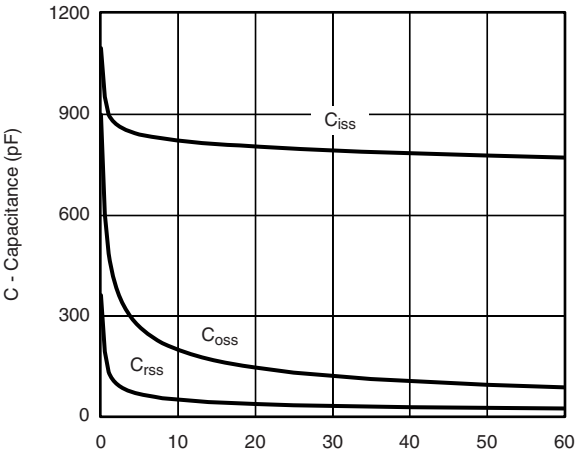
Output Characteristics



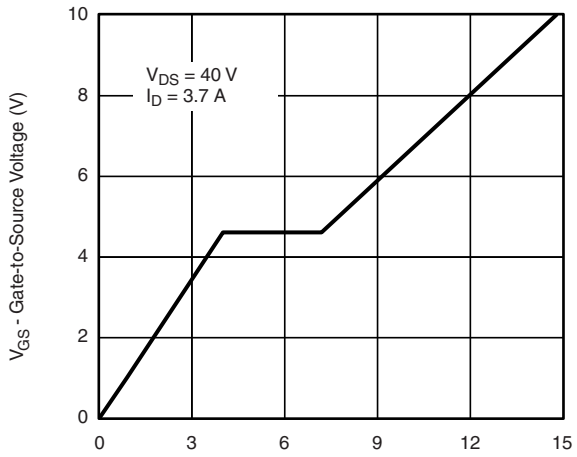
Transfer Characteristics



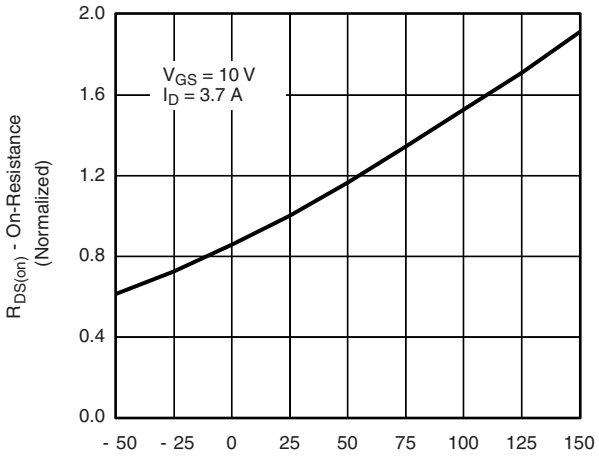
On-Resistance vs. Drain Current



Capacitance

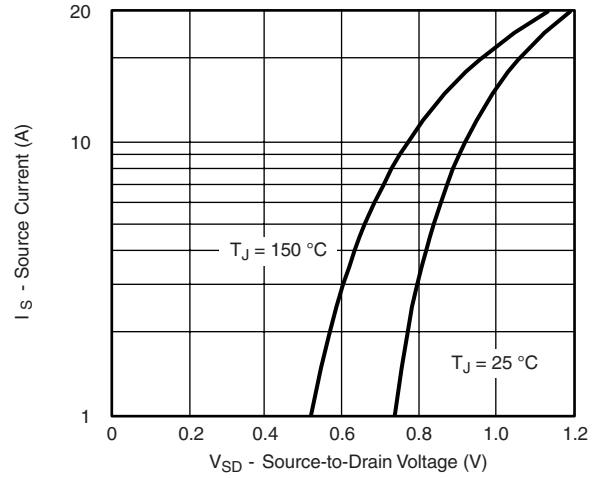


Gate Charge

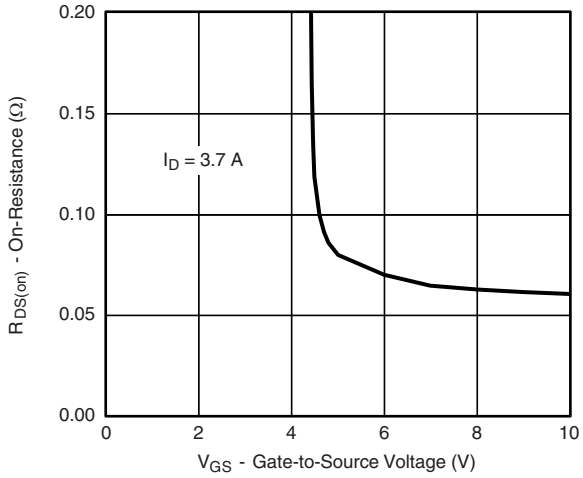


On-Resistance vs. Junction Temperature

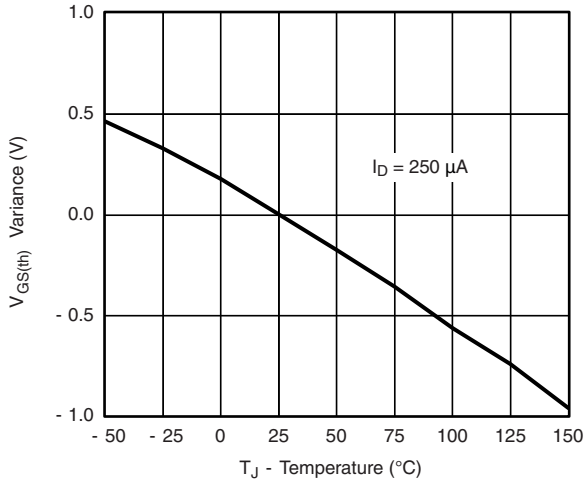
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



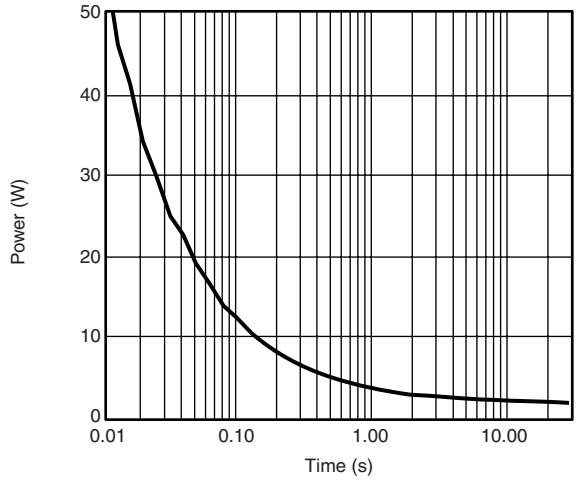
Source-Drain Diode Forward Voltage



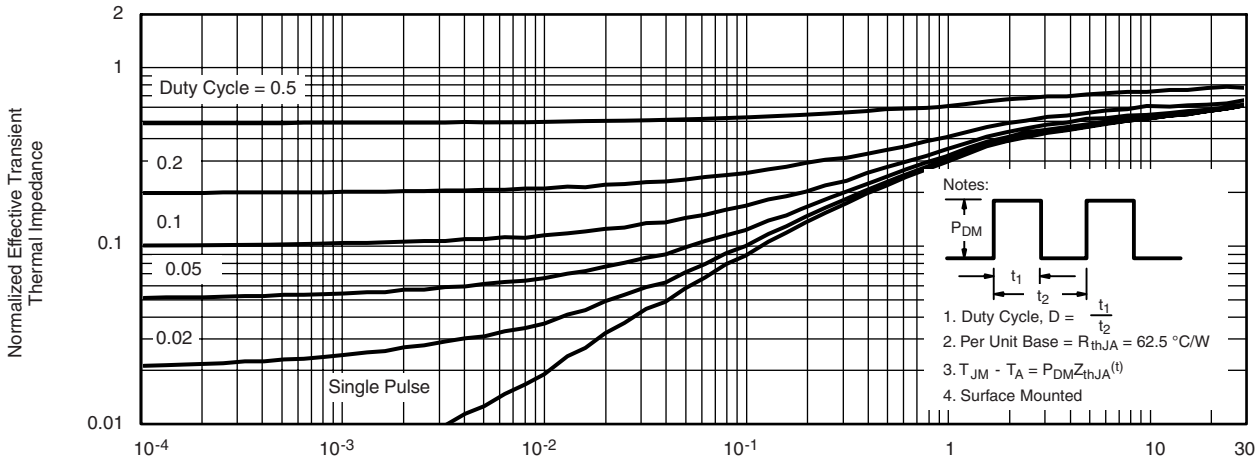
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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