



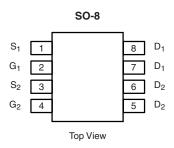
Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)	
100	0.150 at V _{GS} = 10 V	2.6	
	0.180 at V _{GS} = 6 V	2.4	

FEATURES

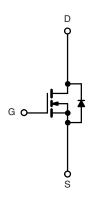
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC





Ordering Information: Si4982DY-T1-E3 (Lead (Pb)-free)

Si4982DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	ss otherwise no	ted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	100	
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	1	2.6	
	T _A = 70 °C	I _D	2.1	
Pulsed Drain Current		I _{DM}	20	A
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	
	T _A = 25 °C	D	2.0	10/
Maximum Power Dissipation ^a	T _A = 70 °C	P _D	1.3	W
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W	

Notes:

a. Surface Mounted on FR4 board, $t \le 10 \text{ s.}$

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2			V		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ		
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			20			
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	15			Α		
Drain-Source On-State Resistance ^b	В	$V_{GS} = 10 \text{ V}, I_D = 2.6 \text{ A}$		0.130	0.150			
	R _{DS(on)}	$V_{GS} = 6 \text{ V}, I_D = 2.4 \text{ A}$		0.140	0.180	Ω		
Forward Transconductance ^b	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 2.6 \text{ A}$		11		S		
Diode Forward Voltage ^b	V_{SD}	I _S = 1.7 A, V _{GS} = 0 V			1.2	V		
Dynamic ^a								
Gate Charge	Qg			15	30			
Gate-Source Charge	Q_{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.6 \text{ A}$		2.7		nC		
Gate-Drain Charge	Q_{gd}			4.0				
Gate Resistance	R_g		1		4.4	Ω		
Turn-On Delay Time	t _{d(on)}			10	20			
Rise Time	t _r	V_{DD} = 50 V, R_L = 50 Ω		10	20			
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 6 \Omega$		30	60	ns		
Fall Time	t _f			10	20			
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, dI/dt = 100 A/μs		60	90			

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

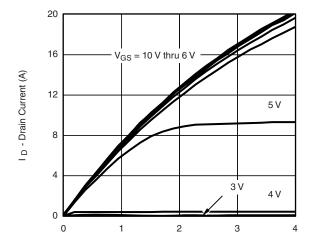
a. For design aid only; not subject to production testing.

b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

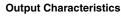


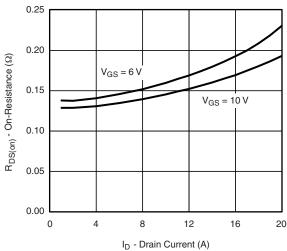


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

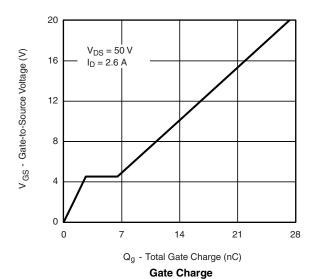


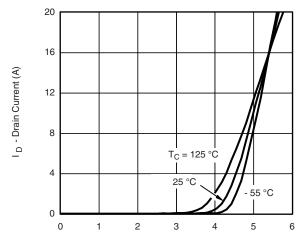
 V_{DS} - Drain-to-Source Voltage (V)





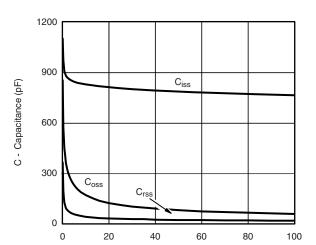
On-Resistance vs. Drain Current





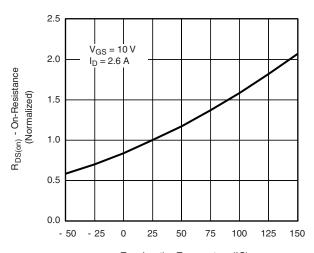
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



V_{DS} - Drain-to-Source Voltage





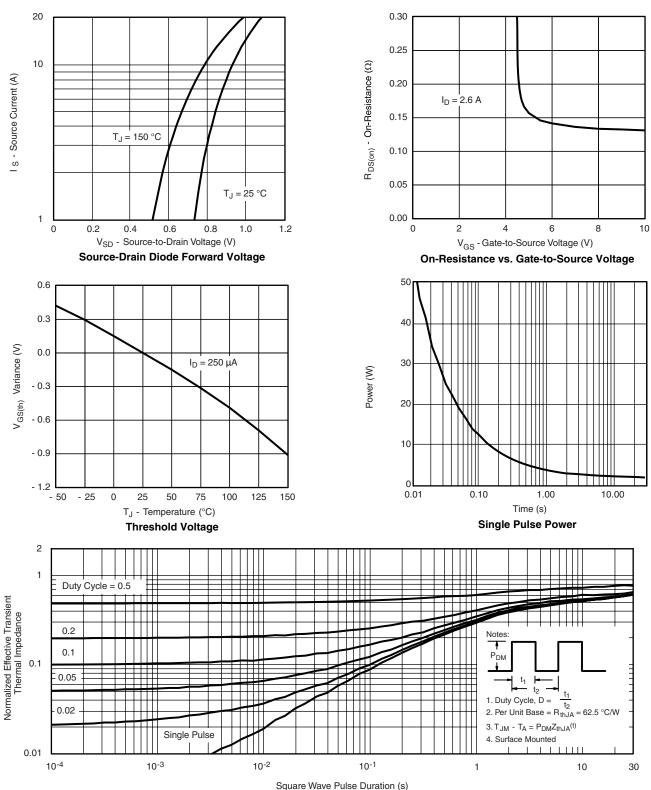
T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg270748.



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