

# Automotive Dual N-Channel 100 V (D-S) 175 °C MOSFET

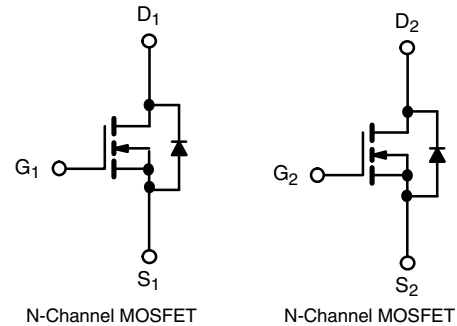
 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

**FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Fully lead (Pb)-free device
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	100
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.0086
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.0114
I <sub>D</sub> (A) per leg	70
Configuration	Dual
Package	PowerPAK 8 x 8L



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V <sub>DS</sub>	100	V
Gate-source voltage	V <sub>GS</sub>	± 20	
Continuous drain current	I <sub>D</sub>	T <sub>C</sub> = 25 °C <sup>a</sup>	70
		T <sub>C</sub> = 125 °C	40
Continuous source current (diode conduction) <sup>a</sup>	I <sub>S</sub>	100	A
Pulsed drain current <sup>b</sup>	I <sub>DM</sub>	280	
Single pulse avalanche current	I <sub>AS</sub>	L = 0.1 mH	42
Single pulse avalanche energy			E <sub>AS</sub>
Maximum power dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	187
		T <sub>C</sub> = 125 °C	62
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R <sub>thJA</sub>	85	°C/W
Junction-to-case (drain)	R <sub>thJC</sub>	2	

**Notes**

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



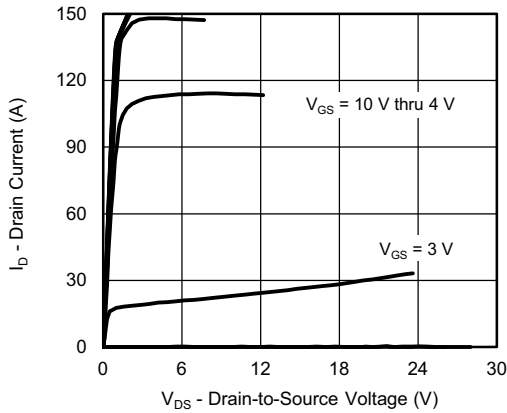
SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.5	2	2.5	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$	-	0.0072	0.0086	$\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 10\text{ A}$	-	0.0095	0.0114	
		$V_{GS} = 10\text{ V}$	$I_D = 5\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0110	
		$V_{GS} = 10\text{ V}$	$I_D = 5\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0187	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		-	52	-	S
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}$	-	2266	2832	$\text{pF}$
Output capacitance	$C_{oss}$			-	799	1000	
Reverse transfer capacitance	$C_{rss}$			-	34	43	
Total gate charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 50\text{ V}, I_D = 10\text{ A}$	-	46	58	$\text{nC}$
Gate-source charge <sup>c</sup>	$Q_{gs}$			-	7	-	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	10	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$		1.1	1.9	3.0	$\Omega$
Turn-on delay time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	11	14	$\text{ns}$
Rise time <sup>c</sup>	$t_r$			-	4	5	
Turn-off delay time <sup>c</sup>	$t_{d(off)}$			-	33	42	
Fall time <sup>c</sup>	$t_f$			-	7	8	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed current <sup>a</sup>	$I_{SM}$			-	-	280	A
Forward voltage	$V_{SD}$	$I_F = 40\text{ A}, V_{GS} = 0$		-	1	1.2	V

**Notes**

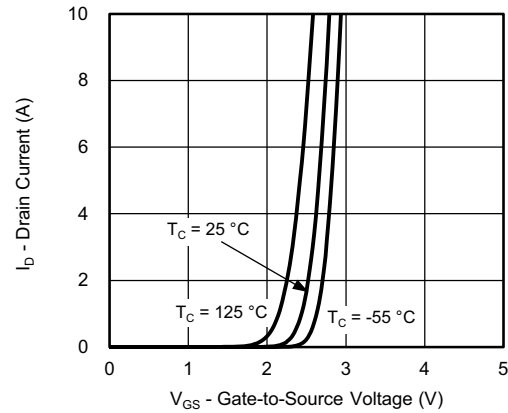
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

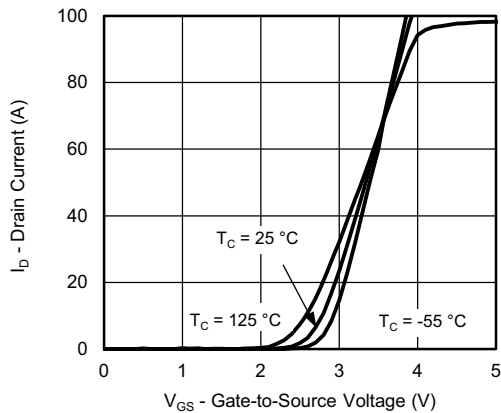
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



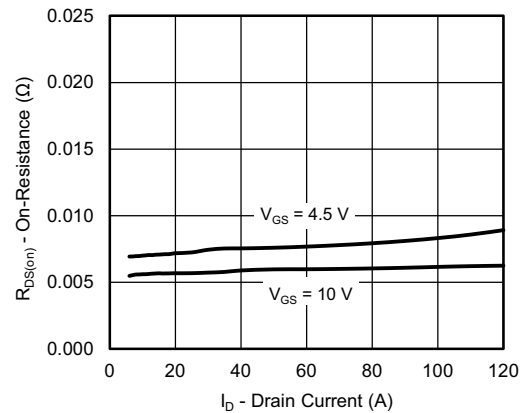
**Output Characteristics**



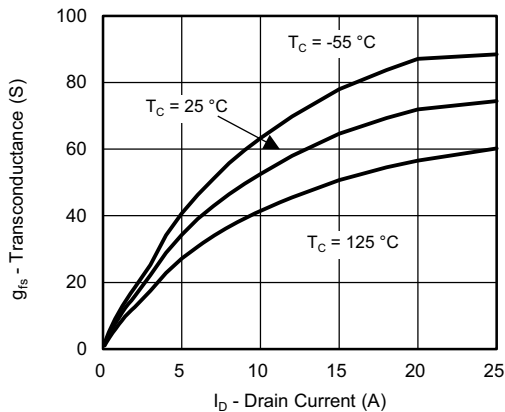
**Transfer Characteristics**



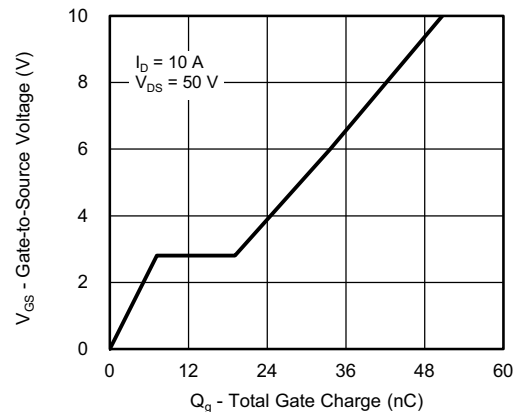
**Transfer Characteristics**



**On-Resistance vs. Drain Current**



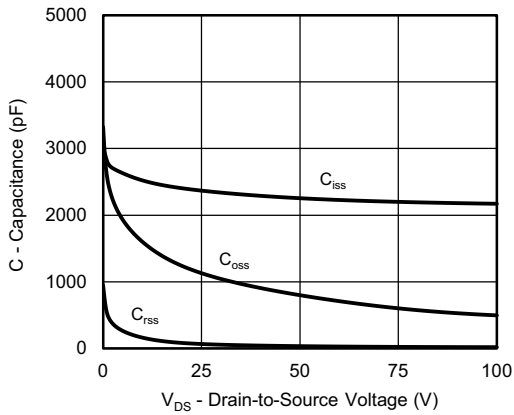
**Transconductance**



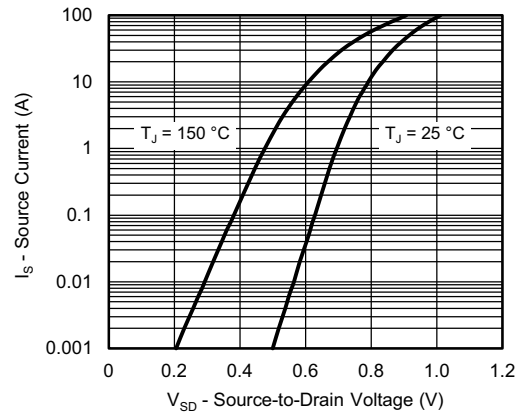
**Capacitance**



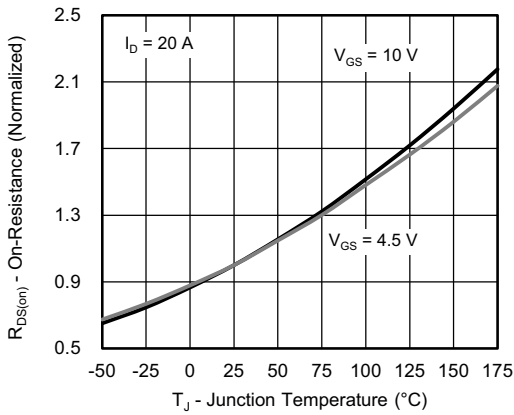
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



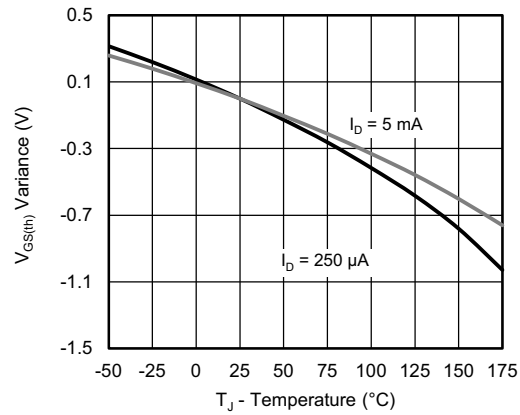
Capacitance



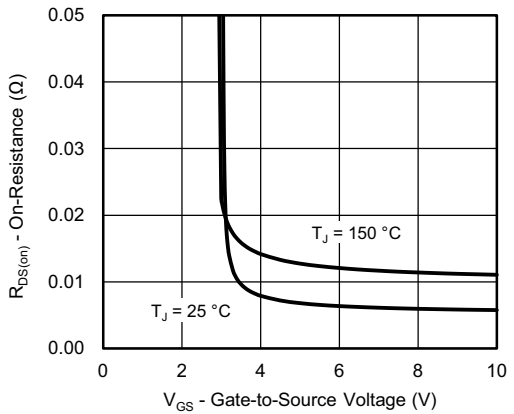
Source Drain Diode Forward Voltage



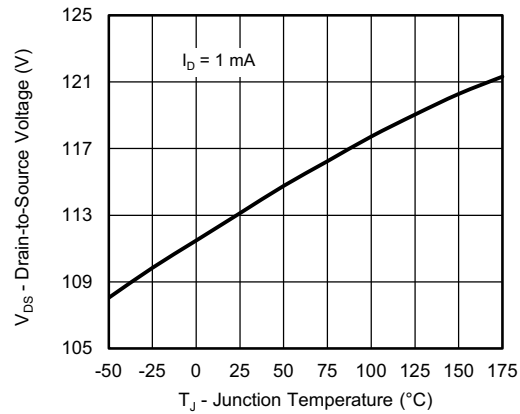
On-Resistance vs. Junction Temperature



Threshold Voltage



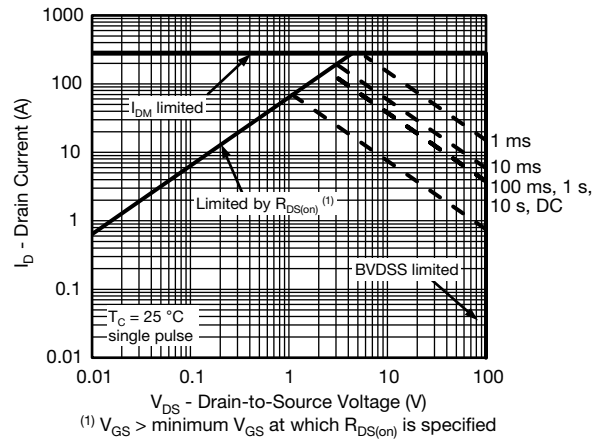
On-Resistance vs. Gate-to-Source Voltage



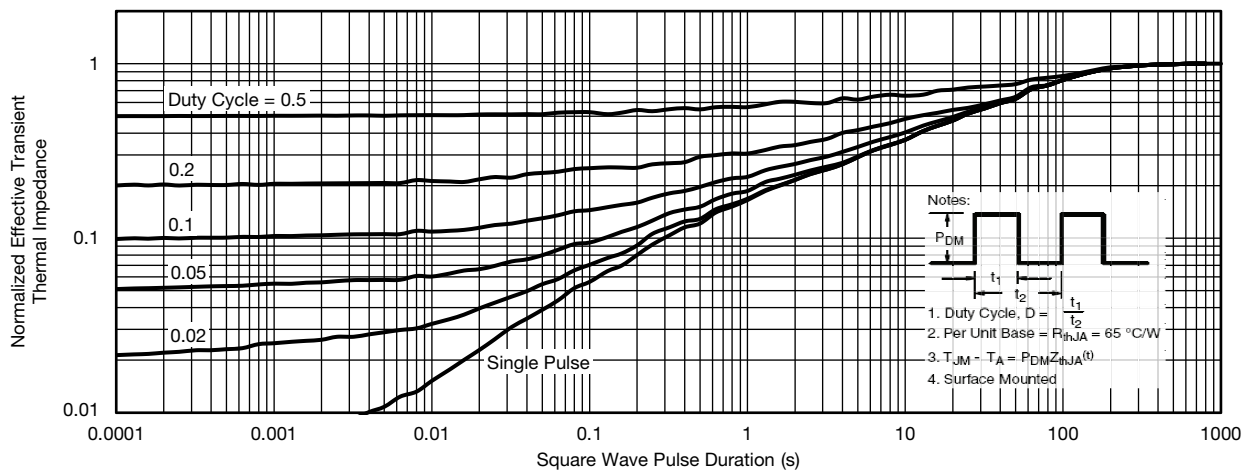
Drain Source Breakdown vs. Junction Temperature



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^\circ\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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