Power Down Fault Protected, 1.8 V to 5.5 V, 2.5 Ω, 4-Channel (4:1) Multiplexer

DESCRIPTION

The DG2034E is a four-channel multiplexer that operates with a single 1.8 V to 5.5 V power supply. It features power down fault protection that prevents excessive current flow when V+ is to ground.

The device's low power dissipation and wide voltage range make it ideal for use in battery powered products. The ultra low capacitance and charge injection of the switch make it an ideal solution for data acquisition and sample and hold applications, where low glitch and fast settling are required. Low switch resistance and fast switching speeds, together with high signal bandwidth, make the DG2034E suitable for video signal switching.

The DG2034E switches one of four inputs to a common output as determined by the 3-bit binary address lines: A0, A1, and EN. Each switch conducts equally well in both directions when on, blocks input voltages up to the supply level when off, and exhibits break before make switching action.

The device's high ESD and latch-up current capability make it more reliable in designs where the part sits close to the interface.

The DG2034E is available in MSOP10 and QFN12 3 mm x 3 mm packages.

FEATURES

- 2.5 Ω switch on-resistance
- 7 pF source-off capacitance
- 27 pF comm-off capacitance
- 33 pF comm-on capacitance
- 13 ns turn-on time
- -2 pC charge injection
- -67 dB off-isolation at 1 MHz
- -71 dB crosstalk at 1 MHz
- 166 MHz bandwidth
- 8 kV ESD / HBM
- 400 mA latch-up current

Pb-free

RoHS COMPLIANT

BENEFITS

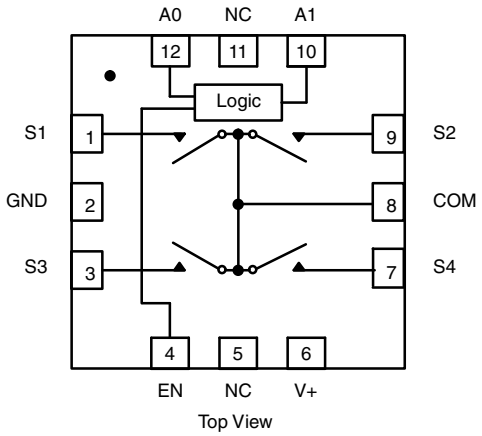
- Power down fault protection
- Low parasitic and charge injection
- Wide operation voltage range
- High ESD tolerance

APPLICATIONS

- Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video switching
- Relay replacements

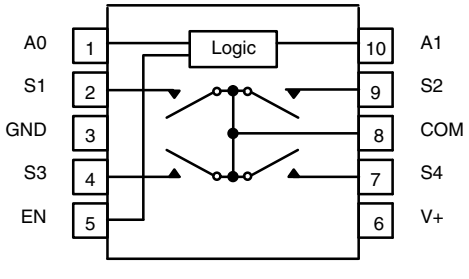
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

12-Pin QFN (3 mm x 3 mm)



Top View

MSOP-10



Top View

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TRUTH TABLE			
A1	A0	EN	ON SWITCH
X	X	0	None
0	0	1	S1
0	1	1	S2
1	0	1	S3
1	1	1	S4

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	MSOP-10	DG2034EDQ-T1-GE3
	12-pin QFN (3 mm x 3 mm)	DG2034EDN-T1-GE4

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Referenced V+ to GND		-0.3 to +6	V
A_X, EN, S_X, COM [a]		-0.3 to (V+ + 0.3)	
Continuous current (any terminal)		± 50	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 100	
Power dissipation (package) [b]	QFN-12 (3 mm x 3 mm) [c]	1295	mW
	MSOP-10 [d]	320	
Storage temperature (D suffix)		-65 to +150	°C
ESD / HBM	EIA / JESD22-A114-A	8k	V
ESD / CDM	EIA / JESD22-C101-A	2k	
Latch up	JESD78	400	mA

Notes
a. Signals on S_X, COM, EN or A_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 16.2 mV/°C above 70 °C
d. Derate 4 mV/°C above 70 °C

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SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 3 V, ± 10 %, V_{AL} = 0.5 V, V_{AH} = 1.5 V [e]		TEMP.[a]	LIMITS -40 to +85 °C MIN. [c]	TYP. [b]	MAX. [c]	UNIT
Analog Switch								
Analog signal range [d]	V_{ANALOG}			Full	0	-	V+	V
Drain-source On-resistance	$R_{DS(on)}$	V+ = 1.8 V, V_S = 0.4 V / V+, I_S = 8 mA		Room	-	7	10	Ω
				Full	-	-	11	
		V+ = 2.7 V, V_{COM} = 0.8 V / 1.8 V I_{COM} = 10 mA		Room	-	4.6	5.3	
				Full	-	-	5.9	
On-resistance matching	$\Delta R_{DS(on)}$	V+ = 2.7 V, V_{COM} = 0.8 V / 1.4 V / 1.8 V I_{COM} = 10 mA		Room	-	0.02	0.27	
				Full	-	-	0.41	
On-resistance flatness [d, f]	$R_{flat(on)}$			Room	-	0.62	1	
				Full	-	-	1.3	
Off leakage current [g]	$I_{S(off)}$	V+ = 3.3 V, V_S = 1 V / 3 V V_{COM} = 3 V / 1 V, V_{EN} = 0 V		Room	-2	0.01	2	nA
				Full	-5	-	5	
COM off leakage current [g]	$I_{COM(off)}$			Room	-2	0.01	2	
				Full	-5	-	5	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 3.3 V V_{COM} = V_S = 1 V / 3 V		Room	-2	0.01	2	
				Full	-5	-	5	
Digital Control								
Input current [d]	I_A or I_{EN}	$V_{A/EN}$ = 0 V or V+, see truth table		Full	-1	0.05	1	µA
Input high voltage [d]	V_{AH} or V_{ENH}			Full	1.5	1.25	-	V
Input low voltage [d]	V_{AL} or V_{ENL}			Full	-	1	0.5	
Digital input capacitance [d]	C_{IN}			Room	-	3	-	pF
Dynamic Characteristics								
Turn-on time	t_{ON}	V_S = 1.5 V, C_L = 35 pF, R_L = 300 Ω		Room	-	19	29	ns
				Full	-	-	39	
Turn-off time	t_{OFF}			Room	-	16	26	
				Full	-	-	36	
Break-before-make time [d]	t_{BBM}			Room	7	12	-	
				Full	5	-	-	
Transition time	t_{trans}	V_S = 1.5 V / 0 V, V_S = 0 V / 1.5 V, R_L = 300 Ω		Room	-	26	41	
				Full	-	-	51	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 1.5 V, R_{gen} = 0 Ω		Room	-	-2	-	pC
Bandwidth [d]	BW	C_L = 5 pF (set up capacitance)		Room	-	166	-	MHz
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room	-	-67	-	dB
			f = 10 MHz	Room	-	-52	-	
Channel-to-channel crosstalk [d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room	-	-71	-	
			f = 10 MHz	Room	-	-55	-	
Off capacitance [d]	$C_{S(off)}$	V+ = 2.7 V, f = 1 MHz		Room	-	7	-	pF
COM off capacitance [d]	$C_{COM(off)}$			Room	-	27	-	
COM on capacitance [d]	$C_{COM(on)}$			Room	-	33	-	
Power Supply								
Power supply range	V+			Full	2.7	-	3.3	V
Power supply current [d]	I+	V+ = 2.7 V, $V_{A/EN}$ = 0 V or 2.7 V, see truth table		Full	-	-	1	µA

Notes

a. Room = 25 °C, Full = as determined by the operating suffix
b. Typical values are for design aid only, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guarantee by design, not subjected to production test
e. V_A, EN = input voltage to perform proper function
f. Difference of min. and max. values
g. Guaranteed by 5 V testing

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SPECIFICATIONS (V+ = 5 V)

PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 5 V, ± 10 %, V_{AL} = 0.5 V, V_{AH} = 2 V [e]		TEMP.[a]	LIMITS -40 to +85 °C MIN. [c]	TYP. [b]	MAX. [c]	UNIT
Analog Switch								
Analog signal range [d]	V_{ANALOG}			Full	0	-	V+	V
Drain-source On-resistance	$R_{DS(on)}$	V+ = 4.5 V, V_{COM} = 0.8 V / 3.5 V, I_{COM} = 10 mA		Room	-	2.5	3.1	Ω
				Full	-	-	4	
On-resistance matching	$\Delta R_{DS(on)}$	V+ = 4.5 V, V_{COM} = 0.8 V / 2.5 V / 3.5 V, I_{COM} = 10 mA		Room	-	0.02	0.29	
				Full	-	-	0.42	
On-resistance flatness [d, f]	$R_{flat(on)}$			Room	-	0.6	0.9	
				Full	-	-	1.2	
Off leakage current [g]	$I_{S(off)}$	V+ = 5.5 V, V_S = 1 V / 4.5 V, V_{COM} = 4.5 V / 1 V, V_{EN} = 0 V		Room	-2	0.17	2	nA
				Full	-8	-	8	
COM off leakage current [g]	$I_{COM(off)}$			Room	-5	0.77	5	
				Full	-15	-	15	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 5.5 V, V_{COM} = V_S = 1 V / 4.5 V		Room	-5	0.61	5	
				Full	-15	-	15	
Power down leakage [d]	I_{PD}	V+ = 0 V, V_D = 5.5 V, S_X open		Full	-	0.01	5	µA
		V+ = 0 V, V_S = 5.5 V, COM, open		Full	-	0.01	5	
Digital Control								
Input current [d]	I_A or I_{EN}	$V_{A/EN}$ = 0 V or V+, see truth table		Full	-	0.01	1	µA
Input high voltage [d]	V_{AH} or V_{ENH}			Full	2	1.76	-	V
Input low voltage [d]	V_{AL} or V_{ENL}			Full	-	1.3	0.5	
Digital input capacitance [d]	C_{IN}			Room	-	3	-	pF
Dynamic Characteristics								
Turn-on time	t_{ON}	V_S = 3 V, C_L = 35 pF, R_L = 300 Ω		Room	-	13	25	ns
				Full	-	-	35	
Turn-off time	t_{OFF}			Room	-	12	20	
				Full	-	-	30	
Break-before-make time [d]	t_{BBM}			Room	4	10	-	
				Full	3	-	-	
Transition time	t_{trans}	V_S = 3 V / 0 V, V_S = 0 V / 3 V, R_L = 300 Ω		Room	-	17	32	
				Full	-	-	42	
Propagation delay [d]	t_{PD}	V+ = 5 V, no R_{LOAD}		Room	-	537	-	ps
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 2.5 V, R_{gen} = 0 Ω		Room	-	-2.6	-	pC
Bandwidth [d]	BW	C_L = 5 pF (set up capacitance)		Room	-	166	-	MHz
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room	-	-67	-	dB
			f = 10 MHz	Room	-	-52	-	
Channel-to-channel crosstalk [d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room	-	-71	-	
			f = 10 MHz	Room	-	-55	-	
Off capacitance [d]	$C_{S(off)}$	V+ = 5 V, f = 1 MHz		Room	-	7	-	pF
COM off capacitance [d]	$C_{COM(off)}$			Room	-	27	-	
COM on capacitance [d]	$C_{COM(on)}$			Room	-	36	-	
Power Supply								
Power supply range	V+			Full	4.5	-	5.5	V
Power supply current [d]	I+	V+ = 5.5 V, $V_{A/EN}$ = 0 V or 5.5 V, see truth table		Full	-	-	1	µA

Notes

a. Room = 25 °C, Full = as determined by the operating suffix
b. Typical values are for design aid only, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guarantee by design, not subjected to production test
e. V_A, EN = input voltage to perform proper function
f. Difference of min. and max. values
g. Guaranteed by 5 V testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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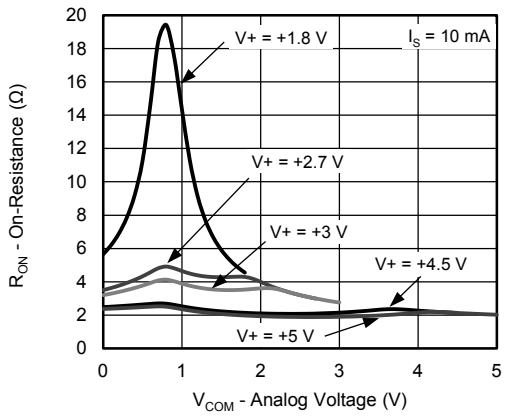
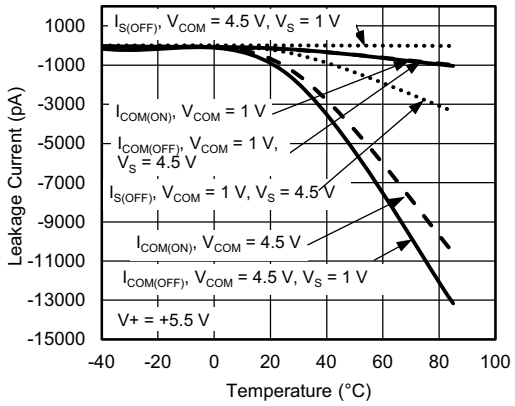
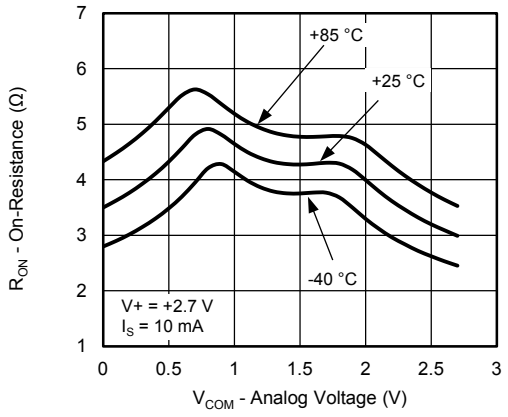


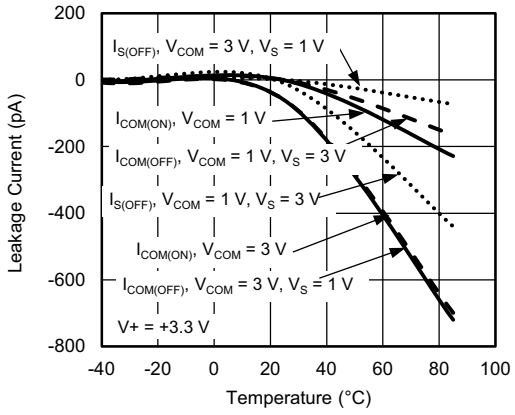
On-Resistance vs. Analog Voltage



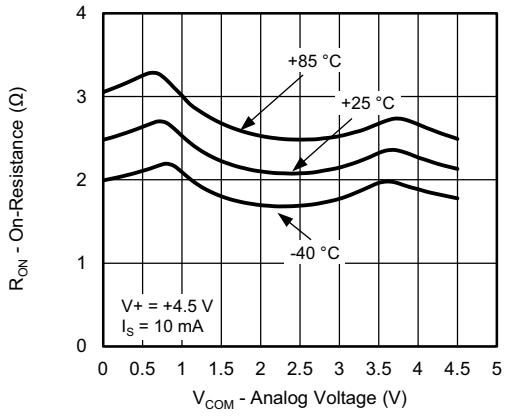
Leakage Current vs. Temperature



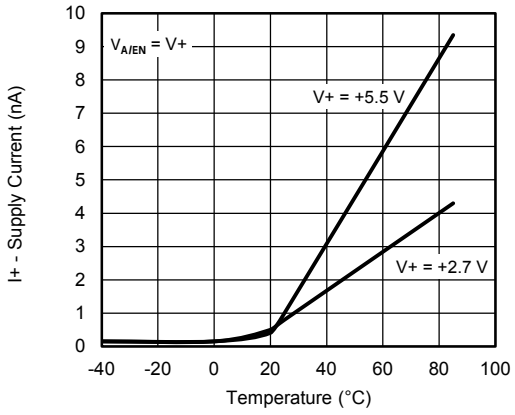
On-Resistance vs. Analog Voltage



Leakage Current vs. Temperature



On-Resistance vs. Analog Voltage



Supply Current vs. Temperature

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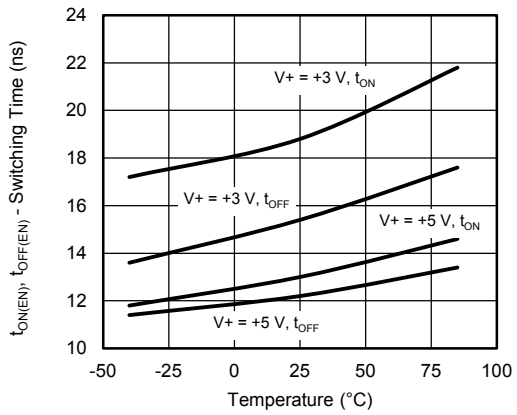
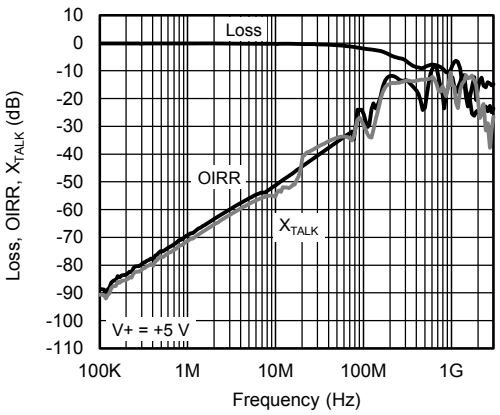
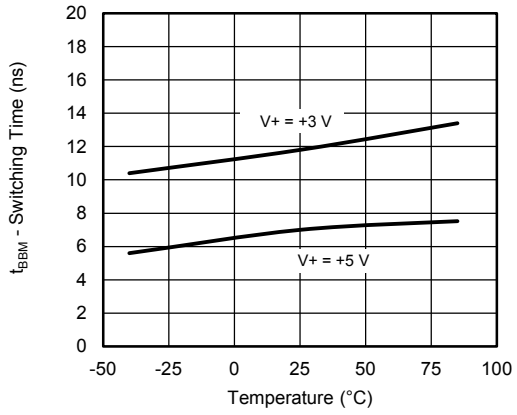


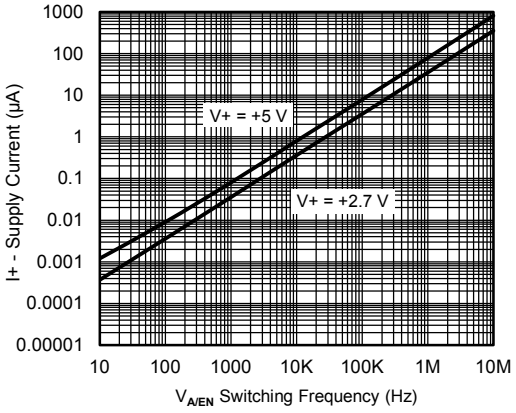
Switching Time vs. Temperature



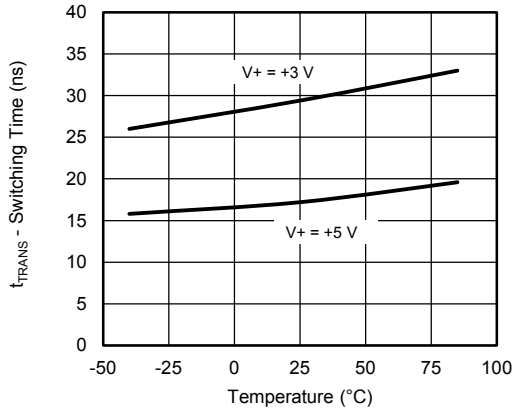
Loss, OIRR, X_{TALK} vs. Frequency



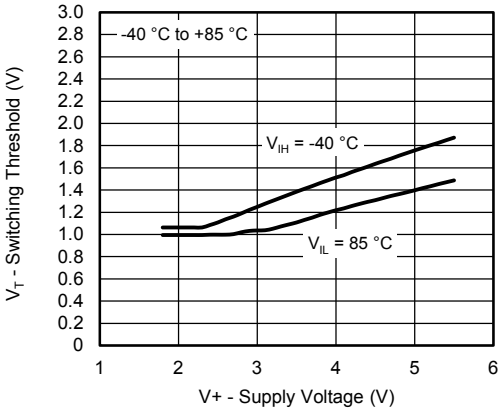
Switching Time vs. Temperature



Positive Supply Current vs. Switching Frequency



Switching Time vs. Temperature



Switching Threshold vs. Supply Voltage

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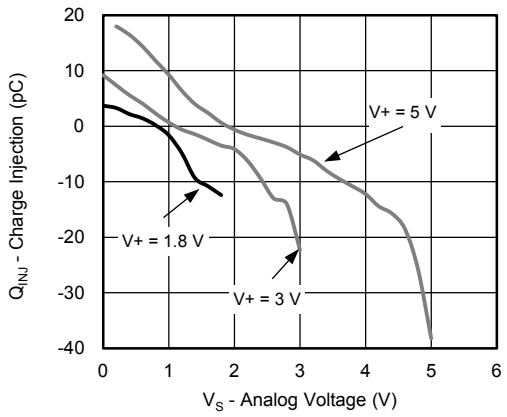
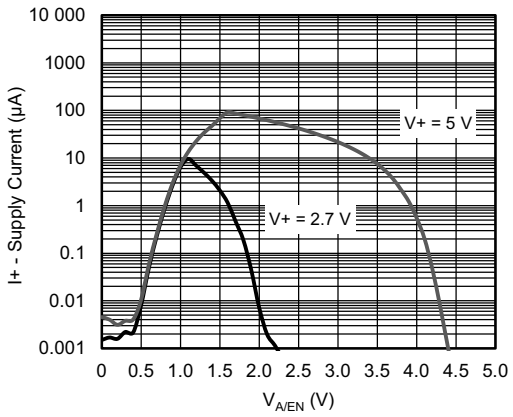
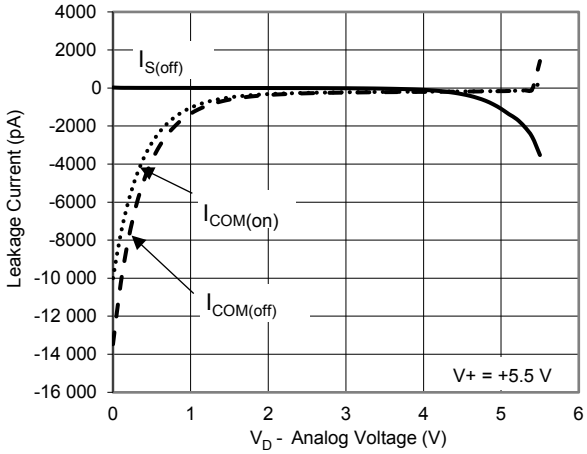


Charge Injection vs. Source Voltage



Positive Supply Current vs. Logic Voltage



Leakage Current vs. Analog Voltage

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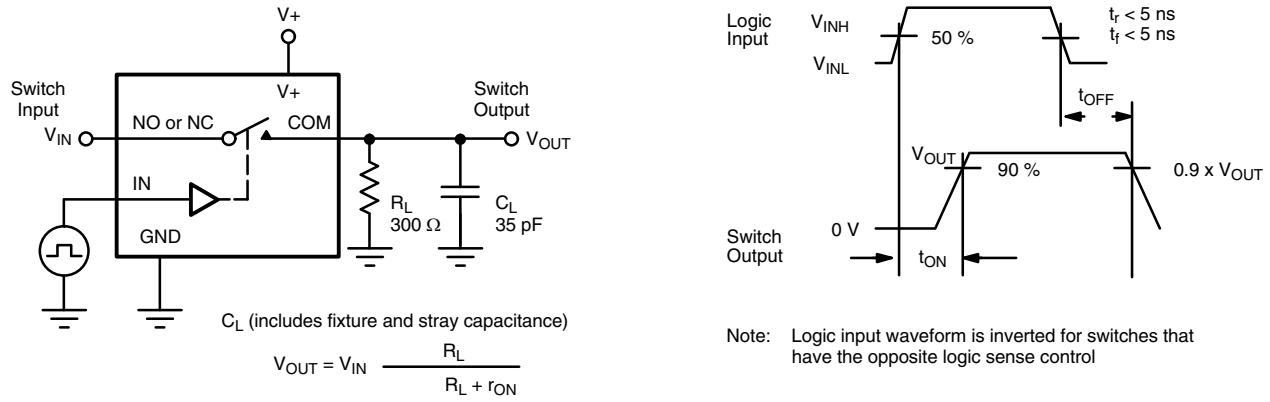
TEST CIRCUITS



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 1 - Switching Time

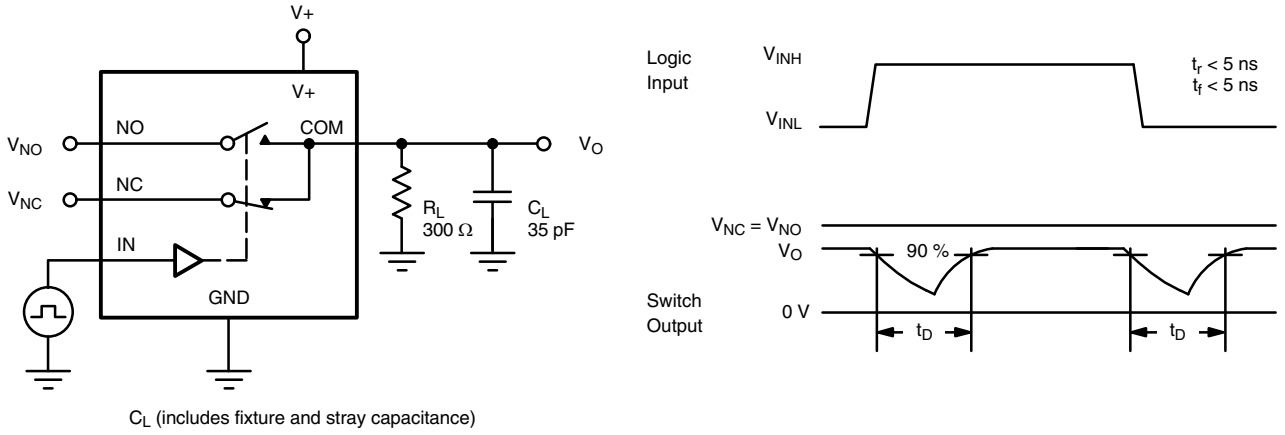


Fig. 2 - Break-Before-Make

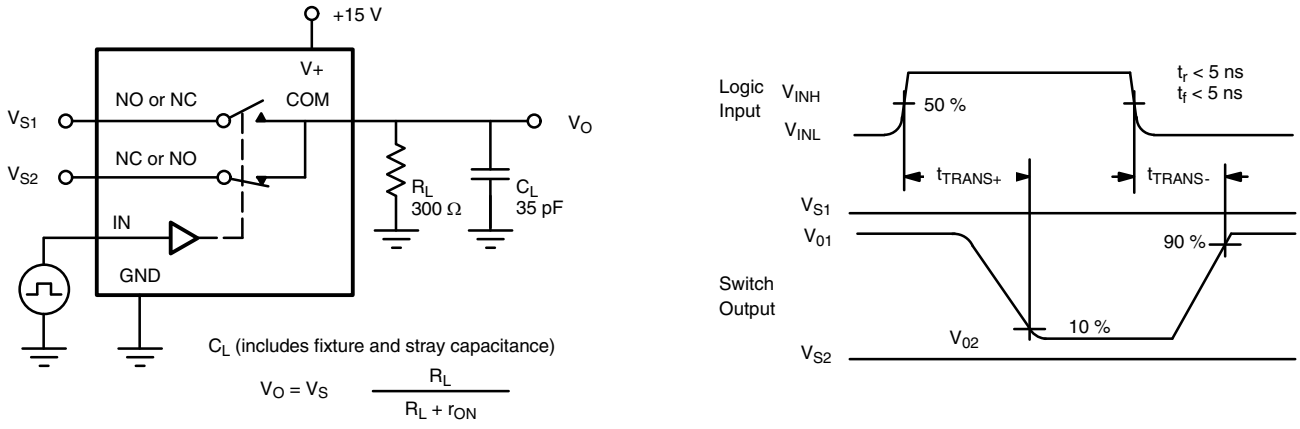


Fig. 3 - Transition Time

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TEST CIRCUITS

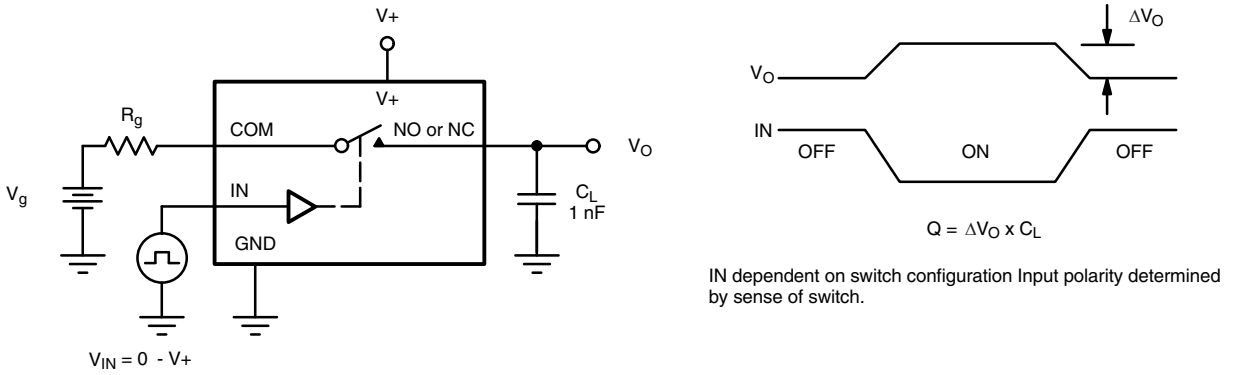

Fig. 4 - Charge Injection

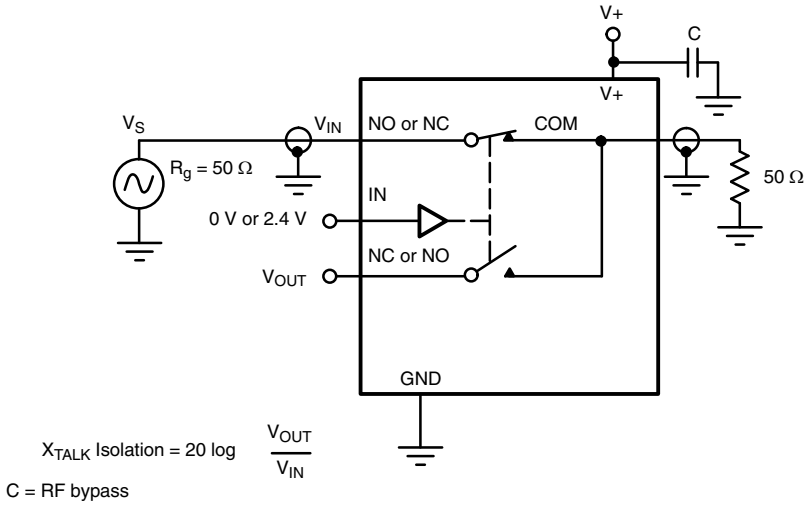

Fig. 5 - Crosstalk

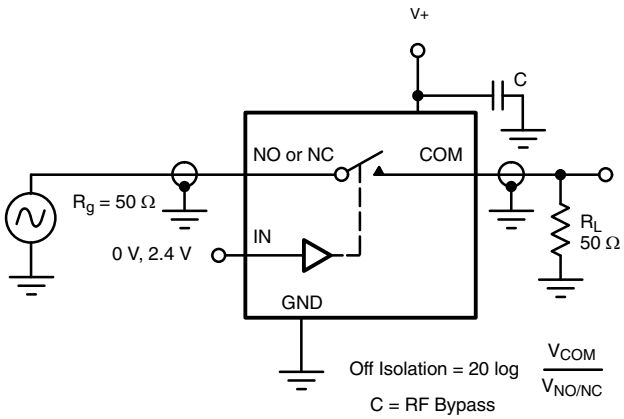

Fig. 6 - Off Isolation

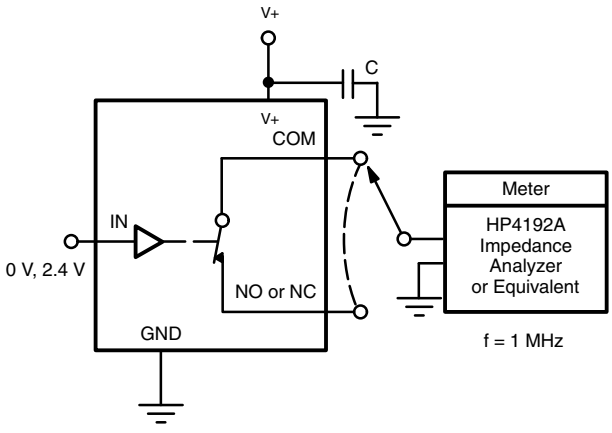

Fig. 7 - Source / Drain Capacitances

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TEST CIRCUITS

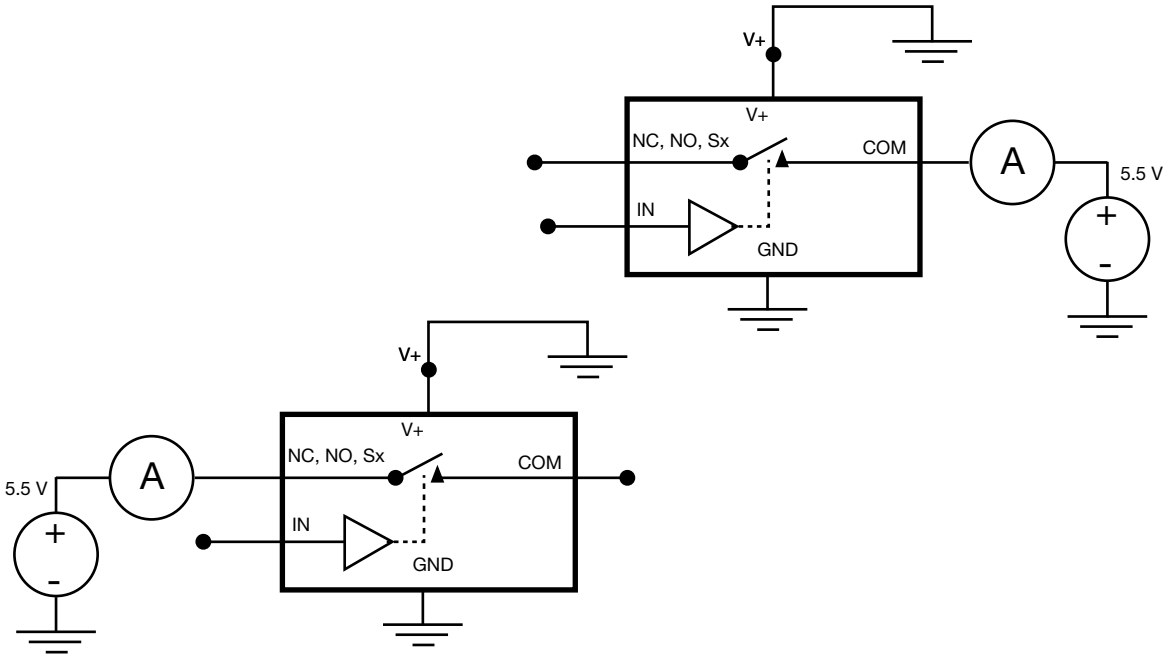

Fig. 8 - Source / Drain Power Down Leakage

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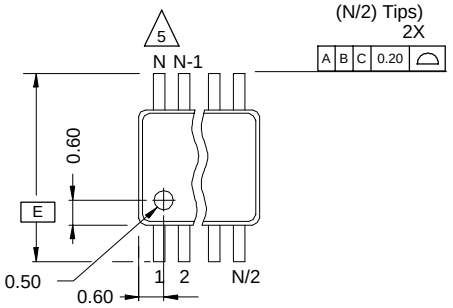
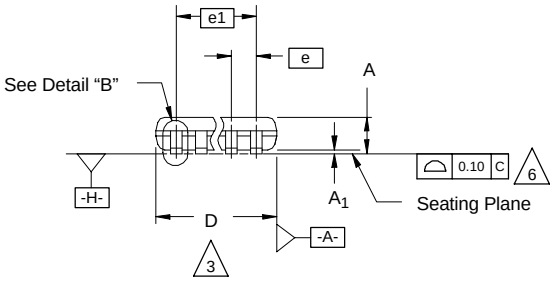
MSOP: 10-LEADS

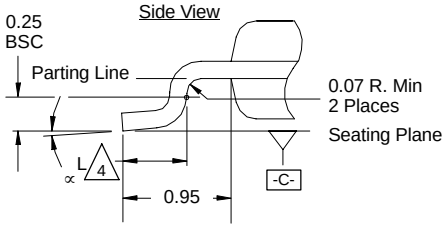
JEDEC Part Number: MO-187, (Variation AA and BA)



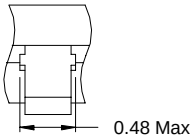
Top View



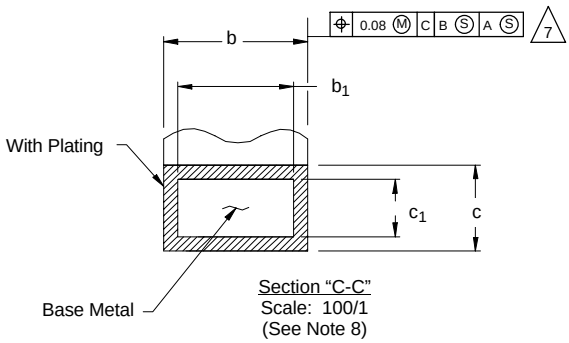
Side View



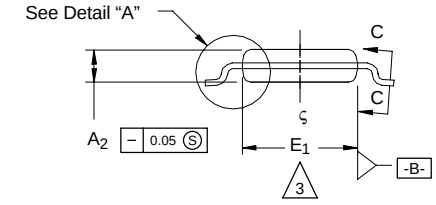
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	-	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

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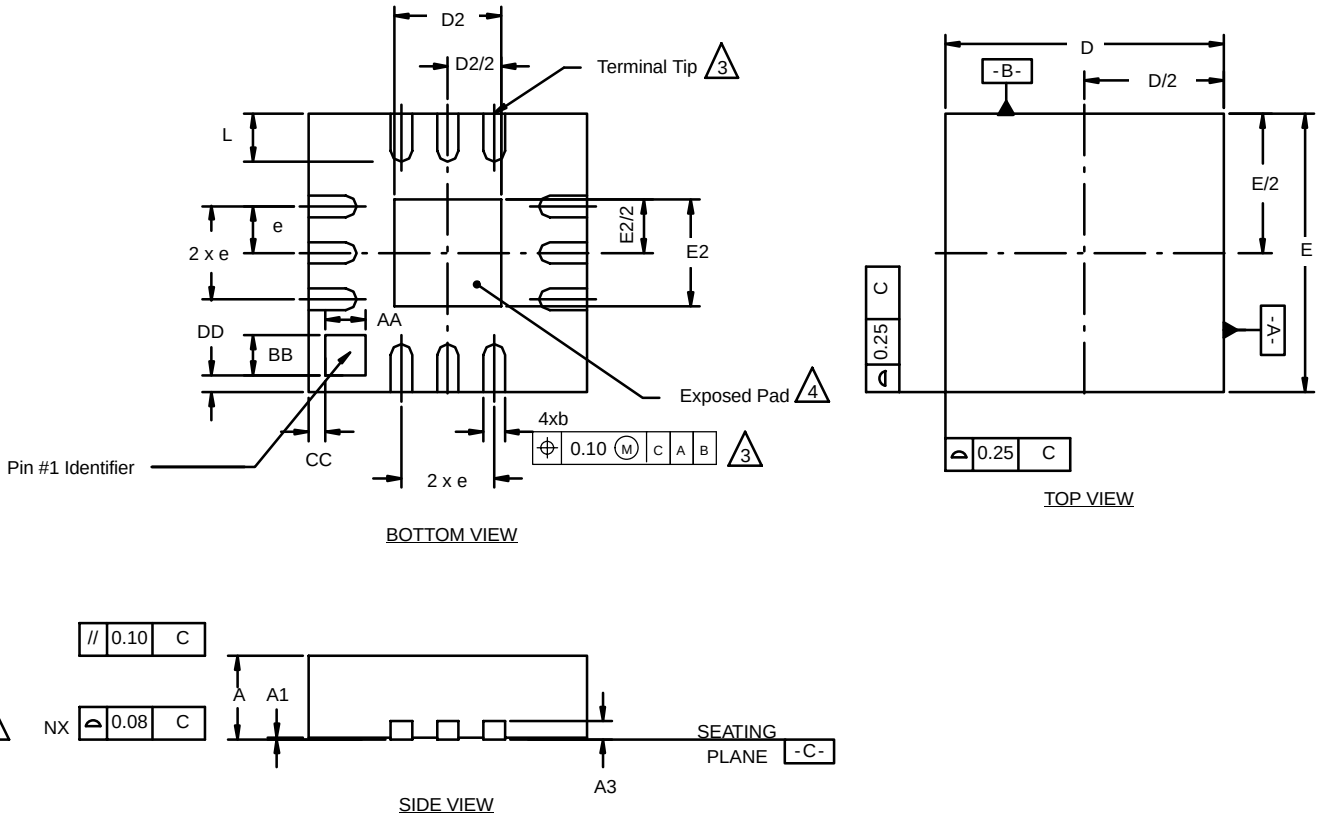
DWG: 5867

QFN-12 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.25 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.90	1.00	0.032	0.035	0.039
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	1.00	1.15	1.25	0.039	0.045	0.049
E		3.00 BSC			0.118 BSC	
E2	1.00	1.15	1.25	0.039	0.045	0.049
e		0.50 BSC			0.02 BSC	
L	0.45	0.55	0.65	0.018	0.022	0.026
AA		0.435			0.017	
BB		0.435			0.017	
CC		0.18			0.007	
DD		0.18			0.007	

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DWG: 5898

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