

## Dual N-Channel 60-V (D-S) 175 °C MOSFET

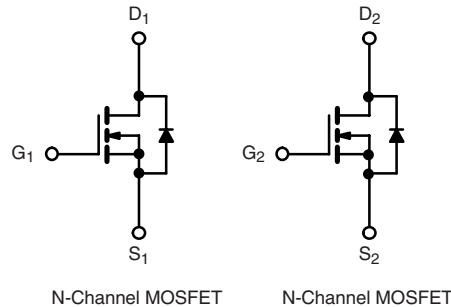
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
60	0.041 at V <sub>GS</sub> = 10 V	6.5	9.2 nC
	0.052 at V <sub>GS</sub> = 4.5 V	5.8	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Maximum Junction Temperature
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



Ordering Information: Si4946BEY-T1-E3 (Lead (Pb)-free)  
Si4946BEY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	6.5
		T <sub>C</sub> = 70 °C	5.5
		T <sub>A</sub> = 25 °C	5.3 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	4.4 <sup>a, b</sup>
Pulsed Drain Current	I <sub>DM</sub>	30	A
Continuous Source Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	2 <sup>a, b</sup>
Avalanche Current	I <sub>AS</sub>	12	mJ
Single-Pulse Avalanche Energy	E <sub>AS</sub>	7.2	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.7
		T <sub>C</sub> = 70 °C	2.6
		T <sub>A</sub> = 25 °C	2.4 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	1.7 <sup>a, b</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, c</sup>	R <sub>thJA</sub>	50	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	33	41		

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W.

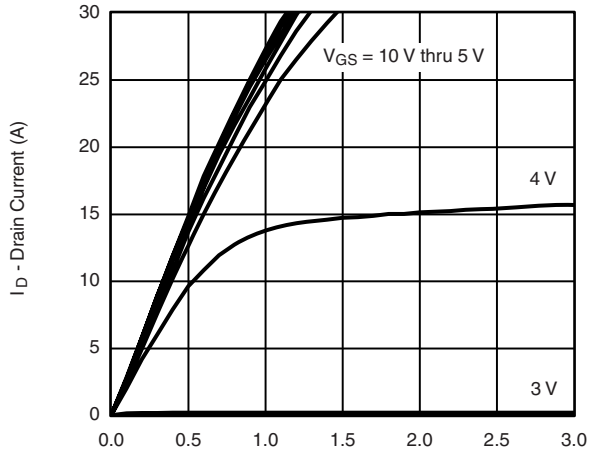
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		53		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	2.4	3.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5.3\text{ A}$		0.033	0.041	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 4.7\text{ A}$		0.041	0.052	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 5.3\text{ A}$		24		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		840		pF
Output Capacitance	$C_{oss}$			71		
Reverse Transfer Capacitance	$C_{rss}$			44		
Total Gate Charge	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 5.3\text{ A}$		17	25	nC
		$V_{DS} = 30\text{ V}, V_{GS} = 5\text{ V}, I_D = 5.3\text{ A}$		9.2	12	
Gate-Source Charge	$Q_{gs}$			3.3		
Gate-Drain Charge	$Q_{gd}$			3.7		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	3.1	6.5	9.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 6.8\text{ }\Omega$ $I_D \cong 4.4\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	$t_r$			120	180	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	$t_f$			30	45	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 6.8\text{ }\Omega$ $I_D \cong 4.4\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			3.1	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				30	
Body Diode Voltage	$V_{SD}$	$I_S = 2\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 4.4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	50	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			25	50	nC
Reverse Recovery Fall Time	$t_a$			18		ns
Reverse Recovery Rise Time	$t_b$			7		

## Notes:

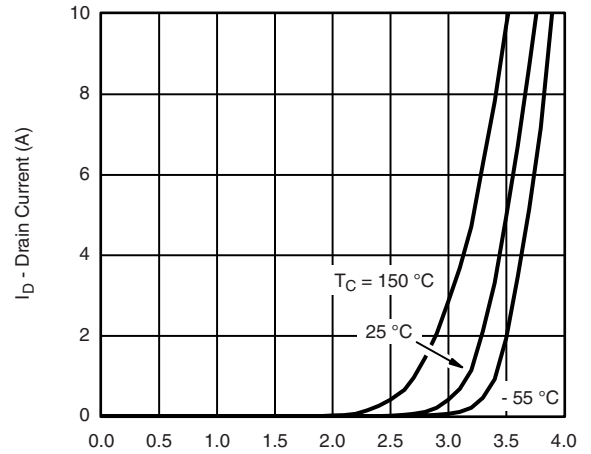
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

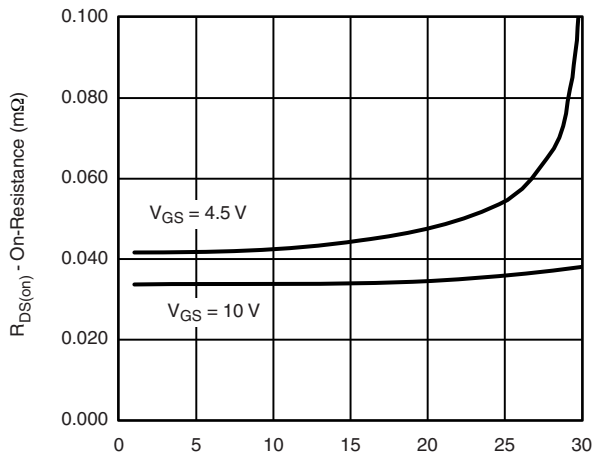
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



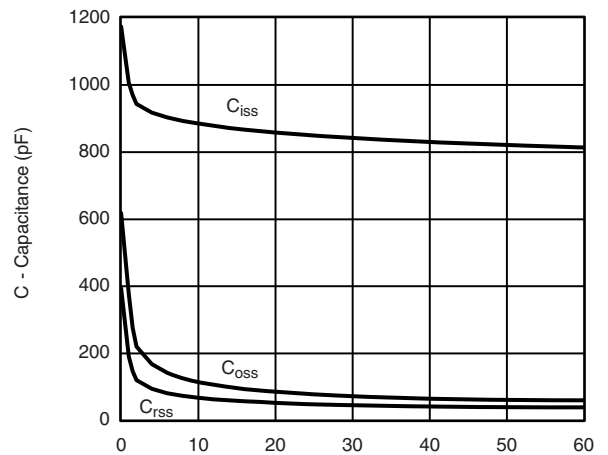
**Output Characteristics**



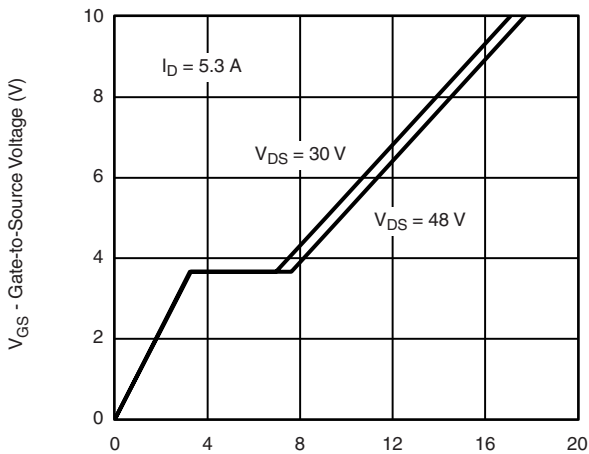
**Transfer Characteristics**



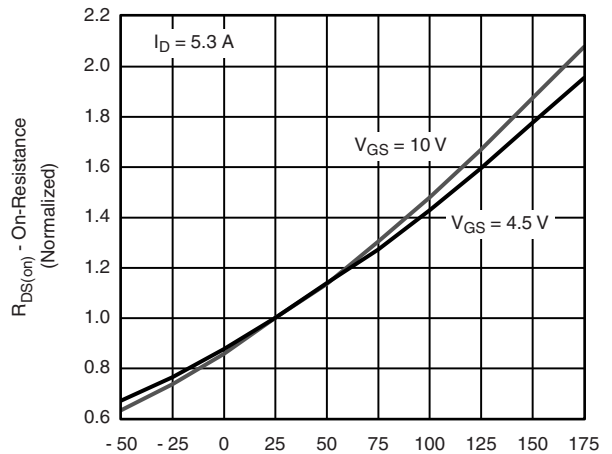
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

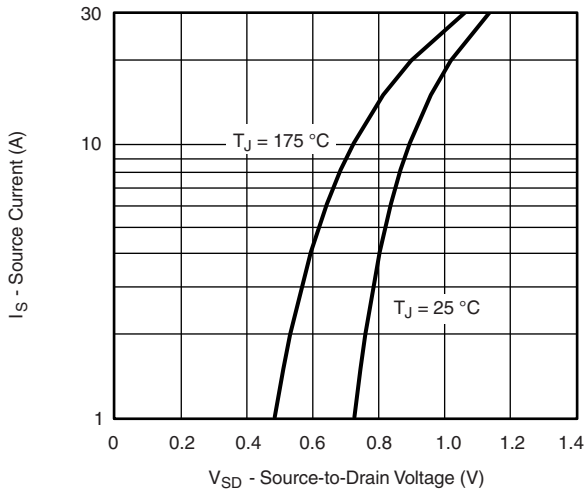


**Gate Charge**

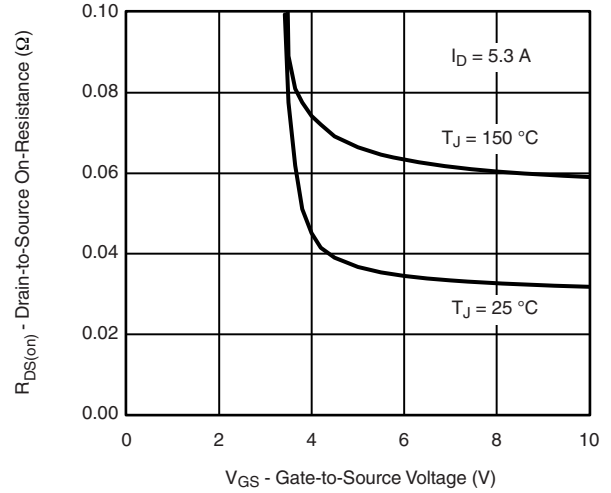


**On-Resistance vs. Junction Temperature**

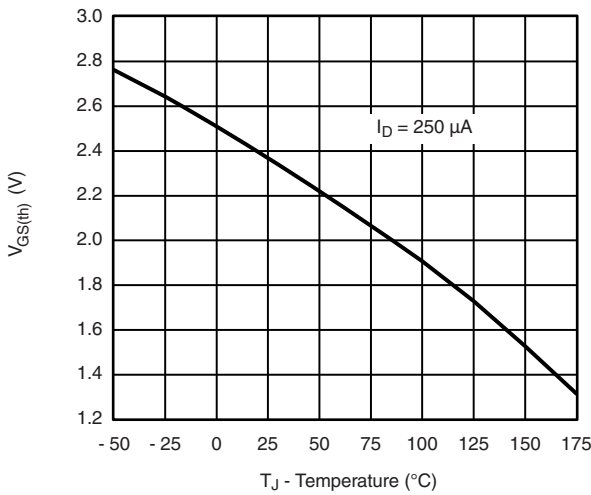
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



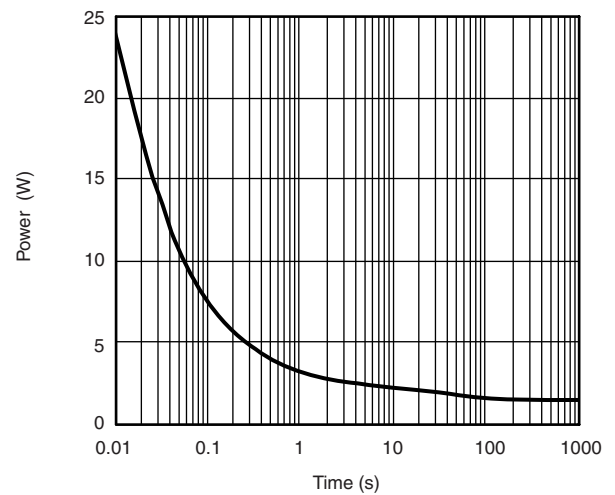
**Source-Drain Diode Forward Voltage**



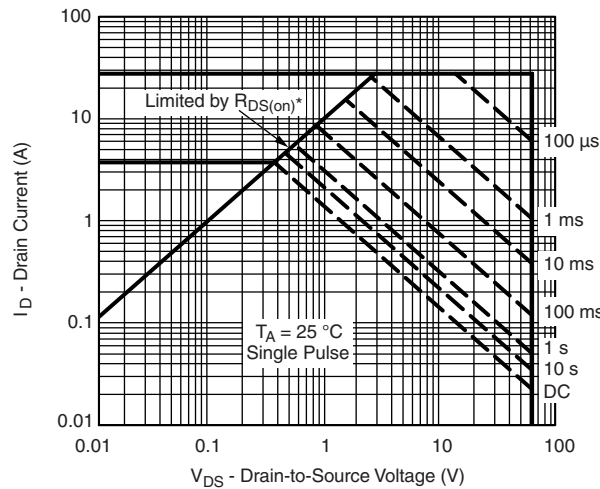
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

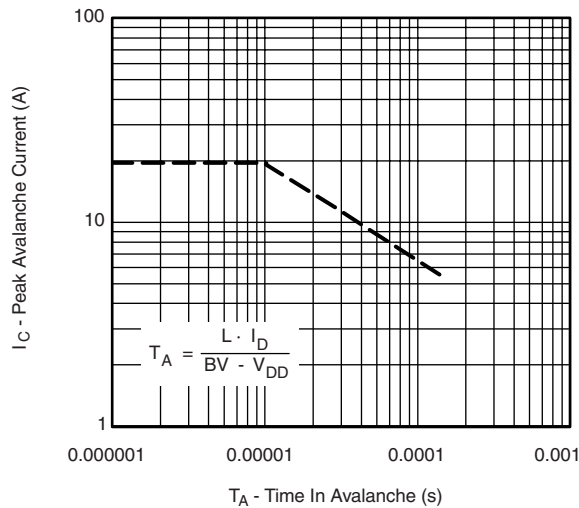
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



$T_C$  - Case Temperature (°C)  
**Current Derating\***



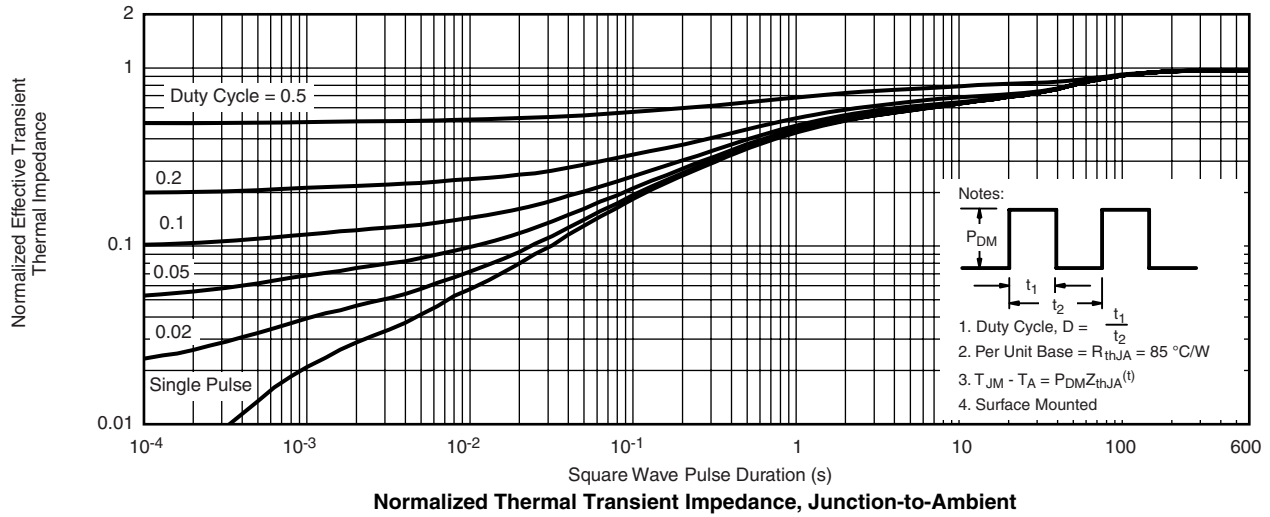
$T_C$  - Case Temperature (°C)  
**Power, Junction-to-Case**



**Single Pulse Avalanche Capability**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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