Low Capacitance, Low Charge Injection, 4- / 8-Channel, Triple SPDT, ± 5 V / 12 V / 5 V / 3 V Analog Multiplexers

DESCRIPTION

The DG4051E, DG4052E, and DG4053E are high precision CMOS analog multiplexers. The DG4051E is an 8-channel multiplexer, the DG4052E is a dual 4-channel multiplexer, and the DG4053E is a triple 2-channel multiplexer or triple SPDT.

The DG4051E, DG4052E, and DG4053E feature low leakage, parasitic capacitance, and low charge injection of 0.3 pC over the full voltage range. These devices are ideal for high precision signal switching and multiplexing.

Designed to operate from a 3 V to 16 V single supply or from a ± 3 V to ± 8 V dual supplies, the DG4051E, DG4052E, and DG4053E are fully specified at 3 V, 5 V, 12 V and ± 5 V. All control logic inputs have guaranteed 2 V logic high limit when operating from 5 V or ± 5 V supplies and 1.4 V when operating from a 3 V supply.

All switches conduct equally well in both directions, offering rail to rail analog signal switching and can be used both as multiplexers as well as de-multiplexers.

The DG4051E, DG4052E, and DG4053E operating temperature is specified from -40 °C to +125 °C and are available in 16 pin TSSOP and the ultra compact 1.8 mm x 2.6 mm miniQFN16 packages.

BENEFITS

- Wide operation voltage range
- Low charge injection
- Low parasitic capacitance
- Compact package option

FEATURES

- 3 V to 16 V single supply or ± 3 to ± 8 V dual supply operation
- Low parasitic capacitance:
  $C_{D(ON)}$: 8.5 pF / typ. (DG4053E)
  $C_{S(OFF)}$: 2.0 pF / typ. (DG4053E)
- Less than 0.3 pC charge injection over the full signal swing range
- Low leakage: < 50 pA, typ.
- Fast switching t_{ON}: 35 ns, typ.
- 3 V logic compatible for control
- Bi-directional rail to rail signal switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

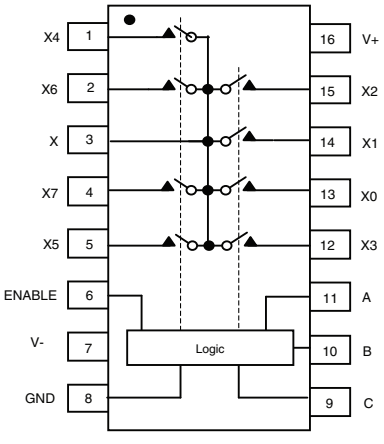
RoHS COMPLIANT

APPLICATIONS

- Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems

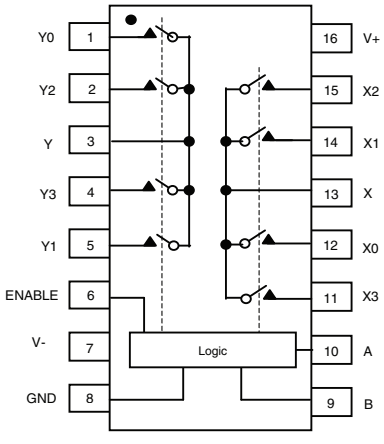
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG4051E
TSSOP16



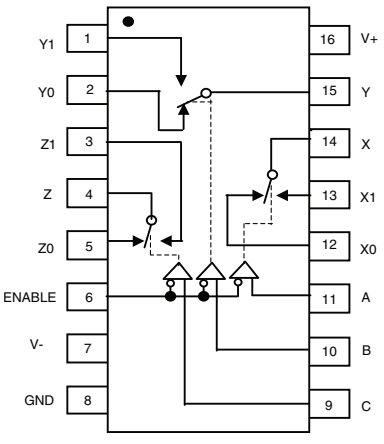
Top View

DG4052E
TSSOP16



Top View

DG4053E
TSSOP16

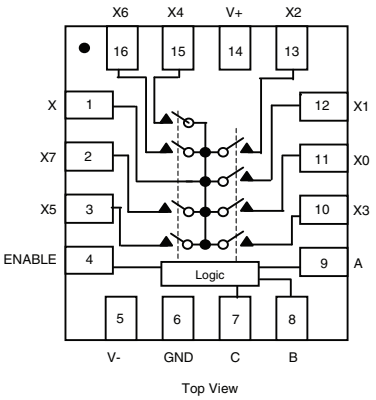


Top View

ENABLE = LO, all switches are controlled by addr pins.
ENABLE = HI, all switches are off.

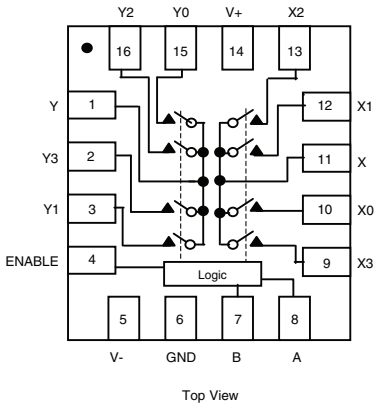
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG4051E
mQFN-16



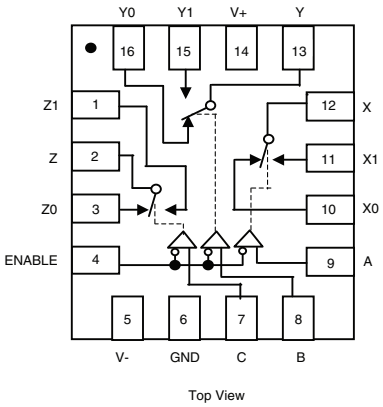
Top View

DG4052E
mQFN-16

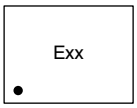


Top View

DG4053E
mQFN-16



Top View



Device Marking: Fxx for DG4051E
(miniQFN16) Gxx for DG4052E
Hxx for DG4053E
xx = Date/Lot Traceability Code

TRUTH TABLE

ENABLE INPUT	SELECT INPUTS			ON SWITCHES		
	C	B	A	DG4051E	DG4052E	DG4053E
H	X	X	X	All switches open	All switches open	All switches open
L	L	L	L	X to X0	X to X0, Y to Y0	X to X0, Y to Y0, Z to Z0
L	L	L	H	X to X1	X to X1, Y to Y1	X to X1, Y to Y0, Z to Z0
L	L	H	L	X to X2	X to X2, Y to Y2	X to X0, Y to Y1, Z to Z0
L	L	H	H	X to X3	X to X3, Y to Y3	X to X1, Y to Y1, Z to Z0
L	H	L	L	X to X4	X to X0, Y to Y0	X to X0, Y to Y0, Z to Z1
L	H	L	H	X to X5	X to X1, Y to Y1	X to X1, Y to Y0, Z to Z1
L	H	H	L	X to X6	X to X2, Y to Y2	X to X0, Y to Y1, Z to Z1
L	H	H	H	X to X7	X to X3, Y to Y3	X to X1, Y to Y1, Z to Z1

ORDERING INFORMATION

TEMPERATURE RANGE	CONFIGURATION	PACKAGE	PART NUMBER	MIN. ORDER / PACKAGING QUANTITY
-40 °C to +125 °C [a] Lead (Pb)-Free	DG4051E	16-pin TSSOP	DG4051EEQ-T1-GE3	Tape and reel 3000 units
		16-pin SOIC	DG4051EEY-T1-GE3	Tape and reel 2500 units
		16-pin miniQFN	DG4051EEN-T1-GE4	Tape and reel 3000 units
	DG4052E	16-pin TSSOP	DG4052EEQ-T1-GE3	Tape and reel 3000 units
		16-pin SOIC	DG4052EEY-T1-GE3	Tape and reel 2500 units
		16-pin miniQFN	DG4052EEN-T1-GE4	Tape and reel 3000 units
	DG4053E	16-pin TSSOP	DG4053EEQ-T1-GE3	Tape and reel 3000 units
		16-pin SOIC	DG4053EEY-T1-GE3	Tape and reel 2500 units
		16-pin miniQFN	DG4053EEN-T1-GE4	Tape and reel 3000 units

Note

a. -40 °C to +85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
PARAMETER		**LIMIT**	**UNIT**
V+ to V-		-0.3 to +18	V
GND to V-		-18	
Digital Inputs [a], V_S, V_D		(V-) - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first	
Continuous Current (any terminal)		30	mA
Peak Current, S or D (pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature		-65 to +150	°C
Power Dissipation [b]	16-pin TSSOP [c]	450	mW
	16-pin miniQFN [d, f]	525	
	16-pin narrow SOIC [e]	640	
Thermal Resistance [b]	16-pin TSSOP [c]	178	°C/W
	16-pin miniQFN [d, f]	152	
	16-pin narrow SOIC [e]	125	
ESD Human Body Model (HBM); per ANSI / ESDA / JEDEC® JS-001		2500	V
Latch Up Current, per JESD78D		400	mA

Notes

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 5.6 mW/°C above 70 °C.
d. Derate 6.6 mW/°C above 70 °C.
e. Derate 8.0 mW/°C above 70 °C.
f. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS FOR DUAL SUPPLIES									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, V- = -5 V $V_{IN(A, B, C, and enable)}$ = 2 V, 0.8 V [a]	**TEMP.** [b]	**TYP.** [c]	-40 °C to +125 °C		-40 °C to +85 °C		**UNIT**
					MIN. [d]	**MAX.** [d]	**MIN.** [d]	**MAX.** [d]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	-5	5	-5	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = -3 V, 0 V, 3 V	Room	68	-	78	-	78	Ω
			Full	-	-	106	-	97	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = ± 3 V	Room	0.91	-	6	-	6	
			Full	-	-	6	-	6	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = -3 V, 0 V, 3 V	Room	10	-	17	-	17	
			Full	-	-	20	-	19	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V, V_D = ± 4.5 V, V_S = ∓ 4.5 V	Room	± 0.05	-1	1	-1	1	nA
			Full	-	-50	50	-5	5	
	$I_{D(off)}$		Room	± 0.05	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_S = V_D = ± 4.5 V	Room	± 0.05	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	$V_{IN(A, B, C, and enable)}$ under test = 0.6 V	Full	0.02	-1	1	-1	1	µA
Input Current, V_{IN} High	I_{IH}	$V_{IN(A, B, C, and enable)}$ under test = 2 V	Full	0.02	-1	1	-1	1	
Input Capacitance [e]	C_{IN}	f = 1 MHz	Room	3.4	-	-	-	-	pF

SPECIFICATIONS FOR DUAL SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = -5 V $V_{IN(A, B, C, and enable)}$ = 2 V, 0.8 V [a]		TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
						MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Dynamic Characteristics										
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 1 pF	f = 100 kHz	Room	-106	-	-	-	-	dB
			f = 10 MHz	Room	-68	-	-	-	-	
			f = 100 MHz	Room	-49	-	-	-	-	
Channel-to-Channel Crosstalk [e]	X_{TALK}		f = 100 kHz	Room	-105	-	-	-	-	
			f = 10 MHz	Room	-62	-	-	-	-	
			f = 100 MHz	Room	-51	-	-	-	-	
Bandwidth, 3 dB	BW	R_L = 50 Ω	DG4051E	Room	308	-	-	-	-	MHz
			DG4052E	Room	353	-	-	-	-	
			DG4053E	Room	930	-	-	-	-	
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see Fig. 1, 2, 3		Room	72	-	112	-	112	ns
				Full	-	-	139	-	131	
Enable Turn-On Time	t_{ON}			Room	35	-	75	-	75	
				Full	-	-	86	-	80	
Enable Turn-Off Time	t_{OFF}			Room	48	-	88	-	88	
				Full	-	-	97	-	95	
Break-Before-Make Time Delay	t_D			Room	-	1	-	1	-	
				Full	-	-	-	-	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Room	0.38	-	-	-	-	pC
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG4051E	Room	2.2	-	-	-	-	pF
			DG4052E	Room	2.1	-	-	-	-	
			DG4053E	Room	2	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG4051E	Room	9.2	-	-	-	-	
			DG4052E	Room	4.8	-	-	-	-	
			DG4053E	Room	3.1	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG4051E	Room	14.9	-	-	-	-	
			DG4052E	Room	10	-	-	-	-	
			DG4053E	Room	8.5	-	-	-	-	
Total Harmonic Distortion [e]	THD	Signal = 5 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω		Room	0.065	-	-	-	-	%
Power Supplies										
Power Supply Current	I+	V+ = 5 V, V- = -5 V $V_{IN(A, B, C, and enable)}$ = 0 V or 5 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V $V_{IN(A, B, C, and enable)}$ = 2 V, 0.8 V [a]		TEMP. [b]	TYP. [c]	-40 °C to +125 °C MIN. [d]	-40 °C to +125 °C MAX. [d]	-40 °C to +85 °C MIN. [d]	-40 °C to +85 °C MAX. [d]	UNIT
Analog Switch										
Analog Signal Range [e]	V_{ANALOG}			Full	-	0	12	0	12	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0.7 V, 11.3 V		Room	85	-	103	-	103	Ω
				Full	-	-	133	-	125	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = 11.3 V		Room	1.24	-	8	-	8	
				Full	-	-	8	-	8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0.7 V, 11.3 V		Room	27	-	37	-	37	
				Full	-	-	44	-	43	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 13.2 V, V- = 0 V V_D = 1 V / 12.2 V, V_S = 12.2 V / 1 V		Room	± 0.05	-1	1	-1	1	nA
				Full	-	-50	50	-5	5	
	$I_{D(off)}$			Room	± 0.05	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 13.2 V, V- = 0 V V_D = V_S = 1 V / 12.2 V		Room	± 0.05	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Digital Control										
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C, and enable)}$ under test = 0.8 V		Full	0.02	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C, and enable)}$ under test = 2 V		Full	0.02	-1	1	-1	1	
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see Fig. 1, 2, 3		Room	43	-	83	-	83	ns
				Full	-	-	95	-	90	
Enable Turn-On Time	t_{ON}			Room	22	-	62	-	62	
				Full	-	-	71	-	67	
Enable Turn-Off Time	t_{OFF}			Room	47	-	87	-	87	
				Full	-	-	94	-	93	
Break-Before-Make Time Delay	t_D			Room	25	1	-	1	-	
				Full	-	-	-	-	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Full	-	-	-	-	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 1 pF f = 100 kHz		Room	-	-	-	-	-	dB
Channel-to-Channel Crosstalk [e]	X_{TALK}			Room	-	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG4051E	Room	-	-	-	-	-	pF
			DG4052E	Room	-	-	-	-	-	
			DG4053E	Room	-	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG4051E	Room	-	-	-	-	-	
			DG4052E	Room	-	-	-	-	-	
			DG4053E	Room	-	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG4051E	Room	-	-	-	-	-	
			DG4052E	Room	-	-	-	-	-	
			DG4053E	Room	-	-	-	-	-	
Power Supplies										
Power Supply Current	I+	$V_{IN(A, B, C, and enable)}$ = 0 V or 5 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = 0 V $V_{IN(A, B, C, and enable)}$ = 2 V, 0.8 V [a]		TEMP. [b]	TYP. [c]	-40 °C to +125 °C MIN. [d]	-40 °C to +125 °C MAX. [d]	-40 °C to +85 °C MIN. [d]	-40 °C to +85 °C MAX. [d]	UNIT
Analog Switch										
Analog Signal Range [e]	V_{ANALOG}			Full	-	0	5	0	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0 V, 3.5 V		Room	125	-	147	-	147	Ω
				Full	-	-	176	-	168	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = 3.5 V		Room	1.3	-	8	-	8	
				Full	-	-	8	-	8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0 V, 3 V		Room	21	-	31	-	31	
				Full	-	-	25	-	29	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V V_D = 1 V / 4.5 V, V_S = 4.5 V / 1 V		Room	± 0.03	-1	1	-1	1	nA
				Full	-	-50	50	-5	5	
	$I_{D(off)}$			Room	± 0.03	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V V_D = V_S = 1 V / 4.5 V		Room	± 0.03	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Digital Control										
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C, and enable)}$ under test = 0.6 V		Full	0.02	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C, and enable)}$ under test = 2 V		Full	0.02	-1	1	-1	1	
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see Fig. 1, 2, 3		Room	95	-	135	-	135	ns
				Full	-	-	169	-	148	
Enable Turn-On Time	t_{ON}			Room	56	-	96	-	96	
				Full	-	-	117	-	107	
Enable Turn-Off Time	t_{OFF}			Room	55	-	95	-	95	
				Full	-	-	110	-	103	
Break-Before-Make Time Delay	t_D			Room	-	12	-	12	-	
				Full	-	-	-	-	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Full	0.32	-	-	-	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 1 pF f = 100 kHz		Room	-86	-	-	-	-	dB
Channel-to-Channel Crosstalk [e]	X_{TALK}			Room	-105	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG4051E	Room	2.4	-	-	-	-	pF
			DG4052E	Room	2.4	-	-	-	-	
			DG4053E	Room	2.3	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG4051E	Room	10.1	-	-	-	-	
			DG4052E	Room	5.3	-	-	-	-	
			DG4053E	Room	3.4	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG4051E	Room	15.9	-	-	-	-	
			DG4052E	Room	10.6	-	-	-	-	
			DG4053E	Room	8.9	-	-	-	-	
Power Supplies										
Power Supply Current	I+	$V_{IN(A, B, C, and enable)}$ = 0 V or 5 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

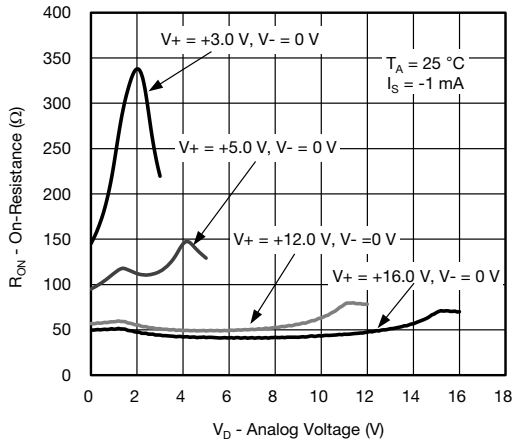
SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V- = 0 V $V_{IN(A, B, C, and enable)}$ = 1.4 V, 0.6 V [a]		TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
						MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch										
Analog Signal Range [e]	V_{ANALOG}			Full	-	0	3	0	3	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 1.5 V		Room	221	-	-	-	-	Ω
				Full	-	-	-	-	-	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 3.3 V, V- = 0 V V_D = 0.3 V / 3 V, V_S = 3 V / 0.3 V		Room	± 0.02	-1	1	-1	1	nA
				Full	-	-50	50	-5	5	
	$I_{D(off)}$			Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V V_D = V_S = 0.3 V / 3 V		Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Digital Control										
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C, and enable)}$ under test = 0.6 V		Full	0.02	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C, and enable)}$ under test = 1.4 V		Full	0.02	-1	1	-1	1	
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see Fig. 1, 2, 3		Room	200	-	-	-	-	ns
				Full	-	-	-	-	-	
Enable Turn-On Time	t_{ON}			Room	130	-	-	-	-	
				Full	-	-	-	-	-	
Enable Turn-Off Time	t_{OFF}			Room	78	-	-	-	-	
				Full	-	-	-	-	-	
Break-Before-Make Time Delay	t_D			Room	130	-	-	-	-	
				Full	-	-	-	-	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Room	0.34	-	-	-	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 1 pF f = 100 kHz		Room	-88	-	-	-	-	dB
Channel-to-Channel Crosstalk [e]	X_{TALK}			Room	-105	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG4051E	Room	2.6	-	-	-	-	pF
			DG4052E	Room	2.6	-	-	-	-	
			DG4053E	Room	2.5	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG4051E	Room	10.7	-	-	-	-	
			DG4052E	Room	5.7	-	-	-	-	
			DG4053E	Room	3.6	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG4051E	Room	16.4	-	-	-	-	
			DG4052E	Room	10.9	-	-	-	-	
			DG4053E	Room	9.1	-	-	-	-	
Power Supplies										
Power Supply Current	I+	$V_{IN(A, B, C, and enable)}$ = 0 V or 3 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

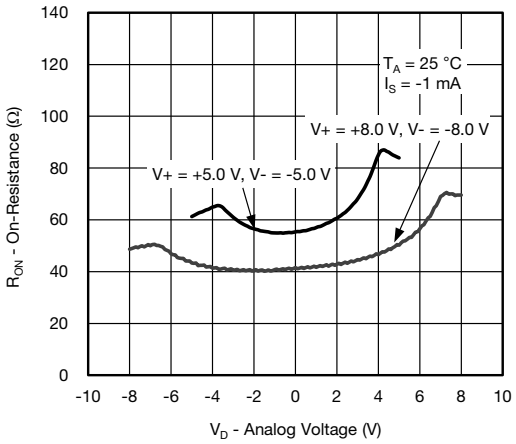
Notes

a. V_{IN} = input voltage to perform proper function.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.

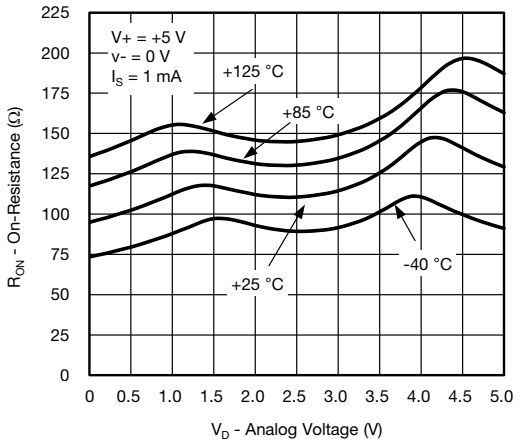
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



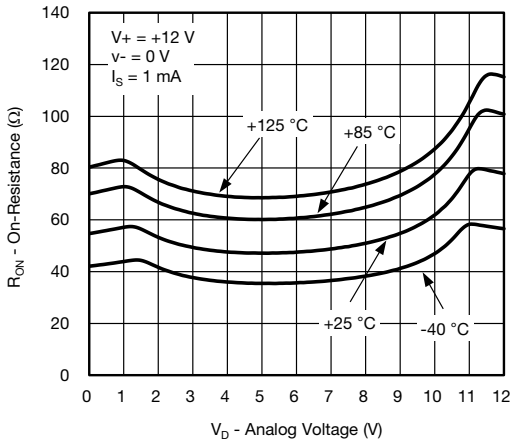
On-Resistance vs. Analog Voltage (Single Supply)



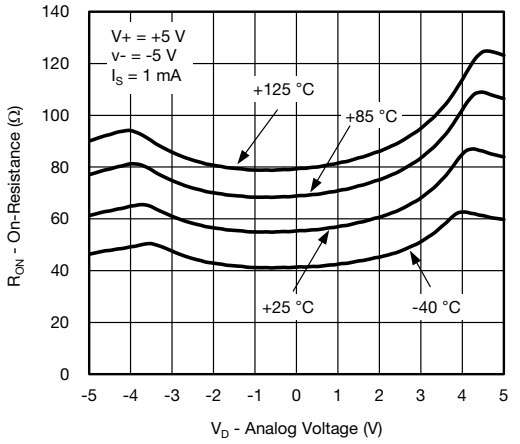
On-Resistance vs. Analog Voltage (Dual Supply)



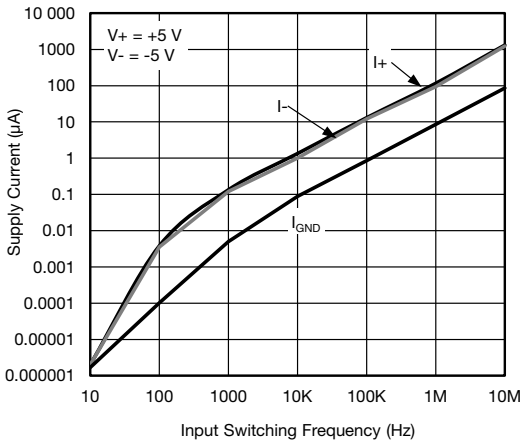
On-Resistance vs. Analog Voltage (Temperature)



On-Resistance vs. Analog Voltage (Temperature)

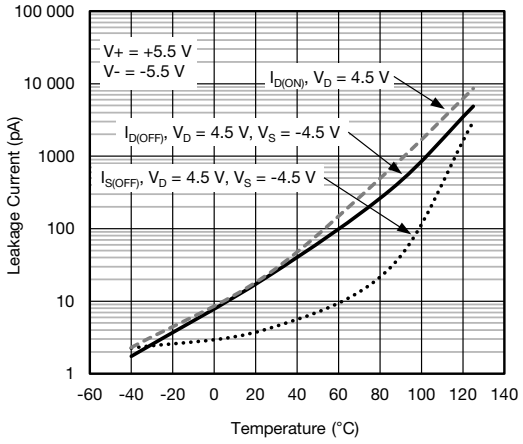


On-Resistance vs. Analog Voltage (Temperature)

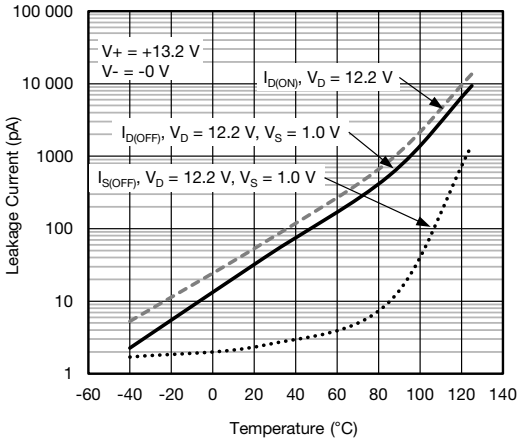


Supply Current vs. Input Switching Frequency

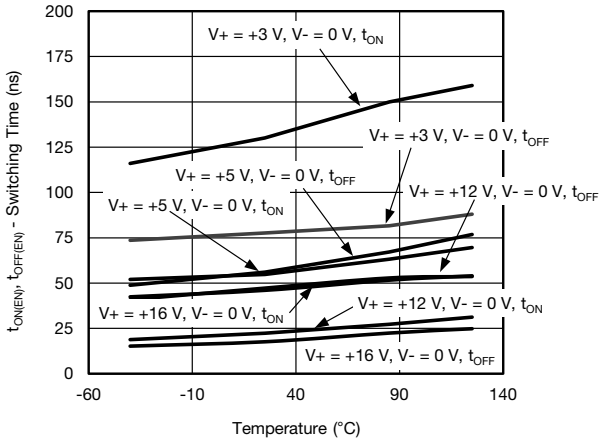
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



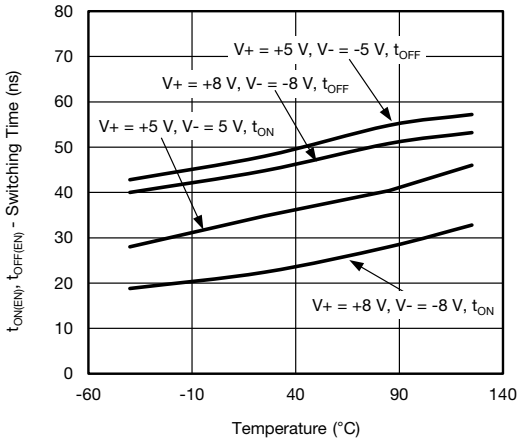
Leakage Current vs. Temperature



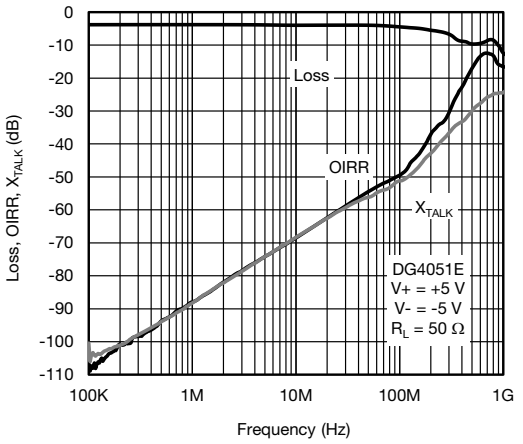
Leakage Current vs. Temperature



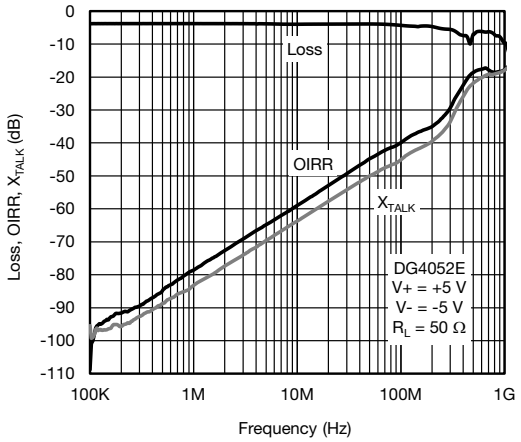
Switching Time vs. Temperature (Single Supply)



Switching Time vs. Temperature (Dual Supply)

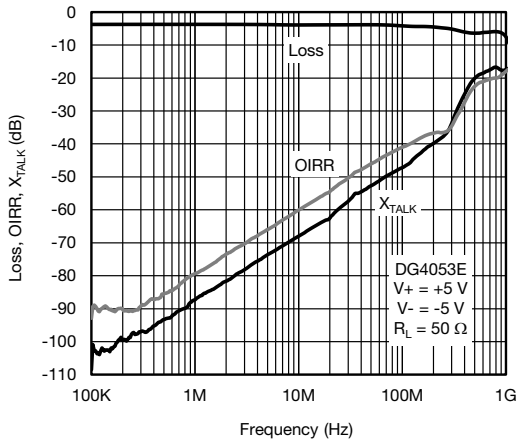


DG4051E Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

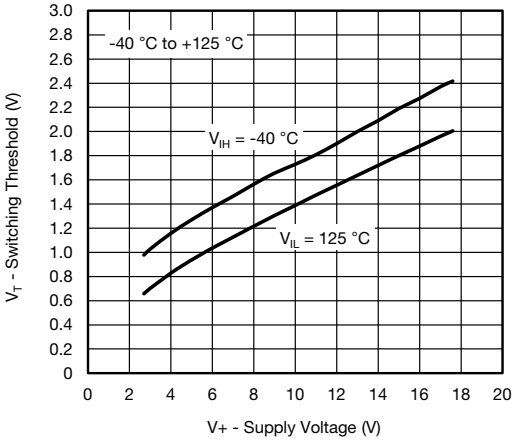


DG4052E Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

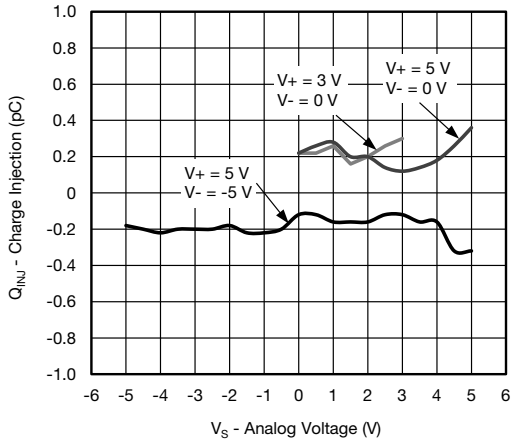
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



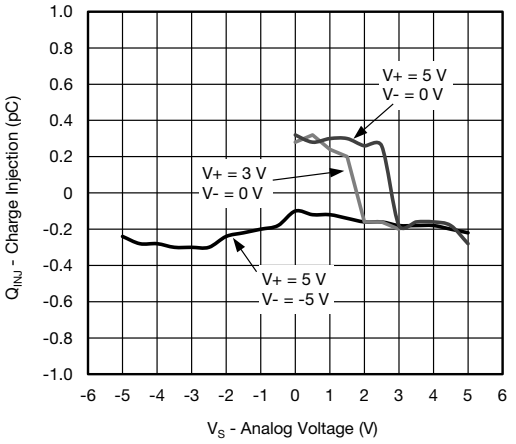
DG4053E Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



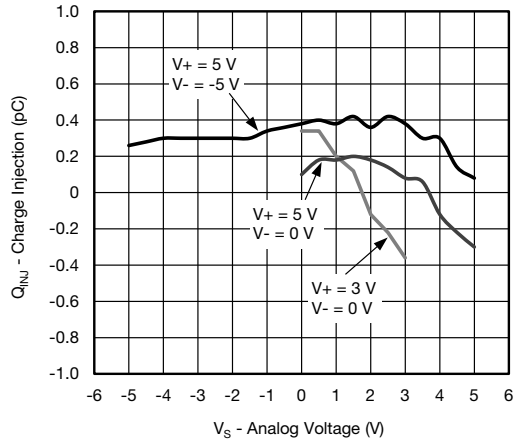
Switching Threshold vs. V+ Supply Voltage



DG4051E Charge Injection vs. Analog Voltage

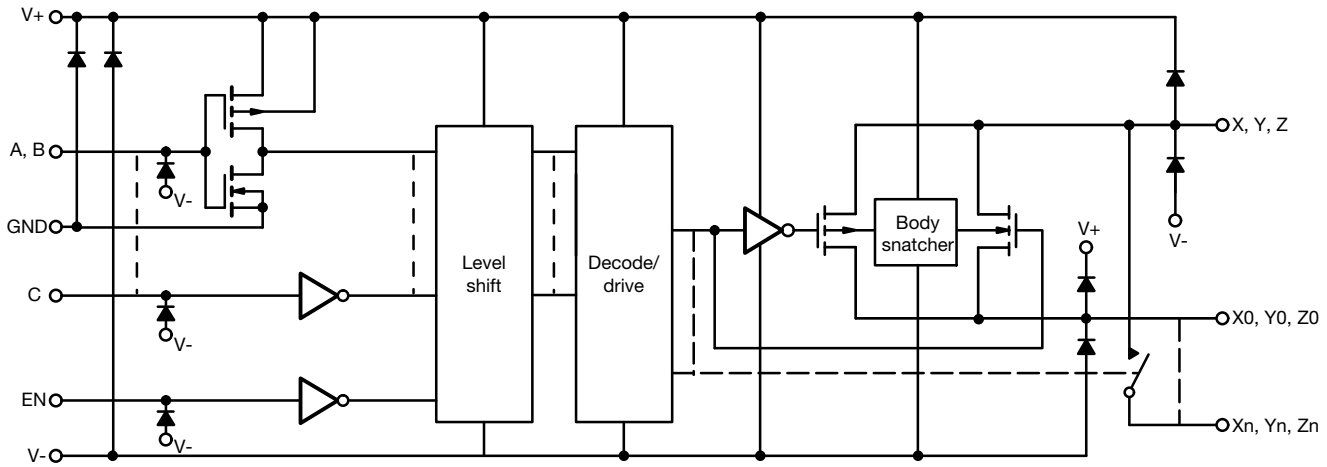


DG4053E Charge Injection vs. Analog Voltage

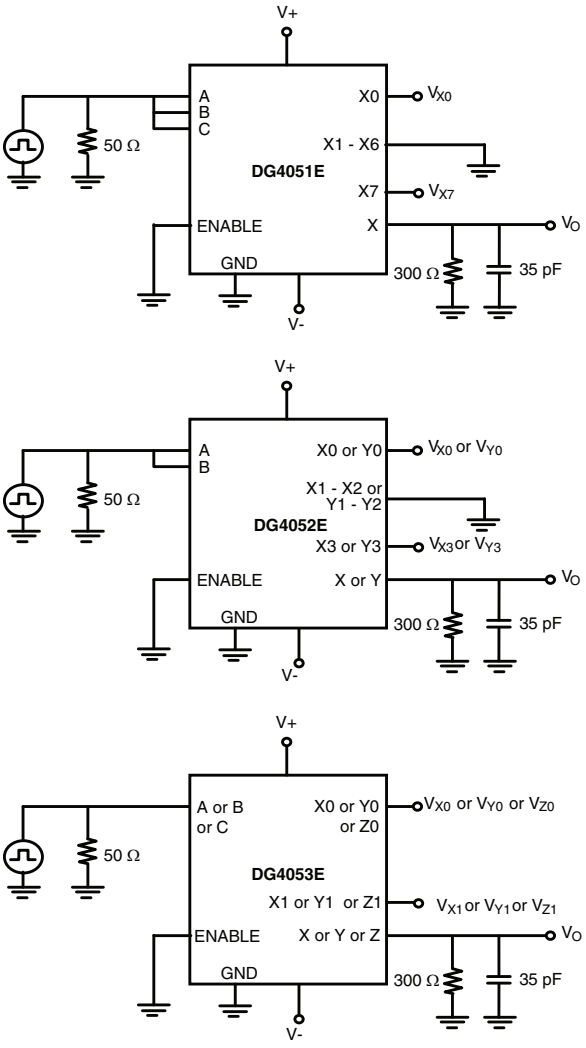


DG4052E Charge Injection vs. Analog Voltage

SCHEMATIC DIAGRAM (Typical Channel)



TEST CIRCUITS



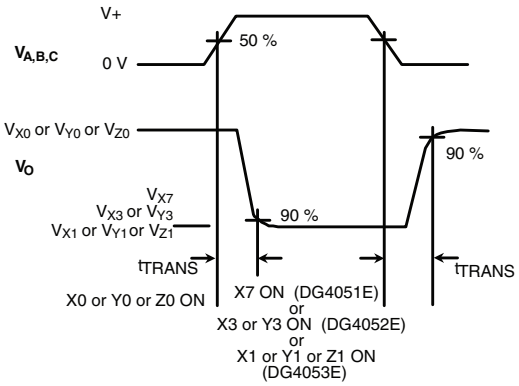


Fig. 1 - Transition Time

TEST CIRCUITS

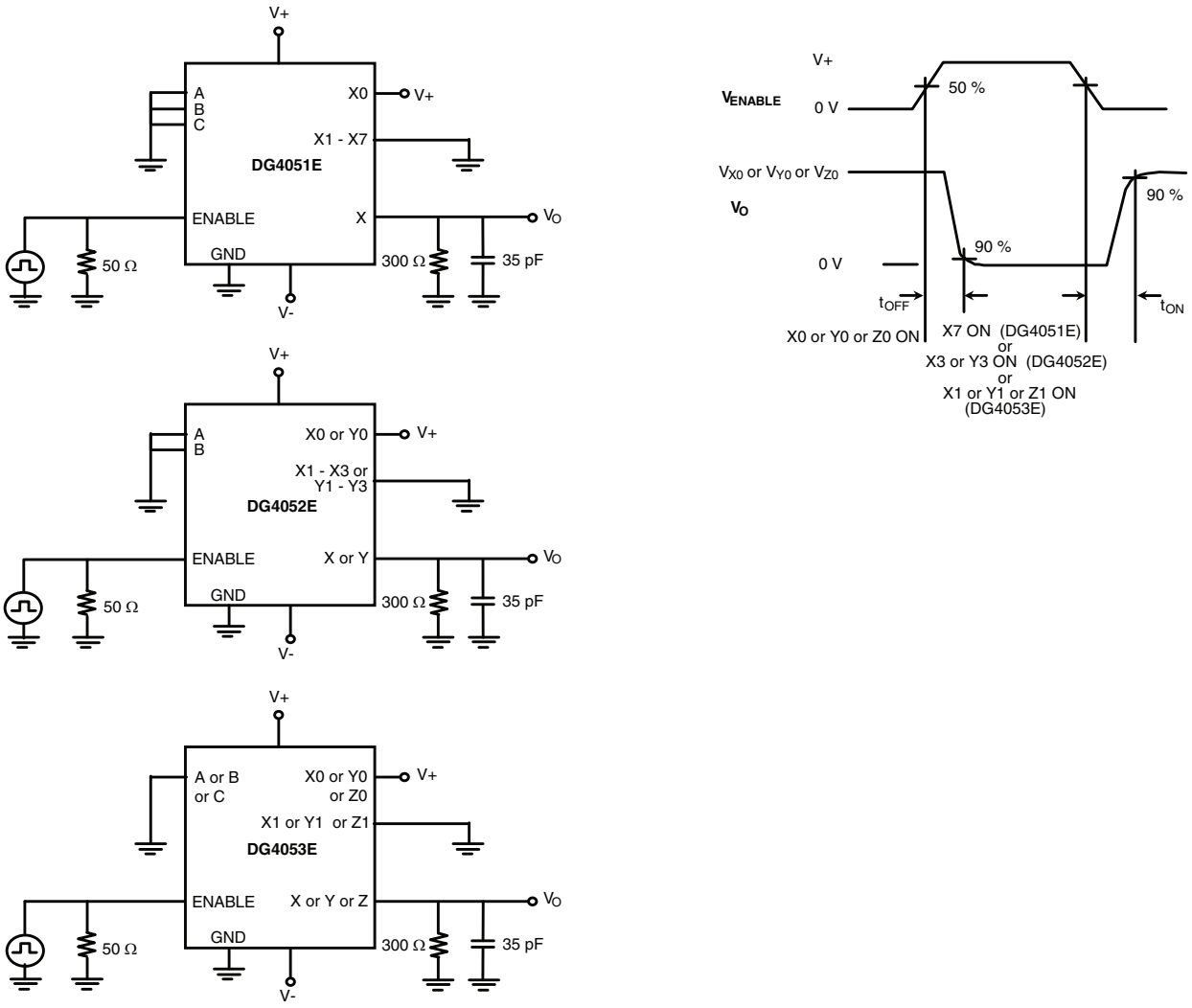
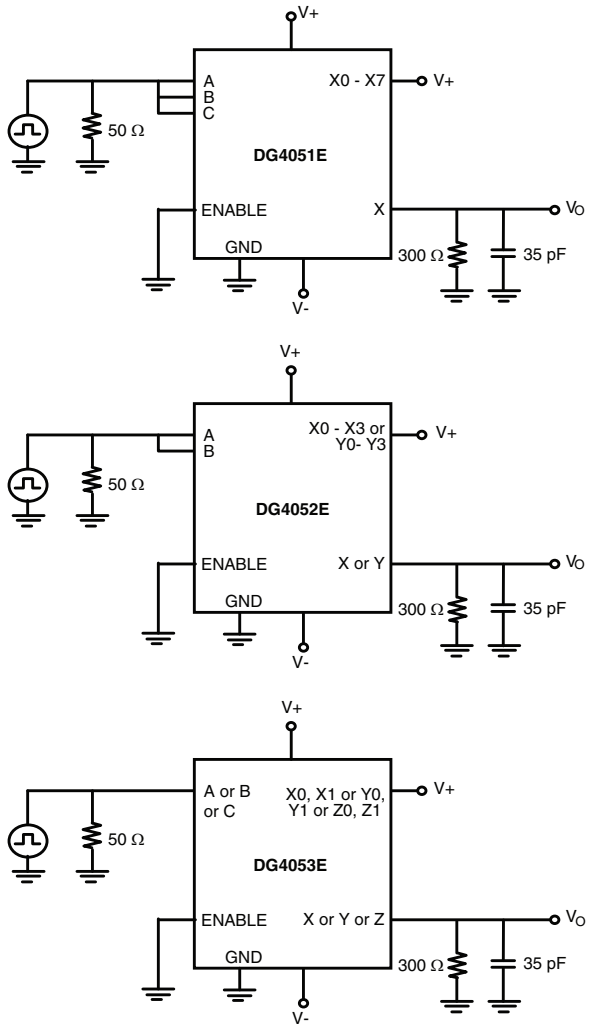


Fig. 2 - Enable Switching Time

TEST CIRCUITS



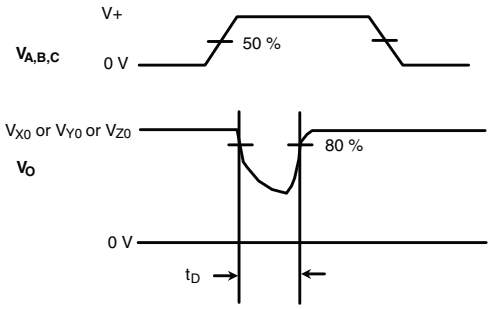
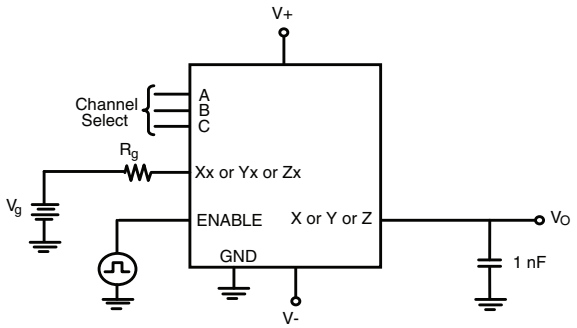


Fig. 3 - Break-Before-Make



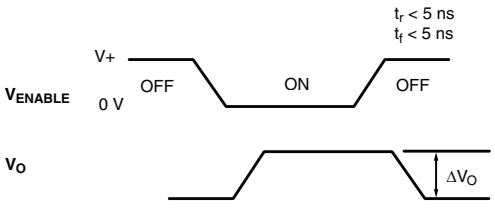


Fig. 4 - Charge Injection

TEST CIRCUITS

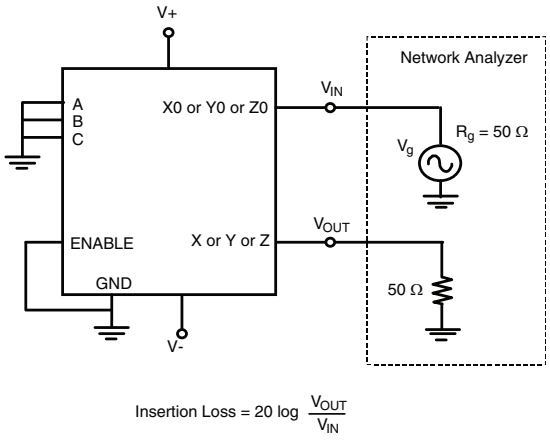


Fig. 5 - Insertion Loss

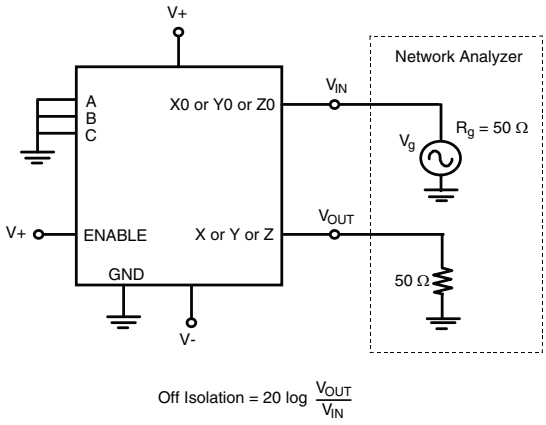


Fig. 7 - Off Isolation

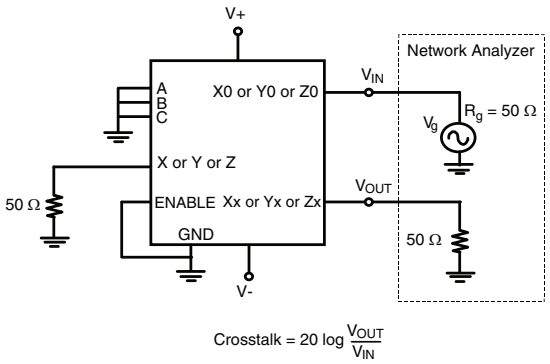


Fig. 6 - Crosstalk

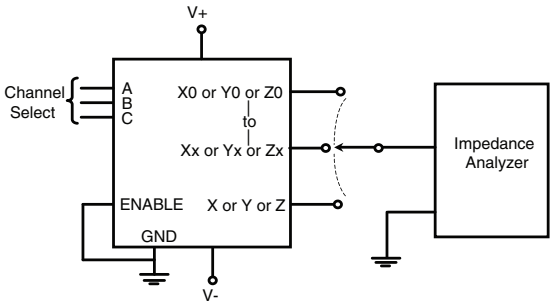


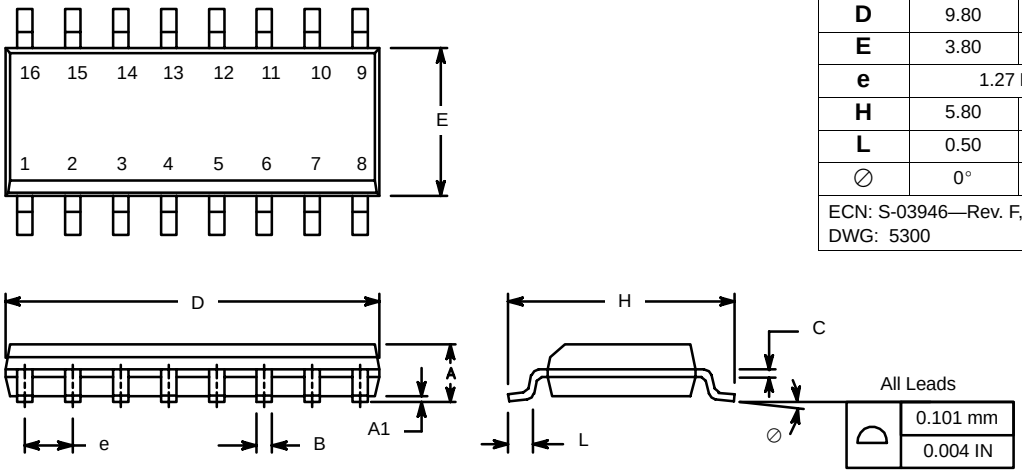
Fig. 8 - Source, Drain Capacitance

SOIC (NARROW): 16-LEAD

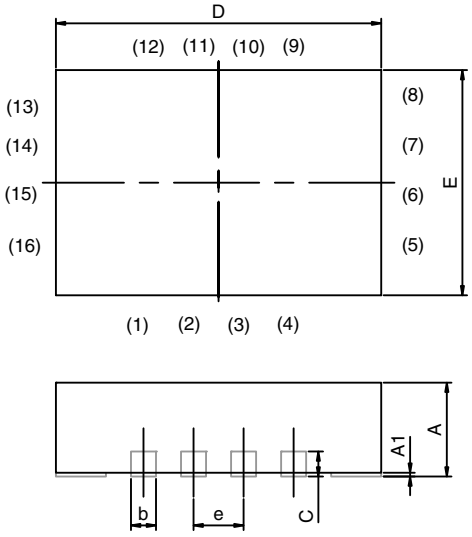
JEDEC Part Number: MS-012

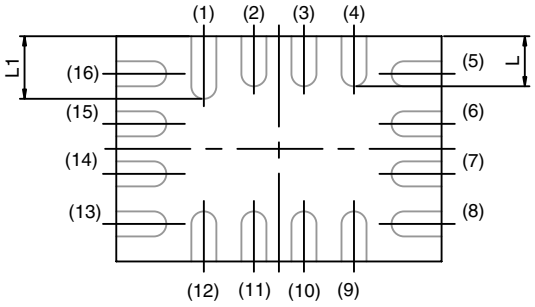
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



miniQFN-16L



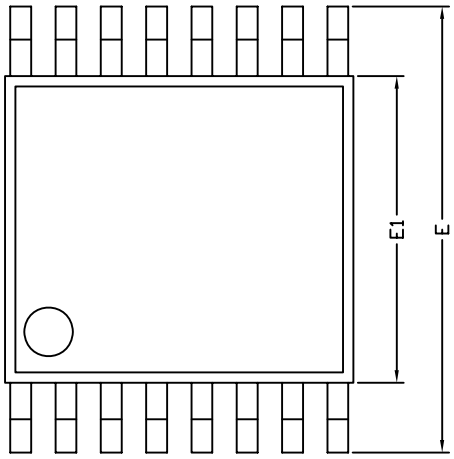


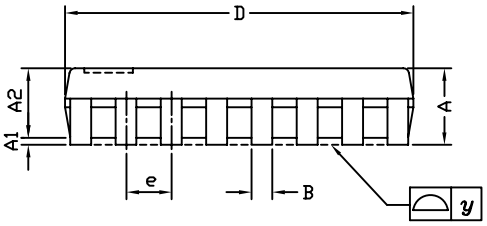
BACK SIDE VIEW

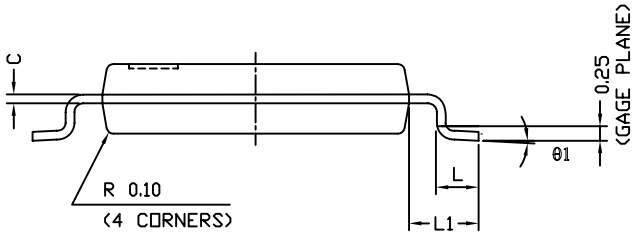
DIM	MILLIMETERS			INCHES		
	MIN.	NAM	MAX.	MIN.	NAM	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	-	0.05	0	-	0.002
b	0.15	0.20	0.25	0.0059	0.0078	0.0098
C	0.15	0.20	0.25	0.0059	0.0078	0.0098
D	2.50	2.60	2.70	0.0984	0.1023	0.1063
E	1.70	1.80	1.90	0.0669	0.0708	0.0748
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177
L1	0.45	0.50	0.55	0.0177	0.0196	0.0216

ECN T16-0234-Rev. B, 09-May-16
DWG: 5954

TSSOP: 16-LEAD

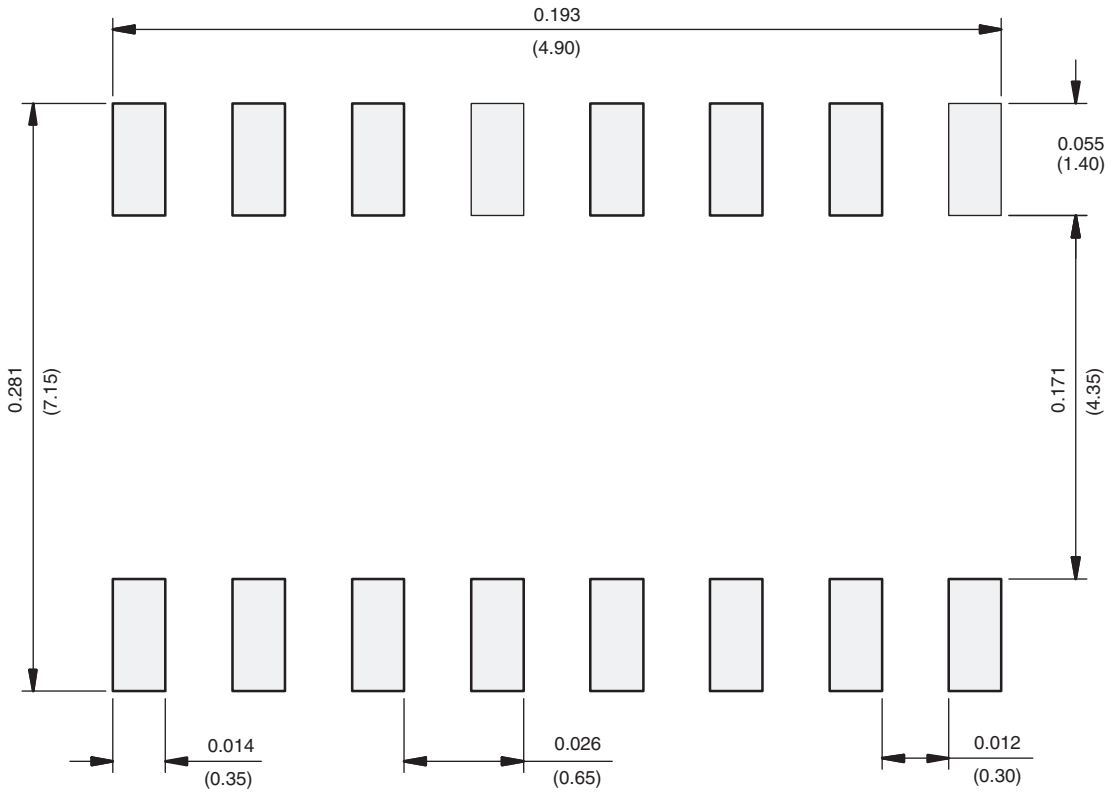






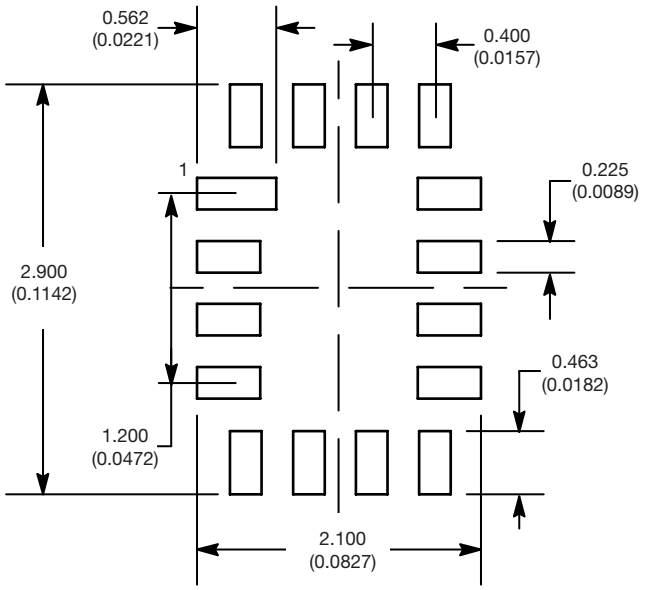
Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



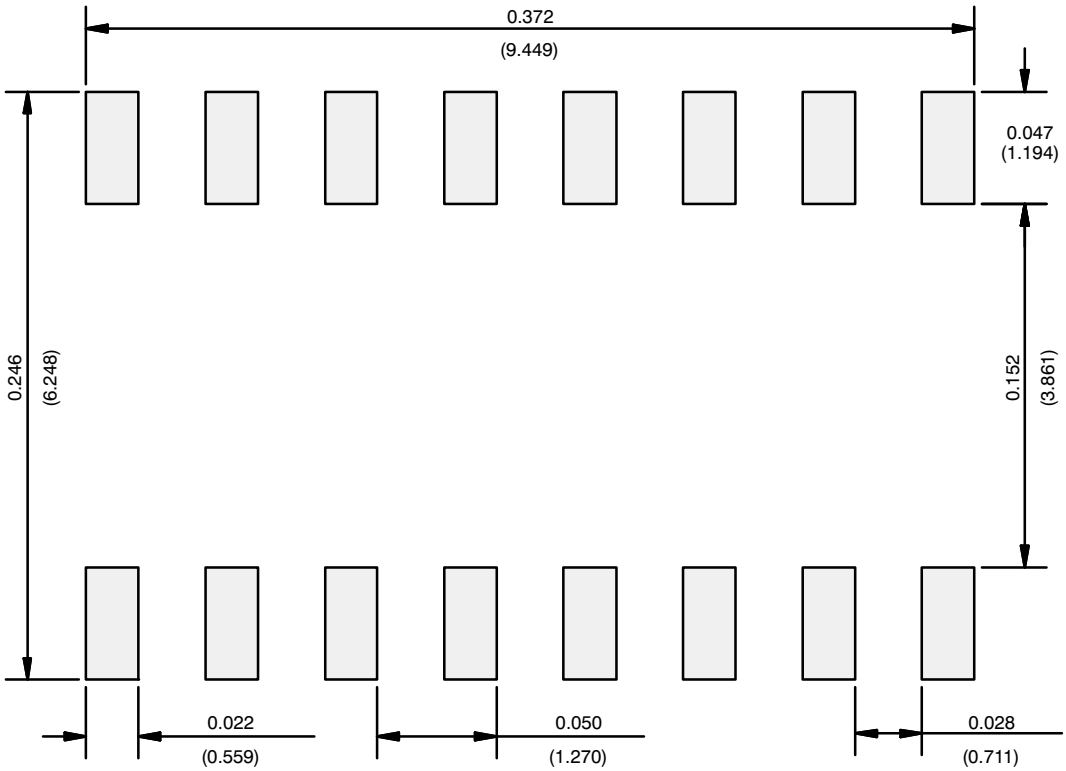
Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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