

Dual N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (Typ.)
Channel-1	30	0.0095 at V _{GS} = 10 V	30 ^a	5.6 nC
		0.0137 at V _{GS} = 4.5 V	22	
Channel-2	30	0.0051 at V _{GS} = 10 V	40 ^a	10.1 nC
		0.0070 at V _{GS} = 4.5 V	40 ^a	

FEATURES

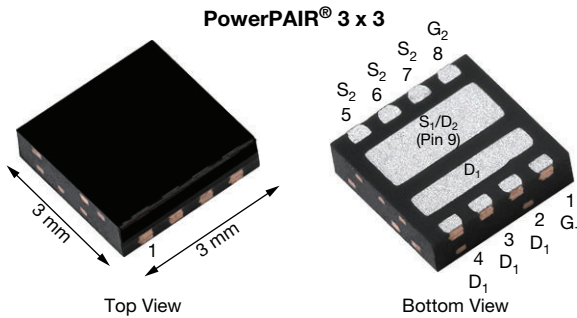
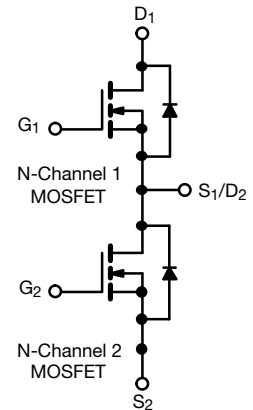
- PowerPAIR® Optimizes high-side and low-side MOSFETs for synchronous buck converters
- TrenchFET® power Mosfets
- 100 % R_g and UIS tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck
 - Battery charging
 - Computer system power
 - Graphic cards
- POL



Ordering Information:

SiZ340DT-T1-GE3 (lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V _{DS}	30		V	
Gate-Source Voltage	V _{GS}	+20, -16			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	30 ^a	40 ^a	A
		T _C = 70 °C	26.5	40 ^a	
		T _A = 25 °C	15.6 ^{b,c}	22.6 ^{b,c}	
		T _A = 70 °C	12.4 ^{b,c}	18.1 ^{b,c}	
Pulsed Drain Current (t = 100 μs)	I _{DM}	100	150		
Continuous Source Drain Diode Current	I _S	T _C = 25 °C	13.9	26	
		T _A = 25 °C	3.1 ^{b,c}	3.5 ^{b,c}	
Avalanche Current	I _{AS}	10	15		
Single Pulse Avalanche Energy	E _{AS}	5	11	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	16.7	31	W
		T _C = 70 °C	10.7	20	
		T _A = 25 °C	3.7 ^{b,c}	4.2 ^{b,c}	
		T _A = 70 °C	2.4 ^{b,c}	2.7 ^{b,c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d,e}		260			

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.



THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{a,b}	$t \leq 10$ s	R_{thJA}	27	34	24	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6	7.5	3.2	4	

Notes

- a. Surface mounted on 1" x 1" FR4 board.
- b. Maximum under steady state conditions is 69 °C/W for channel-1 and 64 °C/W for channel-2.

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)								
Parameter	Symbol	TEST CONDITIONS	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	Ch-1	30	-	-	V	
			Ch-2	30	-	-		
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A	Ch-1	-	18.4	-	mV/°C	
			Ch-2	-	30	-		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250$ μ A	Ch-1	-	-4.3	-	mV/°C	
			Ch-2	-	-5	-		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	Ch-1	1	-	2.4	V	
			Ch-2	1	-	2.4		
Gate Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = +20$ V, -16 V	Ch-1	-	-	± 100	nA	
			Ch-2	-	-	± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	Ch-1	-	-	1	μ A	
			Ch-2	-	-	1		
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	Ch-1	-	-	5		
			Ch-2	-	-	5		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	Ch-1	10	-	-	A	
			Ch-2	10	-	-		
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 15.6$ A	Ch-1	-	0.0079	0.0095	Ω	
			Ch-2	-	0.0042	0.0051		
			$V_{GS} = 4.5$ V, $I_D = 13$ A	Ch-1	-	0.0110		0.0137
				Ch-2	-	0.0058		0.0070
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15$ V, $I_D = 15.6$ A	Ch-1	-	37	-	S	
			Ch-2	-	60	-		
Dynamic^a								
Input Capacitance	C_{iss}	Channel-1 $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	Ch-1	-	760	-	pF	
			Ch-2	-	1552	-		
Output Capacitance	C_{oss}	Channel-2 $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	Ch-1	-	250	-	pF	
			Ch-2	-	450	-		
Reverse Transfer Capacitance	C_{rss}	Channel-2 $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	Ch-1	-	32	-	pF	
			Ch-2	-	40	-		
C_{rss} / C_{iss} Ratio			Ch-1	0.042	-	0.084	-	
			Ch-2	0.025	-	0.050		
Total Gate Charge	Q_g	$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 15.6$ A	Ch-1	-	12.3	19	nC	
			Ch-2	-	22.6	35		
		$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 20$ A	Ch-1	-	5.6	9		
			Ch-2	-	10.1	16		
Gate-Source Charge	Q_{gs}	Channel-1 $V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 15.6$ A	Ch-1	-	2.3	-	nC	
			Ch-2	-	4.2	-		
Gate-Drain Charge	Q_{gd}	Channel-2 $V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A	Ch-1	-	1	-	nC	
			Ch-2	-	1.8	-		
Output Charge	Q_{oss}		Ch-1	-	6.6	-	nC	
			Ch-2	-	12.4	-		
Gate Resistance	R_g	$f = 1$ MHz	Ch-1	0.3	1.7	3.4	Ω	
			Ch-2	0.3	1.3	2.6		



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	TEST CONDITIONS	Min.	Typ.	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	13	20	ns
Rise Time	t _r		Ch-2	-	22	33	
Turn-Off Delay Time	t _{d(off)}	Chan nel-2 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	55	85	
			Ch-2	-	82	123	
Fall Time	t _f		Ch-1	-	16	25	
			Ch-2	-	20	30	
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	7	14	
			Ch-2	-	7	14	
Rise Time	t _r		Ch-1	-	8	16	
			Ch-2	-	10	20	
Turn-Off Delay Time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	11	20	
			Ch-2	-	12	20	
Fall Time	t _f		Ch-1	-	12	20	
			Ch-2	-	16	30	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1	-	-	13.9	A
			Ch-2	-	-	25.8	
Pulse Diode Forward Current (t = 100 μs)	I _{SM}		Ch-1	-	-	100	
			Ch-2	-	-	150	
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	Ch-1	-	0.8	1.2	V
			Ch-2	-	0.82	1.2	
Body Diode Reverse Recovery Time	t _{rr}		Ch-1	-	20	35	ns
			Ch-2	-	26	40	
Body Diode Reverse Recovery Charge	Q _{rr}	Channel-1 I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	9	20	nC
			Ch-2	-	20	30	
Reverse Recovery Fall Time	t _a	Channel-2 I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	11.5	-	ns
			Ch-2	-	18.1	-	
Reverse Recovery Rise Time	t _b		Ch-1	-	8.5	-	
			Ch-2	-	7.9	-	

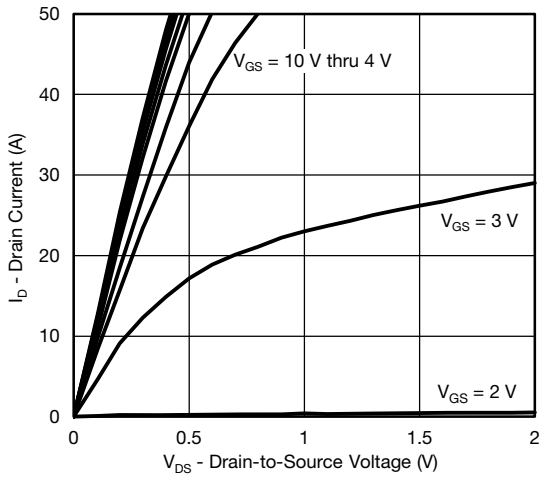
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

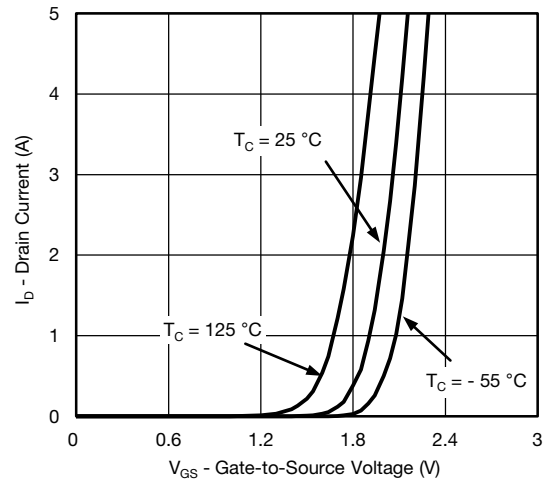
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



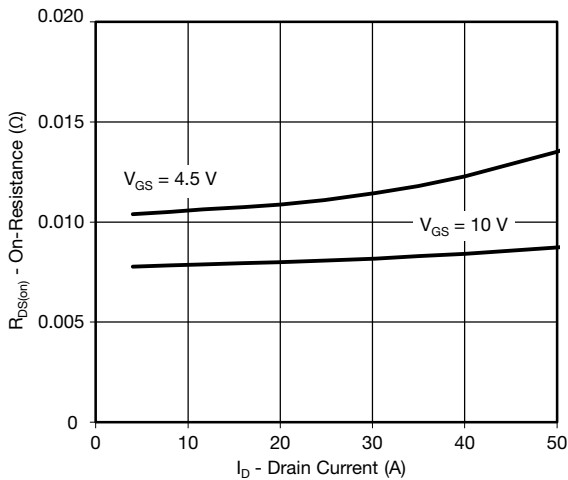
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



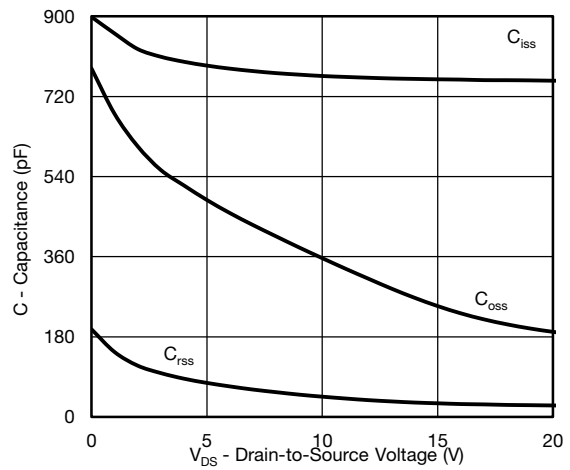
Output Characteristics



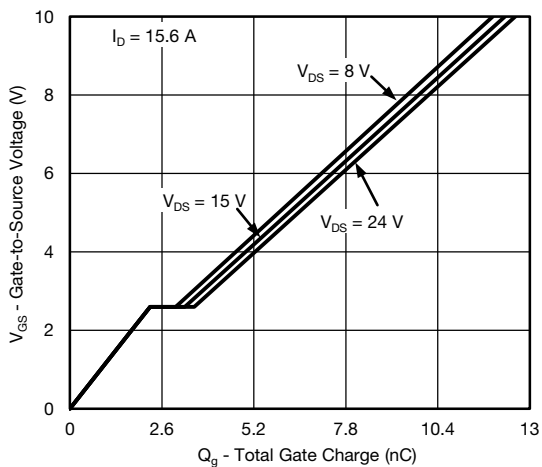
Transfer Characteristics



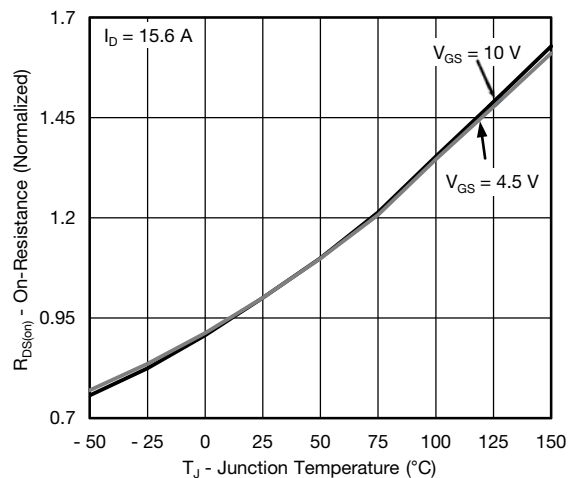
On-Resistance vs. Drain Current



Capacitance



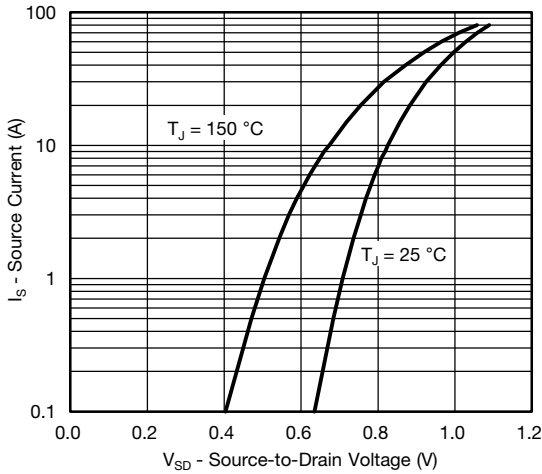
Gate Charge



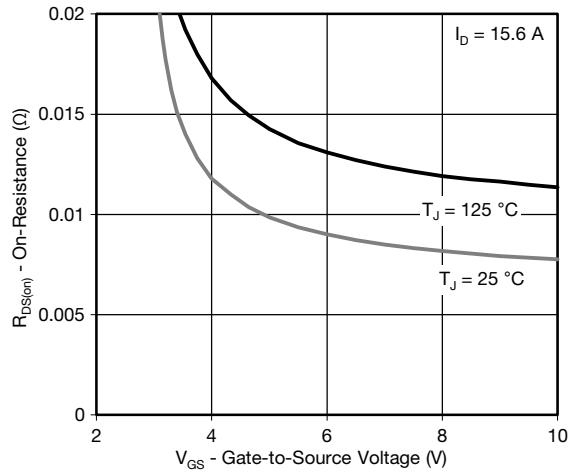
On-Resistance vs. Junction Temperature



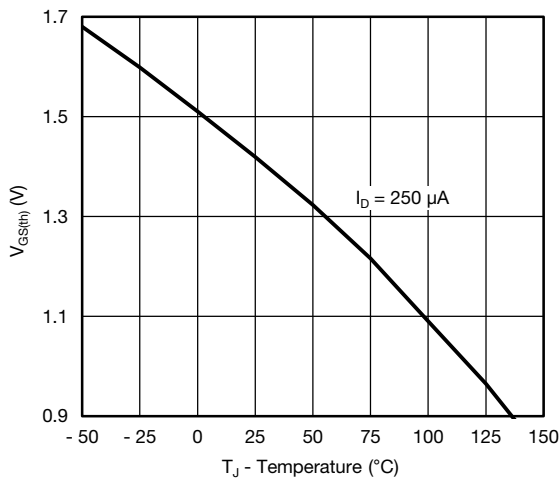
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



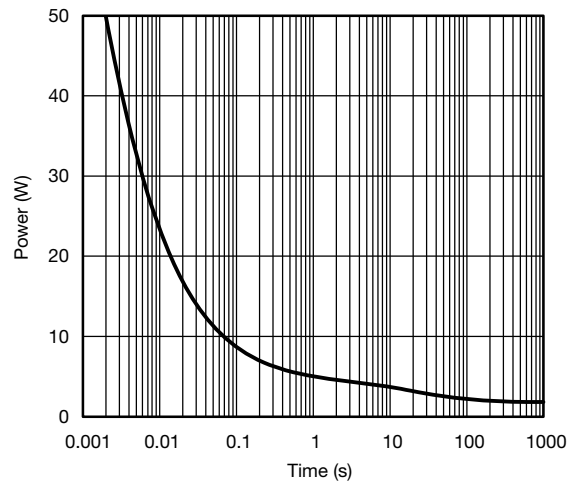
Source-Drain Diode Forward Voltage



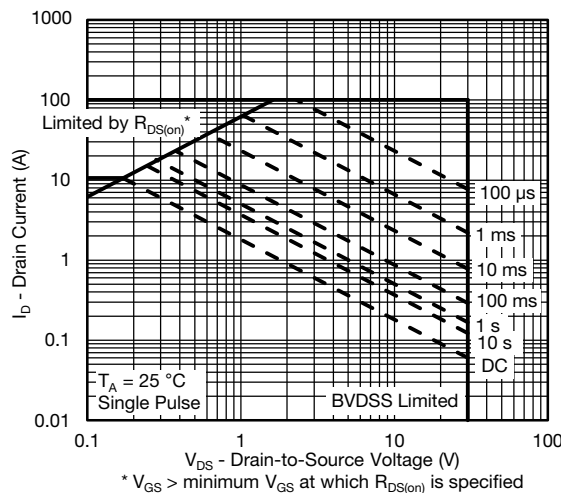
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



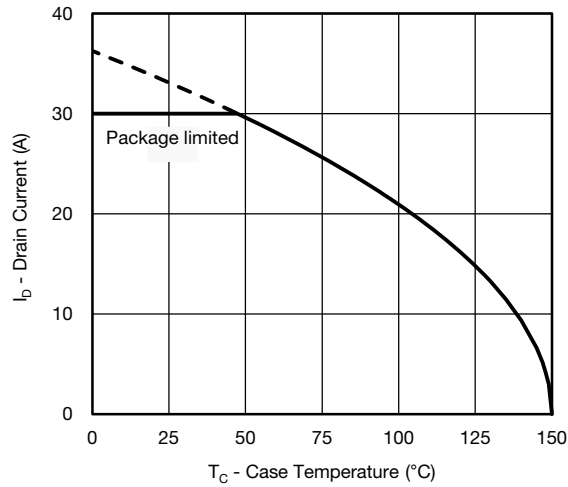
Single Pulse Power



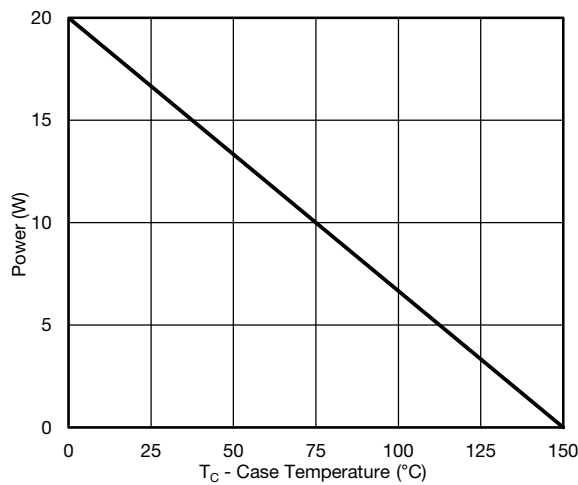
Safe Operating Area, Junction-to-Ambient



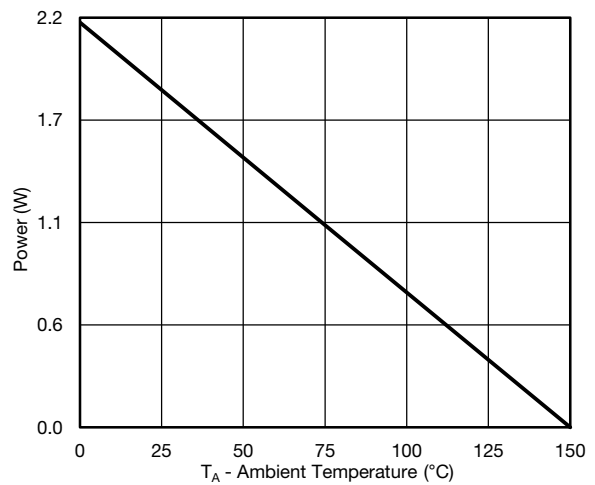
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Case

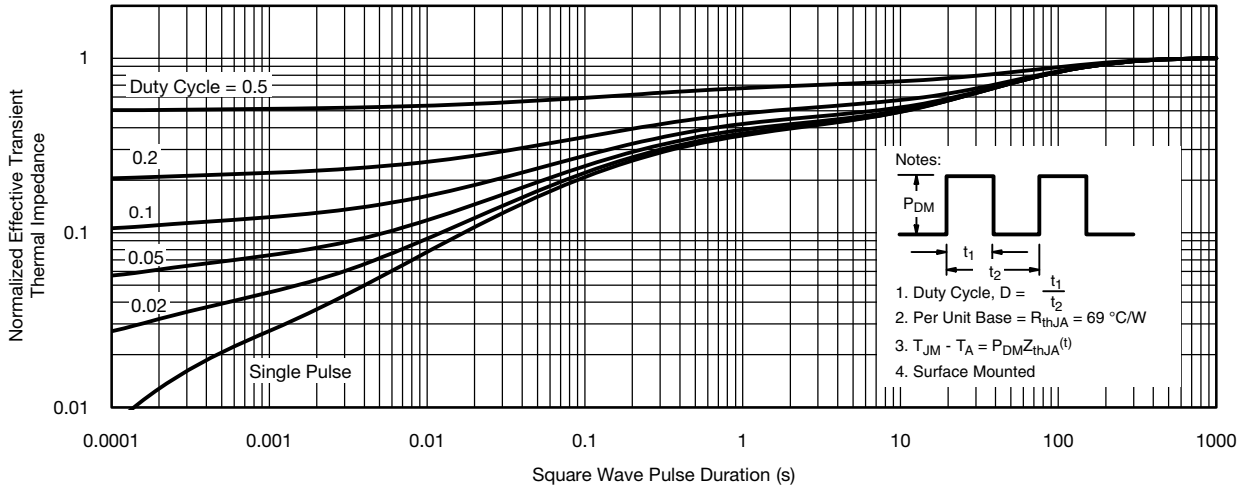


Power, Junction-to-Ambient

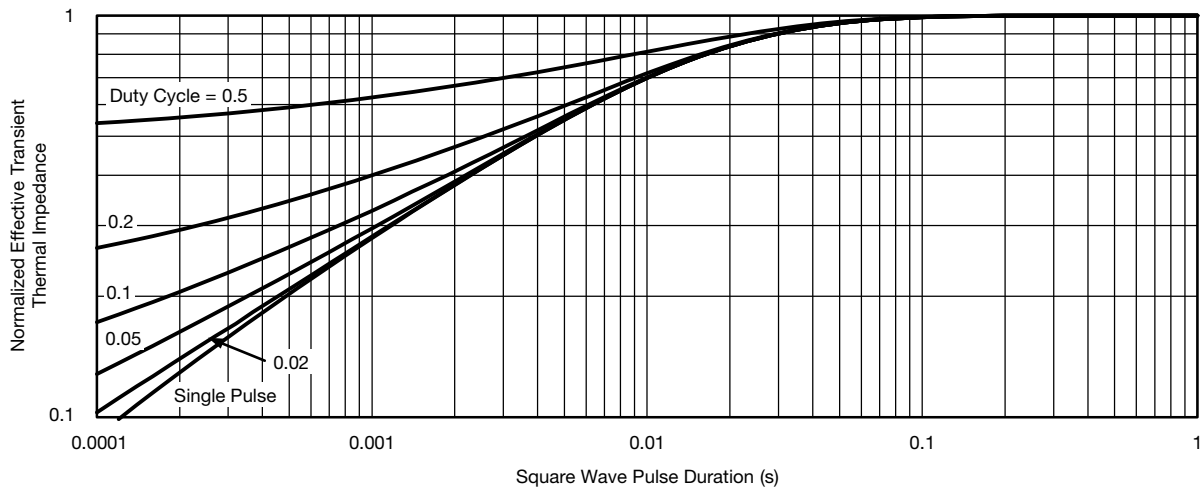
* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



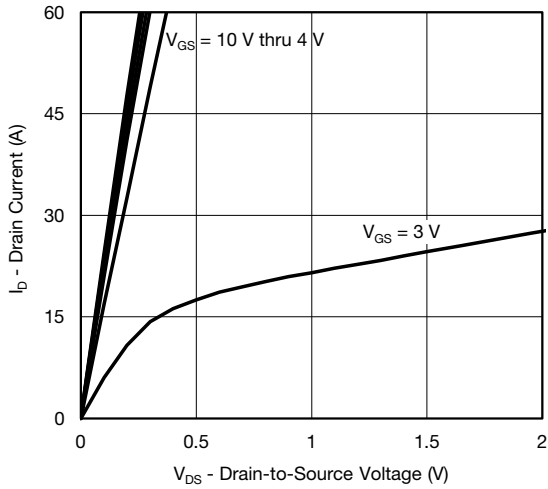
Normalized Thermal Transient Impedance, Junction-to-Ambient



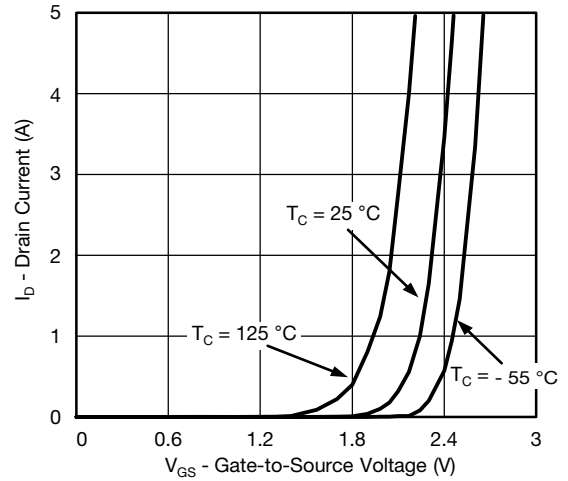
Normalized Thermal Transient Impedance, Junction-to-Case



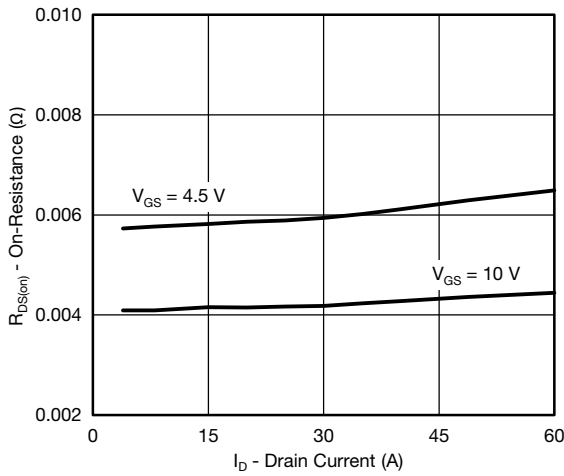
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



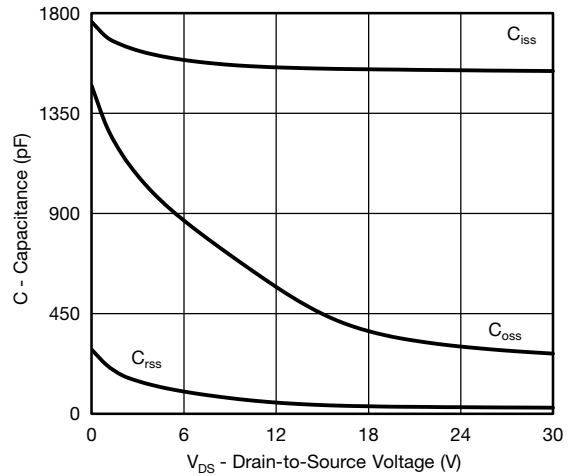
Output Characteristics



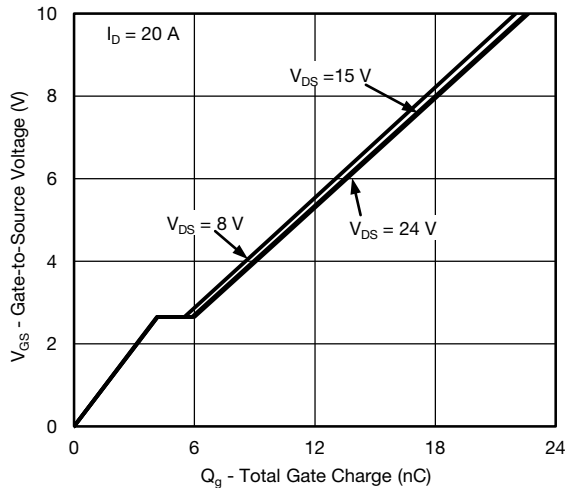
Transfer Characteristics



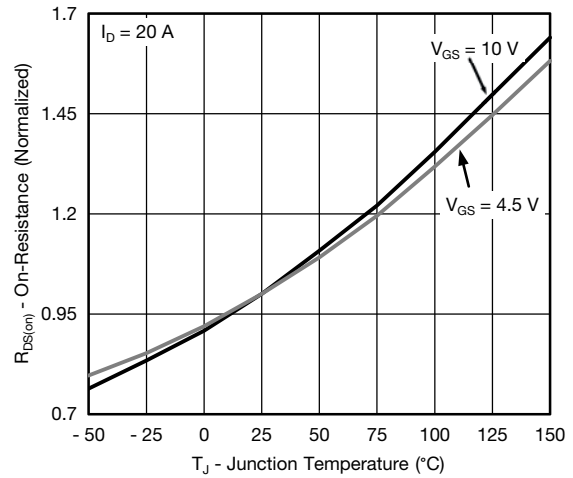
On-Resistance vs. Drain Current



Capacitance

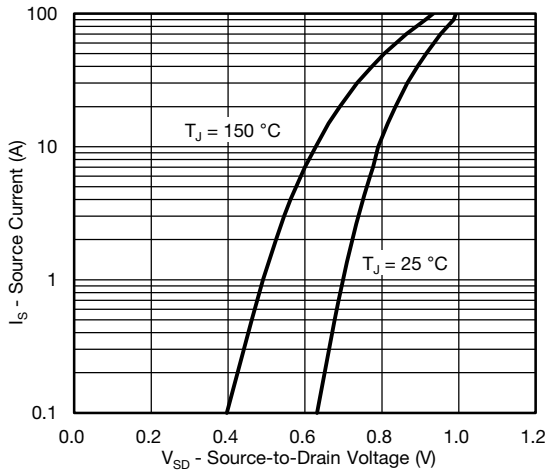


Gate Charge

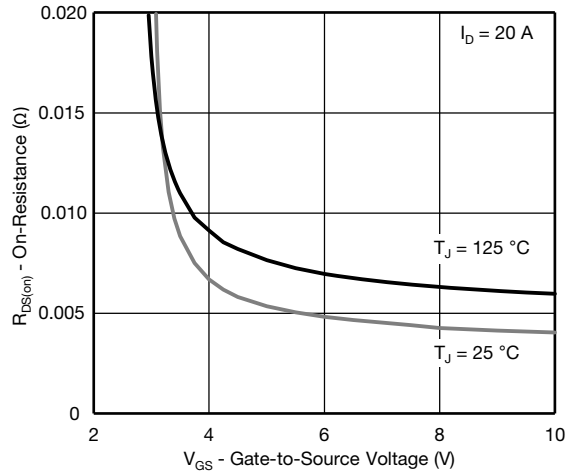


On-Resistance vs. Junction Temperature

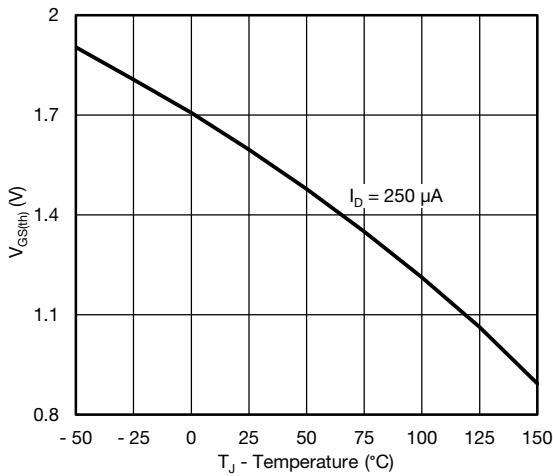
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



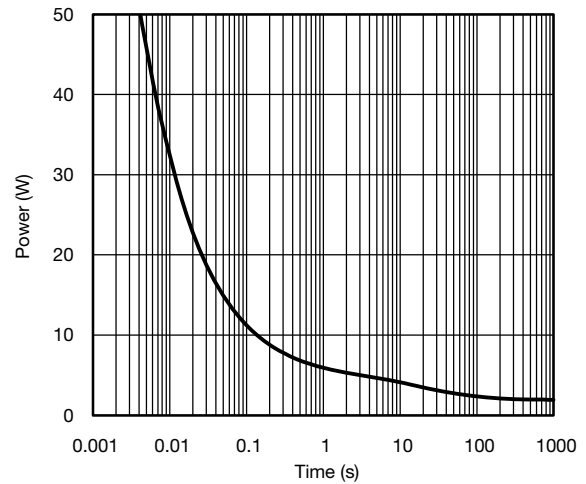
Source-Drain Diode Forward Voltage



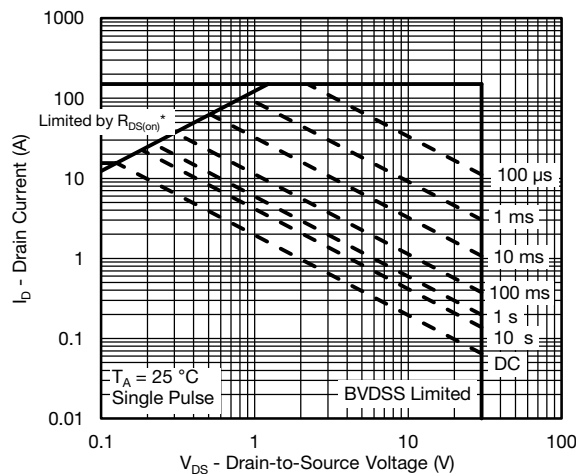
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



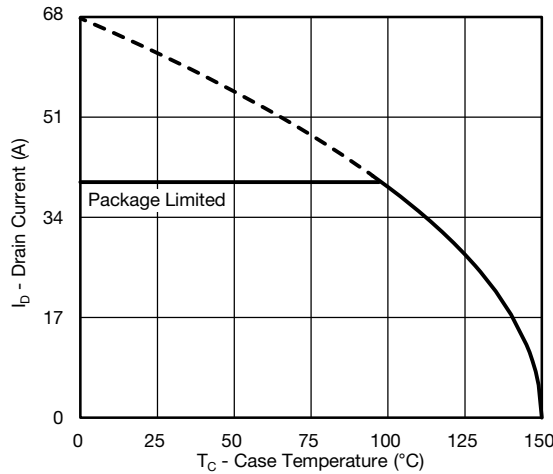
Single Pulse Power



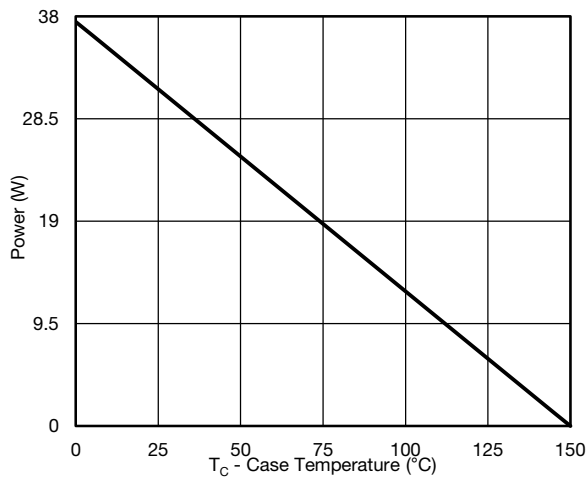
Safe Operating Area, Junction-to-Ambient



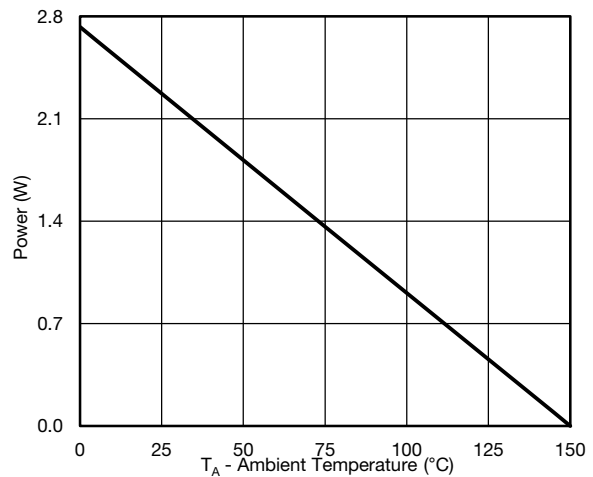
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Case

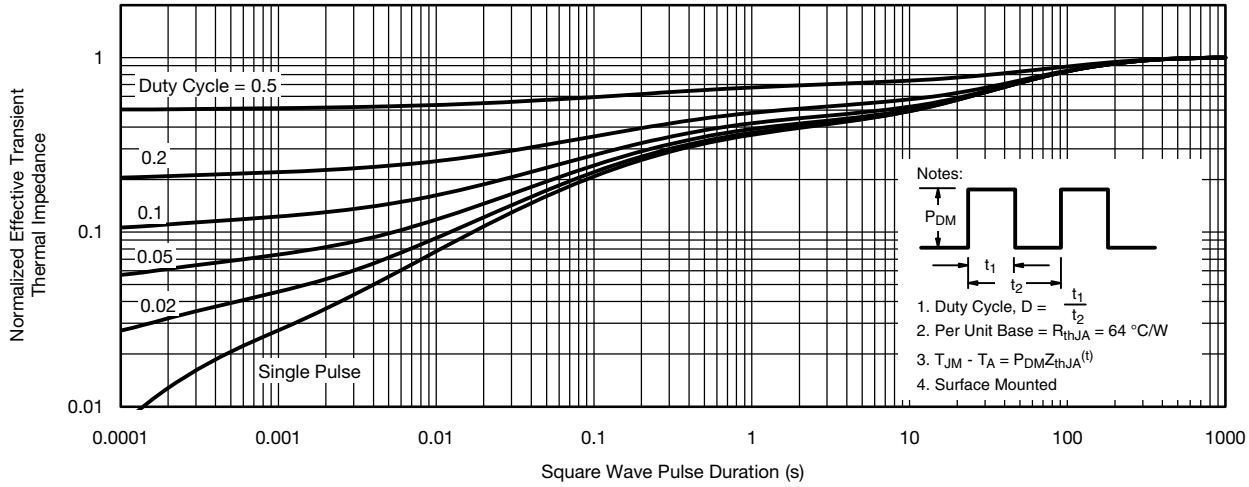


Power, Junction-to-Ambient

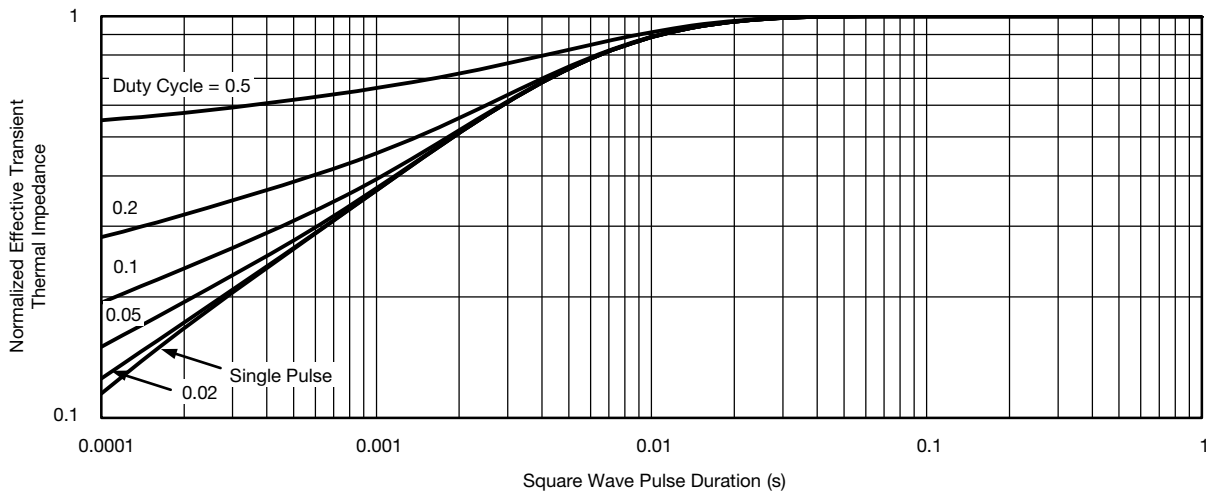
* The power dissipation P_D is based on T_{J(max.)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62877.



PowerPAIR® 3 x 3 Case Outline



Note
* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



Disclaimer

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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.