



## N- and P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
N-Channel	12	0.034 at V <sub>GS</sub> = 4.5 V	4.5 <sup>a</sup>	5.6 nC
		0.040 at V <sub>GS</sub> = 2.5 V	4.5 <sup>a</sup>	
		0.050 at V <sub>GS</sub> = 1.8 V	4.5 <sup>a</sup>	
		0.070 at V <sub>GS</sub> = 1.5 V	4.5 <sup>a</sup>	
P-Channel	- 12	0.059 at V <sub>GS</sub> = - 4.5 V	- 4.5 <sup>a</sup>	7.8 nC
		0.081 at V <sub>GS</sub> = - 2.5 V	- 4.5 <sup>a</sup>	
		0.115 at V <sub>GS</sub> = - 1.8 V	- 4.5 <sup>a</sup>	
		0.215 at V <sub>GS</sub> = - 1.5 V	- 1.5	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Typical ESD Protection: N-Channel 1500 V  
P-Channel 1000 V
- 100 % R<sub>G</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

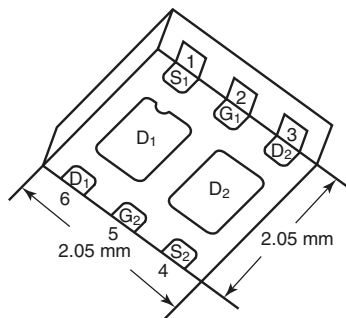


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

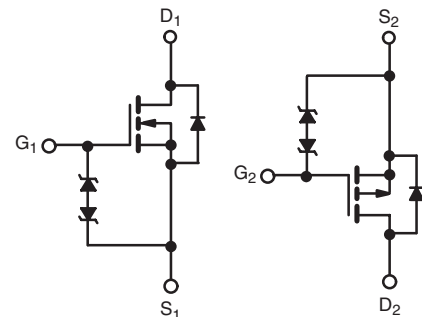
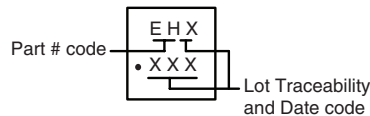
### APPLICATIONS

- Load Switch for Portable Devices
- DC/DC Converters

PowerPAK® SC-70-6 Dual



Marking Code



N-Channel MOSFET

P-Channel MOSFET

Ordering Information: SiA533EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V <sub>DS</sub>	12	- 12	V	
Gate-Source Voltage	V <sub>GS</sub>	± 8			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	4.5 <sup>a</sup>	- 4.5 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	4.5 <sup>a</sup>	- 4.5 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	4.5 <sup>a, b, c</sup>	- 4.5 <sup>a, b, c</sup>	
		T <sub>A</sub> = 70 °C	4.5 <sup>a, b, c</sup>	- 3.7 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	20	- 15		
Source Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	4.5 <sup>a</sup>	- 4.5 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	1.6 <sup>b, c</sup>	- 1.6 <sup>b, c</sup>	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	7.8	7.8	W
		T <sub>C</sub> = 70 °C	5	5	
		T <sub>A</sub> = 25 °C	1.9 <sup>b, c</sup>	1.9 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	1.2 <sup>b, c</sup>	1.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260			



THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient <sup>b, f</sup>	$t \leq 5 \text{ s}$	$R_{thJA}$	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	12.5	16	12.5	16	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c.  $t = 5 \text{ s}$ .d. See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 110 °C/W.

SPECIFICATIONS $T_J = 25 \text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \text{ } \mu\text{A}$	N-Ch	12			V
		$V_{GS} = 0 \text{ V}, I_D = -250 \text{ } \mu\text{A}$	P-Ch	-12			
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \text{ } \mu\text{A}$	N-Ch		19		mV/°C
		$I_D = -250 \text{ } \mu\text{A}$	P-Ch		-5.7		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \text{ } \mu\text{A}$	N-Ch		-2.7		mV/°C
		$I_D = -250 \text{ } \mu\text{A}$	P-Ch		1.7		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \text{ } \mu\text{A}$	N-Ch	0.4		1.0	V
		$V_{DS} = V_{GS}, I_D = -250 \text{ } \mu\text{A}$	P-Ch	-0.4		-1.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	N-Ch			$\pm 0.5$	$\mu\text{A}$
			P-Ch			$\pm 0.5$	
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	N-Ch			$\pm 5$	
			P-Ch			$\pm 5$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch			1	$\mu\text{A}$
		$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch			-1	
		$V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	10			A
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	-10			
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 4.6 \text{ A}$	N-Ch		0.028	0.034	$\Omega$
		$V_{GS} = -4.5 \text{ V}, I_D = -3.6 \text{ A}$	P-Ch		0.048	0.059	
		$V_{GS} = 2.5 \text{ V}, I_D = 4.2 \text{ A}$	N-Ch		0.032	0.040	
		$V_{GS} = -2.5 \text{ V}, I_D = -3.1 \text{ A}$	P-Ch		0.066	0.081	
		$V_{GS} = 1.8 \text{ V}, I_D = 3.8 \text{ A}$	N-Ch		0.038	0.050	
		$V_{GS} = -1.8 \text{ V}, I_D = -2.6 \text{ A}$	P-Ch		0.093	0.115	
		$V_{GS} = 1.5 \text{ V}, I_D = 1.5 \text{ A}$	N-Ch		0.045	0.070	
		$V_{GS} = -1.5 \text{ V}, I_D = -0.5 \text{ A}$	P-Ch		0.120	0.215	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 6 \text{ V}, I_D = 4.6 \text{ A}$	N-Ch		21		S
		$V_{DS} = -6 \text{ V}, I_D = -3.6 \text{ A}$	P-Ch		11		
Input Capacitance	$C_{iss}$	N-Channel $V_{DS} = 6 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	N-Ch		420		pF
Output Capacitance	$C_{oss}$		P-Ch		545		
			N-Ch		100		
Reverse Transfer Capacitance	$C_{rss}$		P-Ch		192		
		N-Ch		62			
		P-Channel $V_{DS} = -6 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	N-Ch		62		
			P-Ch		175		



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 5.9\text{ A}$	N-Ch		10	15	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -4.7\text{ A}$	P-Ch		13	20	
		N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5.9\text{ A}$	N-Ch		5.6	8.5	
			P-Ch		7.8	12	
Gate-Source Charge	$Q_{gs}$	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.7\text{ A}$	N-Ch		0.7		
			P-Ch		1.3		
Gate-Drain Charge	$Q_{gd}$		N-Ch		0.85		
			P-Ch		2.3		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	N-Ch	0.7	3.5	7	$\Omega$
			P-Ch	1.4	7	14	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong 4.8\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		10	15	ns
			P-Ch		15	25	
Rise Time	$t_r$		N-Ch		10	15	
			P-Ch		15	25	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}, R_L = 1.6\text{ }\Omega$ $I_D \cong -3.7\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		20	30	
			P-Ch		25	40	
Fall Time	$t_f$		N-Ch		10	15	
			P-Ch		10	15	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong 4.8\text{ A}, V_{GEN} = 8\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		5	10	
			P-Ch		5	10	
Rise Time	$t_r$		N-Ch		10	15	
			P-Ch		10	15	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}, R_L = 1.6\text{ }\Omega$ $I_D \cong -3.7\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		20	30	
			P-Ch		25	40	
Fall Time	$t_f$		N-Ch		10	15	
			P-Ch		10	15	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			4.5	A
			P-Ch			-4.5	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		N-Ch			20	A
			P-Ch			-15	
Body Diode Voltage	$V_{SD}$	$I_S = 4.8\text{ A}, V_{GS} = 0\text{ V}$ $I_S = -3.7\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.85	1.2	V
			P-Ch		-0.87	-1.2	
Body Diode Reverse Recovery Time	$t_{rr}$	N-Channel $I_F = 4.4\text{ A}, dl/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		10	20	ns
			P-Ch		25	50	
Body Diode Reverse Recovery Charge	$Q_{rr}$		N-Ch		5	10	nC
			P-Ch		10	20	
Reverse Recovery Fall Time	$t_a$	P-Channel $I_F = -3.7\text{ A}, dl/dt = -100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		5.5		ns
			P-Ch		17		
Reverse Recovery Rise Time	$t_b$		N-Ch		4.5		
			P-Ch		8		

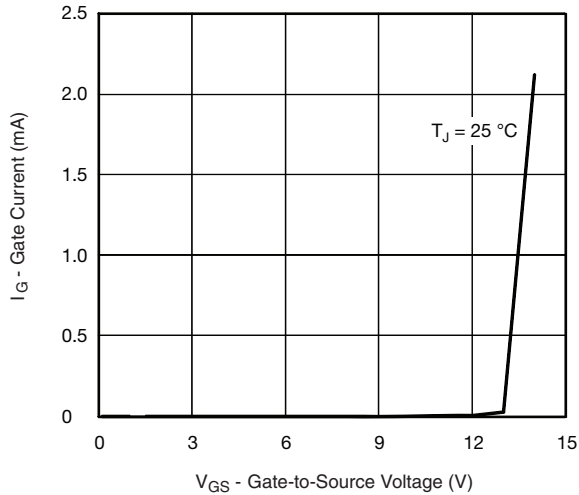
Notes:

a. Guaranteed by design, not subject to production testing.

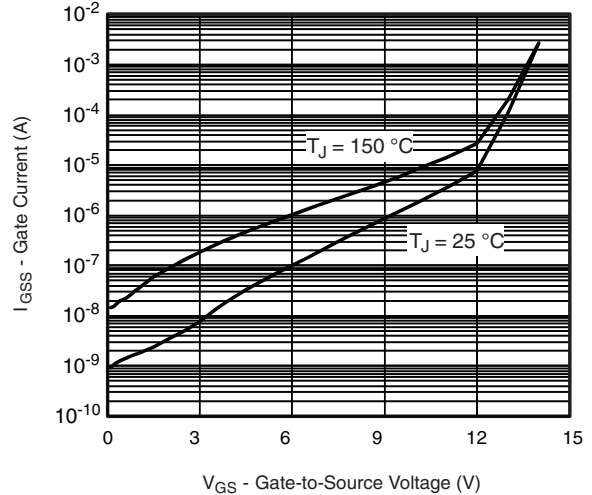
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

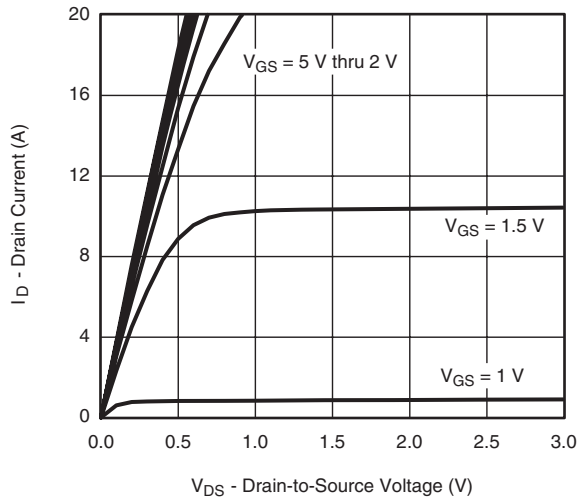
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



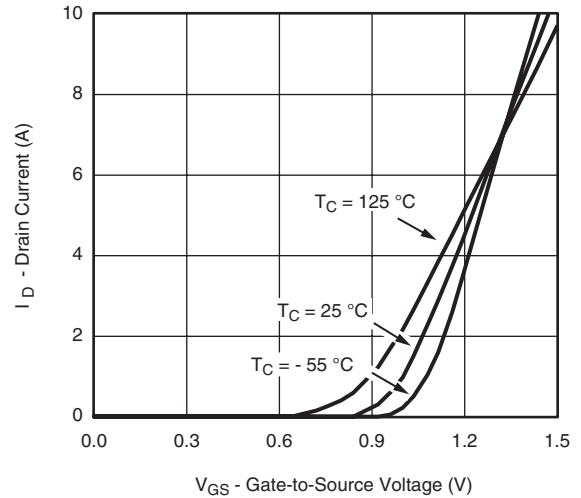
Gate Current vs. Gate-Source Voltage



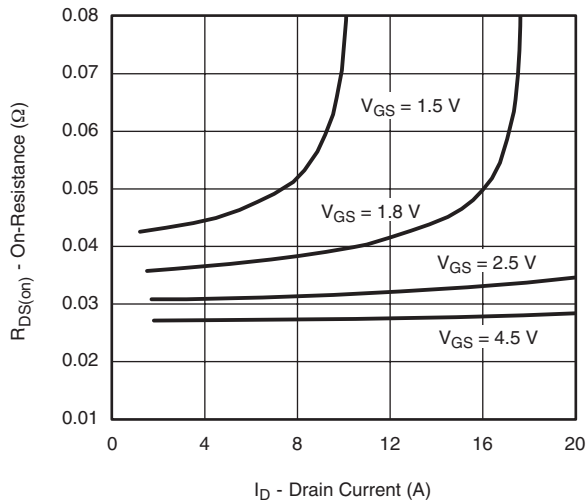
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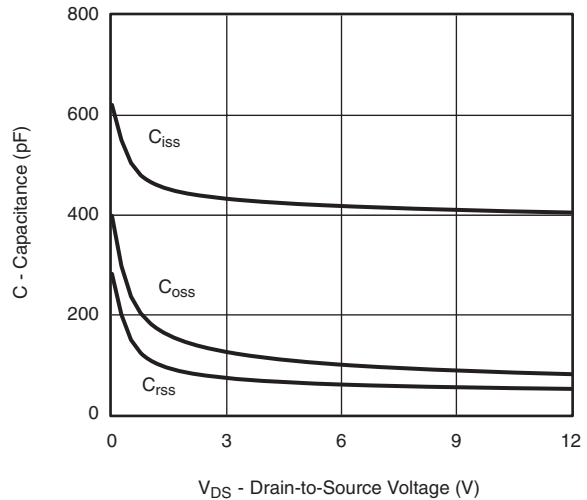
Output Characteristics



Transfer Characteristics



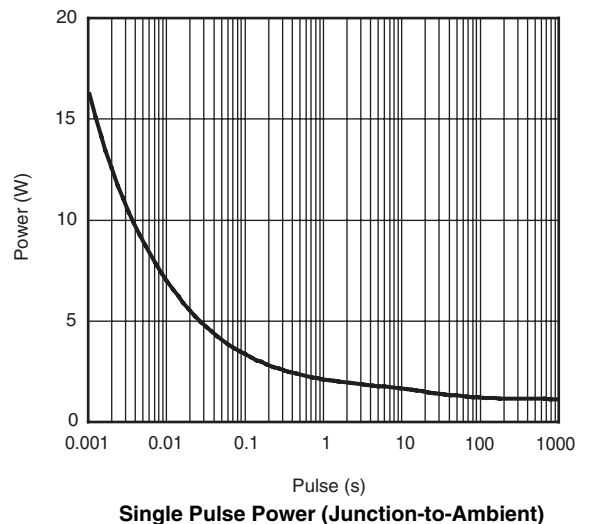
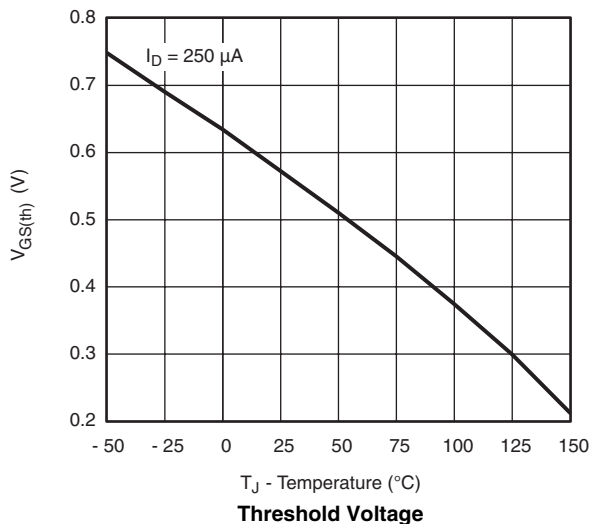
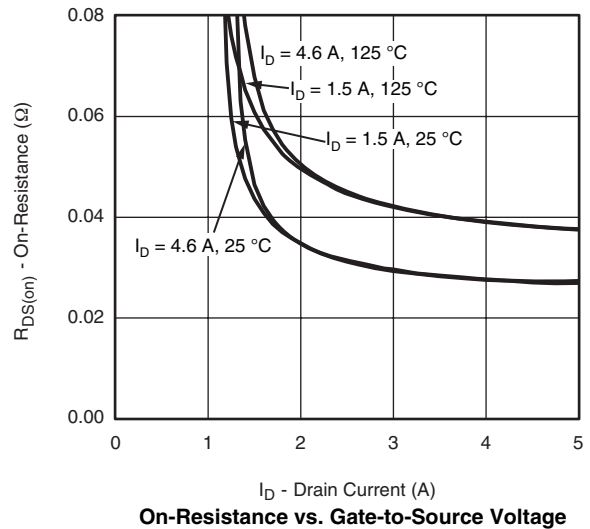
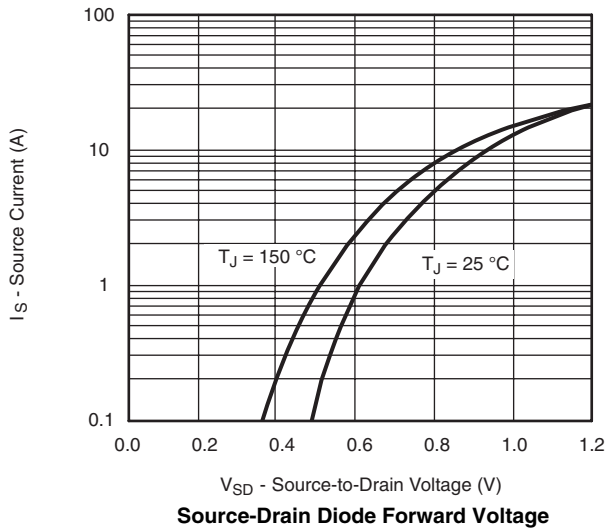
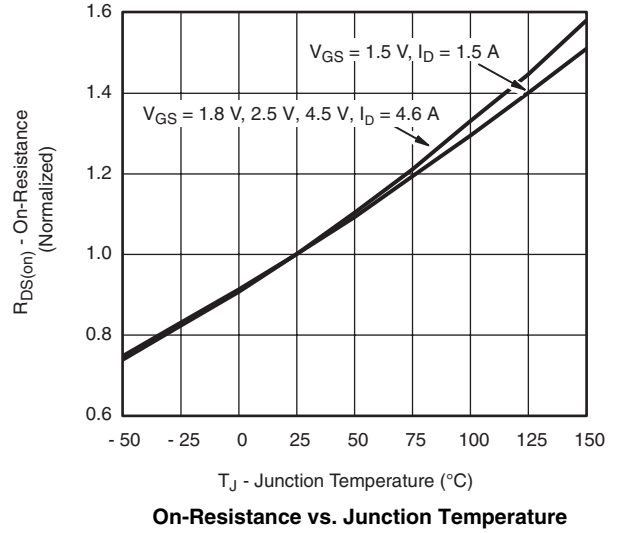
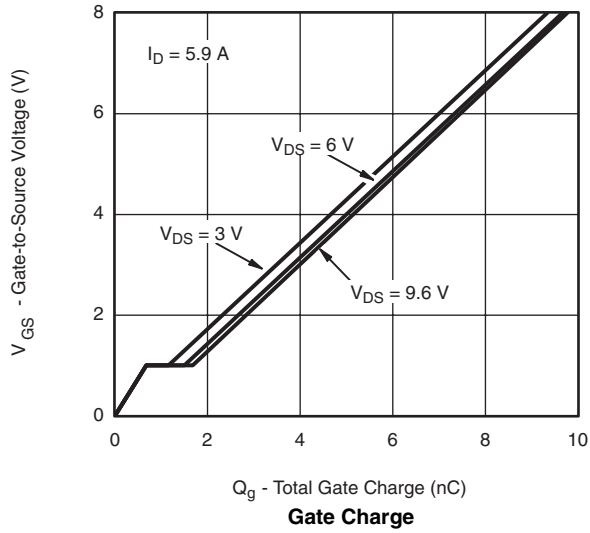
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

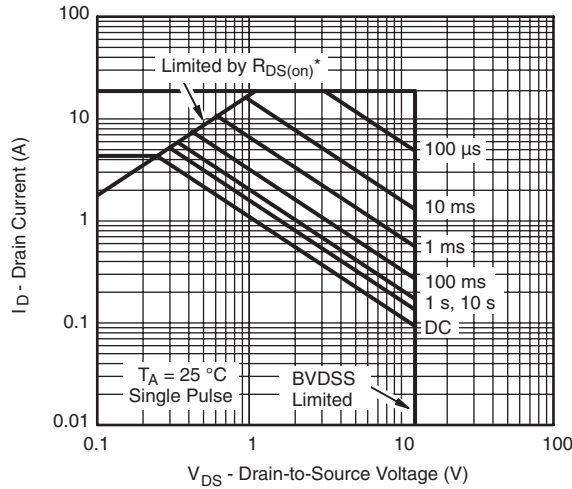


# SiA533EDJ

Vishay Siliconix

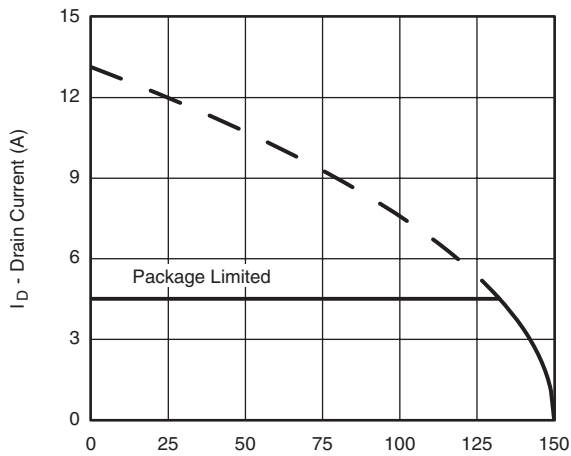


## N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



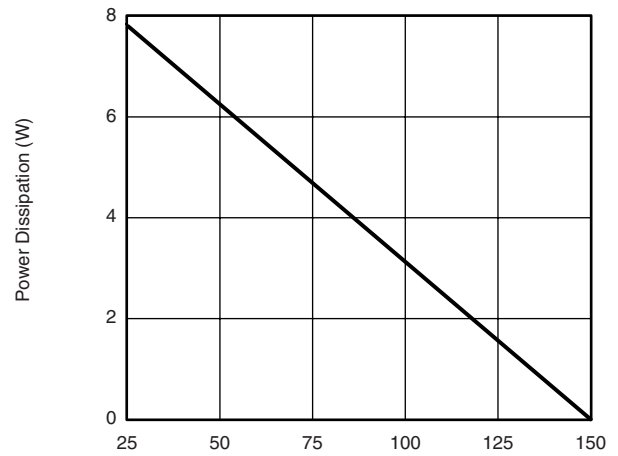
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

### Safe Operating Area, Junction-to-Ambient



$T_C$  - Case Temperature (°C)

### Current Derating\*



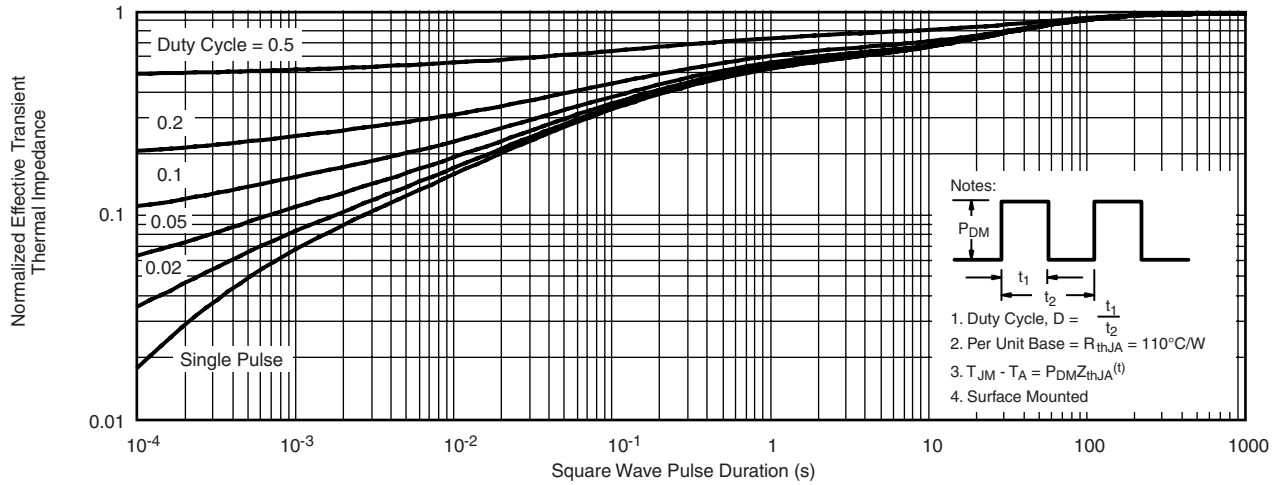
$T_C$  - Case Temperature (°C)

### Power Derating

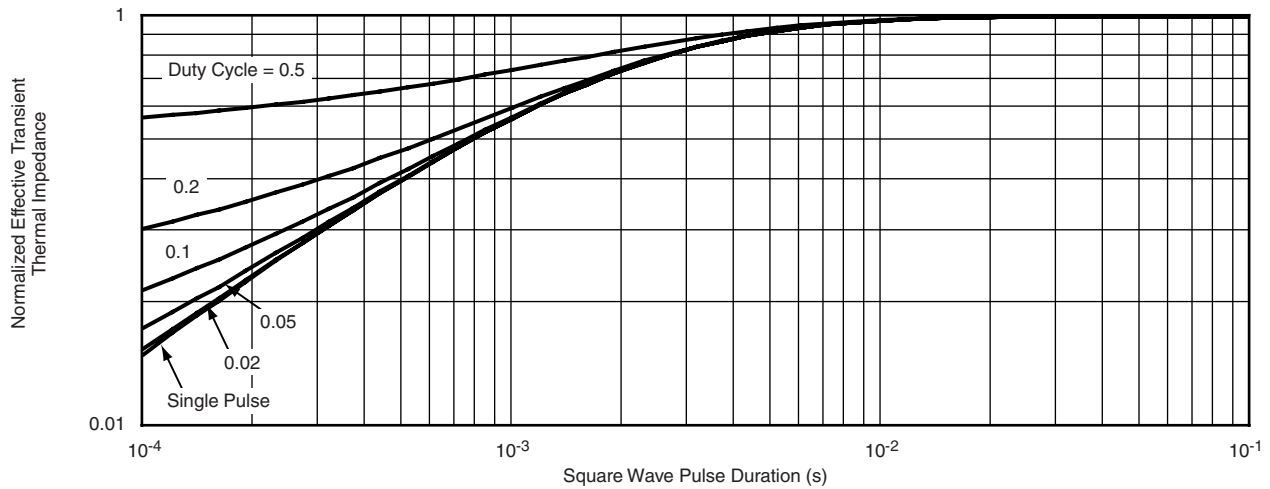
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



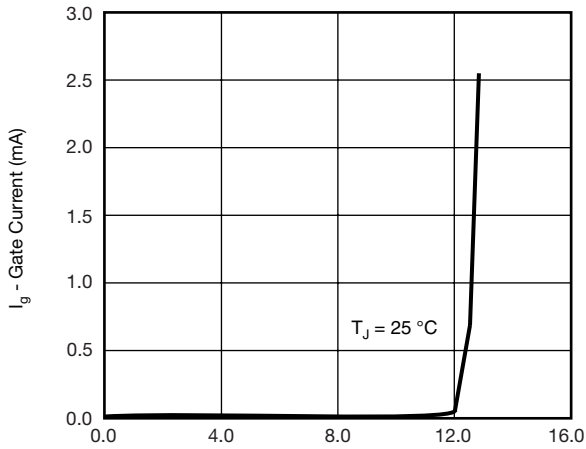
**Normalized Thermal Transient Impedance, Junction-to-Case**

# SiA533EDJ

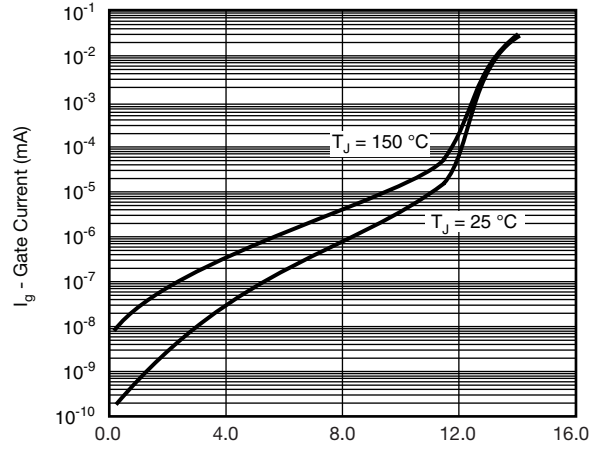
Vishay Siliconix



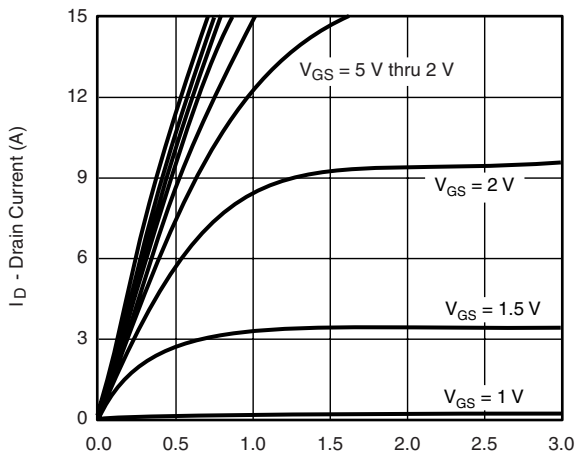
## P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



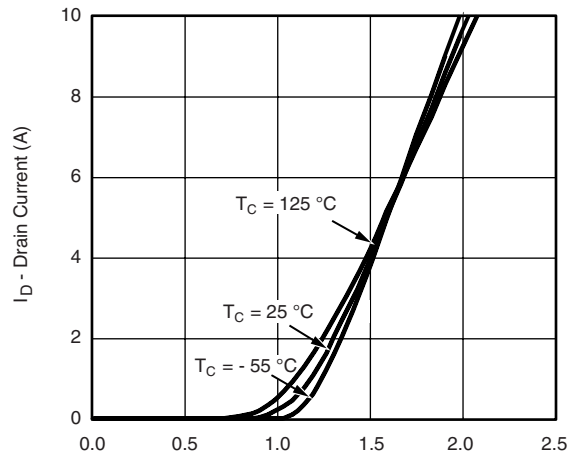
$V_{GS}$  - Gate-to-Source Voltage (V)  
**Gate Current vs. Gate-Source Voltage**



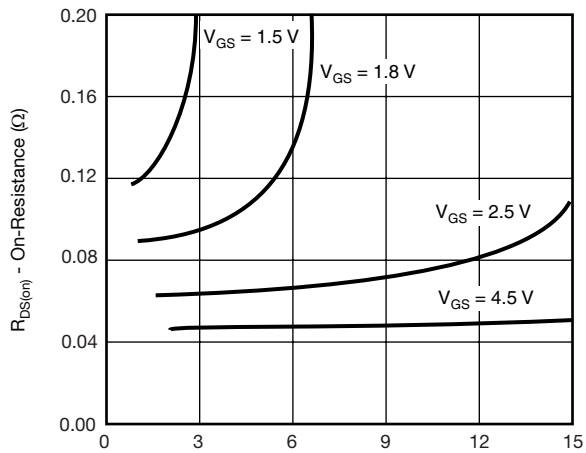
$V_{GS}$  - Gate-to-Source Voltage (V)  
**Gate Current vs. Gate-Source Voltage**



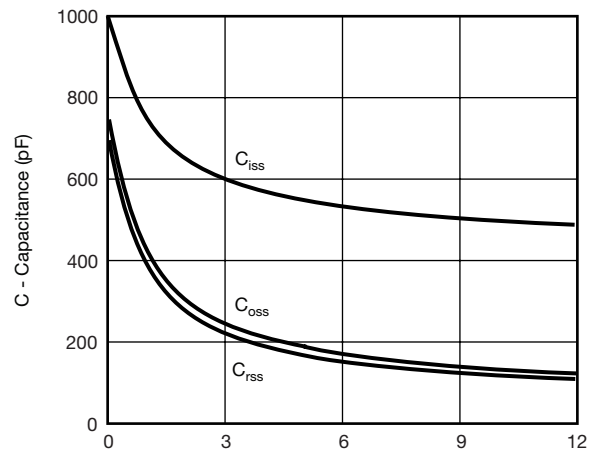
$V_{DS}$  - Drain-to-Source Voltage (V)  
**Output Characteristics**



$V_{GS}$  - Gate-to-Source Voltage (V)  
**Transfer Characteristics**



$I_D$  - Drain Current (A)  
**On-Resistance vs. Drain Current and Gate Voltage**

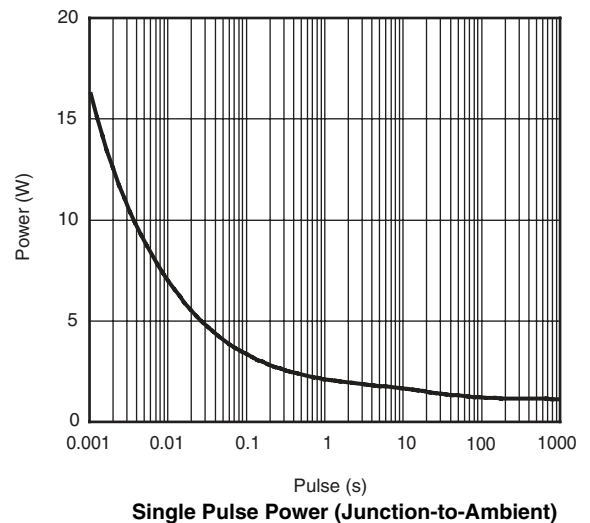
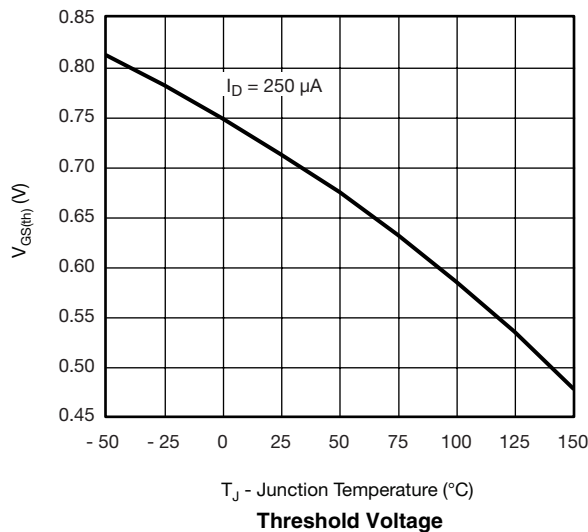
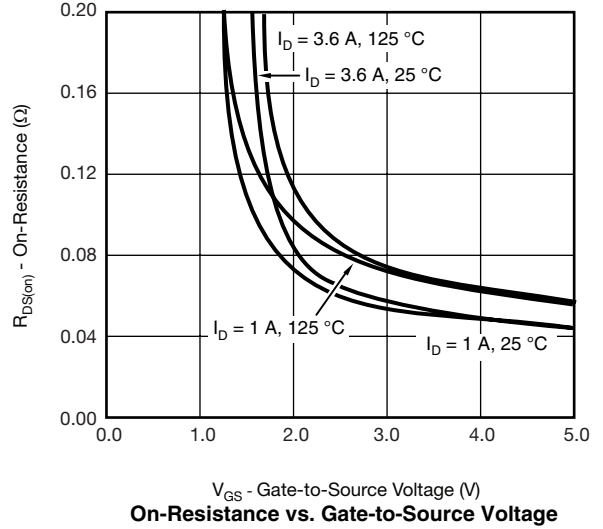
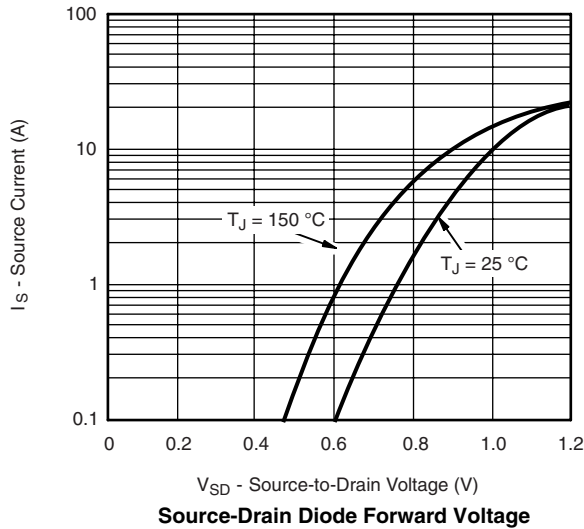
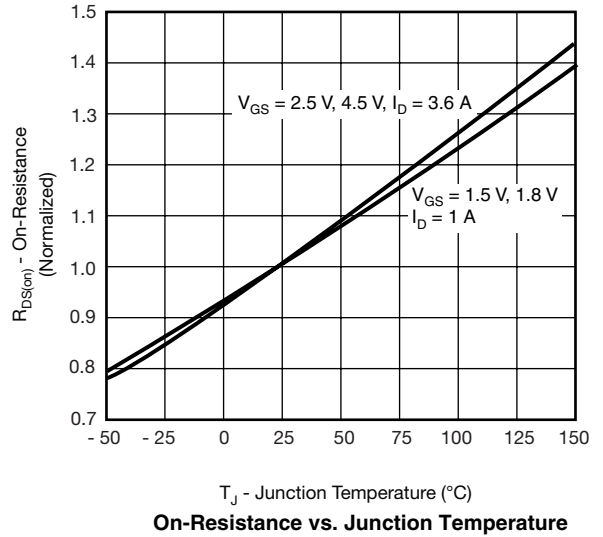
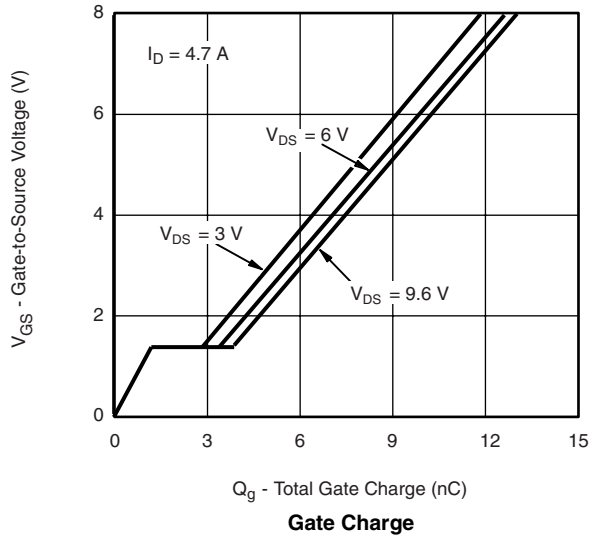


$V_{DS}$  - Drain-to-Source Voltage (V)  
**Capacitance**





**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

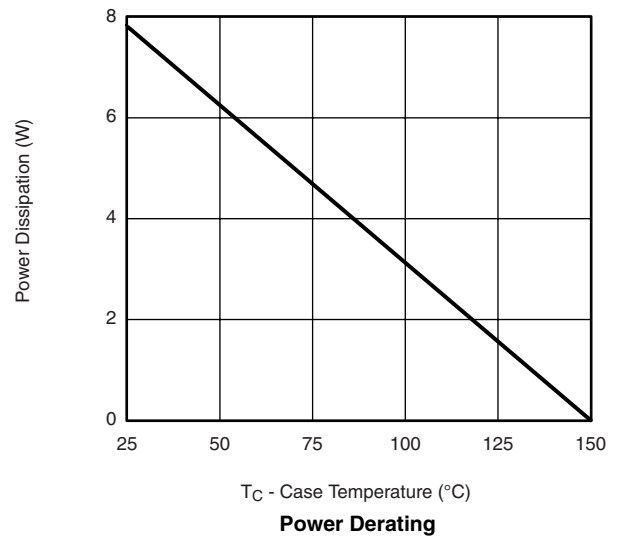
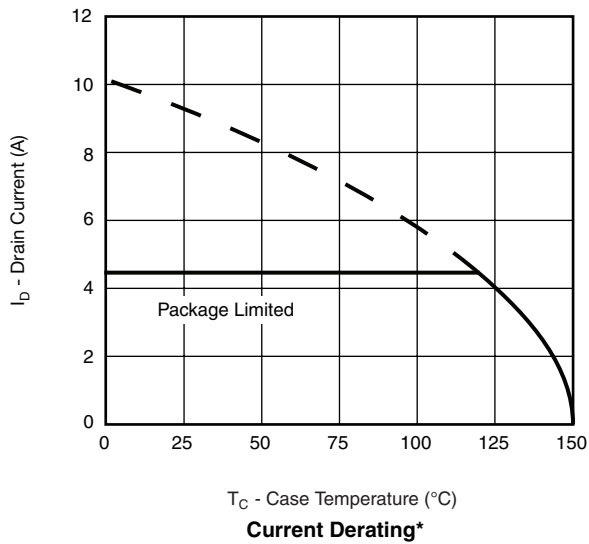
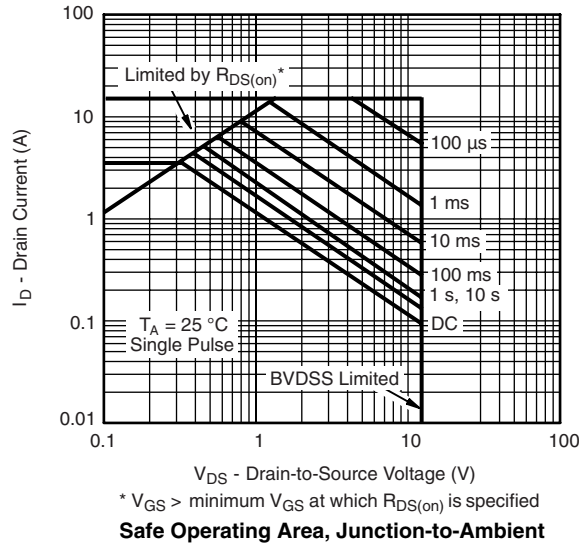


# SiA533EDJ

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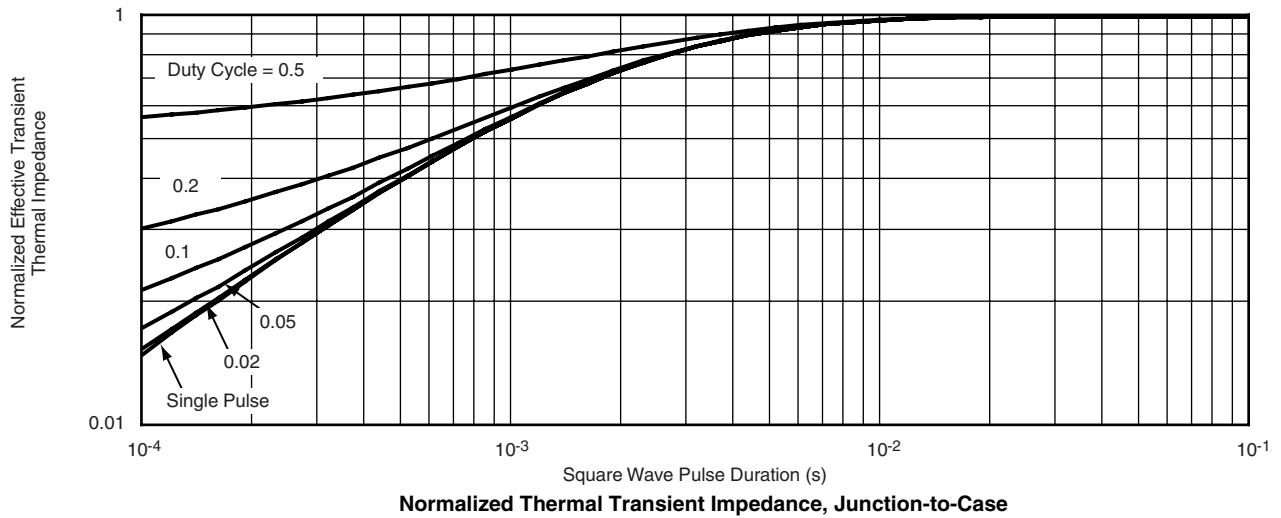
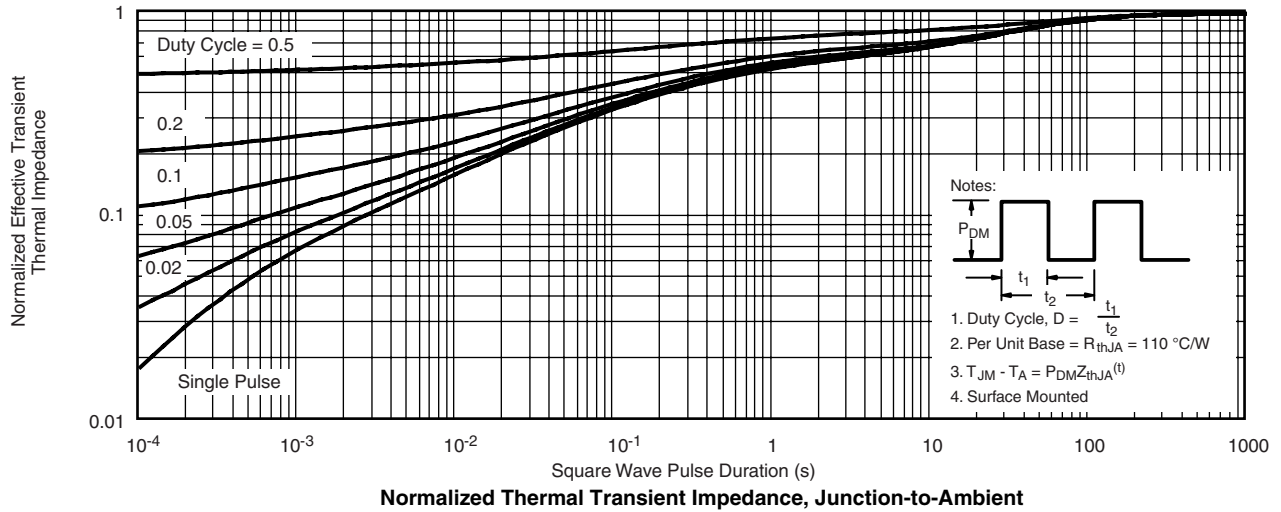
## P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



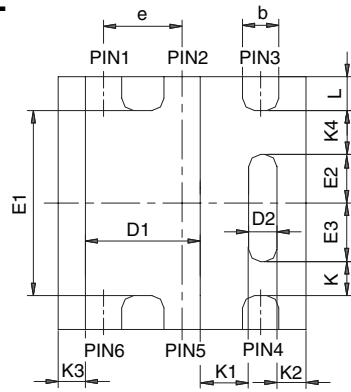
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



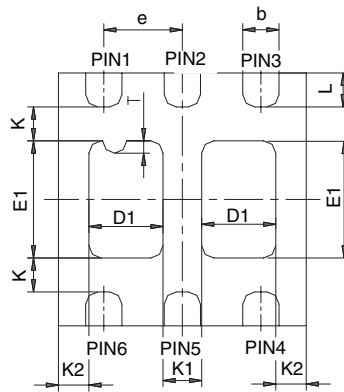
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?65706](http://www.vishay.com/ppg?65706).



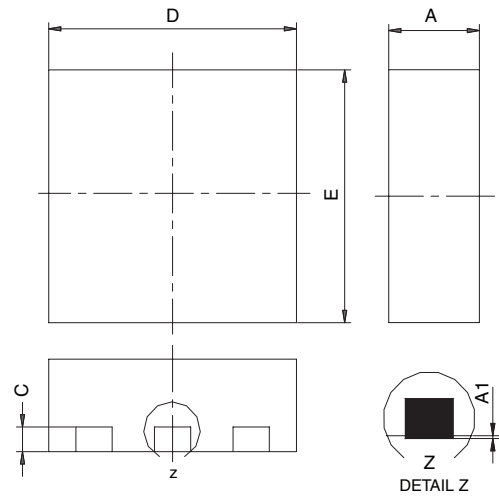
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



- Notes:  
 1. All dimensions are in millimeters  
 2. Package outline exclusive of mold flash and metal burr  
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

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 DWG: 5934





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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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