



# Small Signal Diodes

Vishay Semiconductor (Austria) Ges.m.b.H.

# QualPack

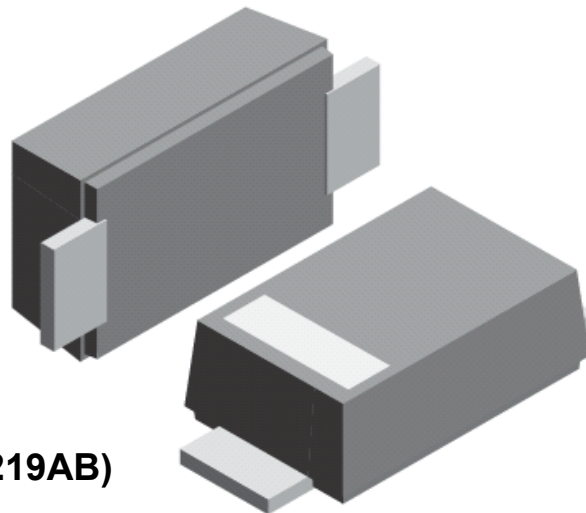


**VTVS3V3ASMF-M to VTVS63GSMF-M**

**400 W TransZorb® Transient Voltage Suppressor (TVS) Diode**



## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M



SMF (DO-219AB)

**AUTOMOTIVE  
GRADE**  
Available



**RoHS  
COMPLIANT**  
**HALOGEN  
FREE**

Base P/N-M – halogen-free, RoHS-compliant, and commercial grade

# VTVS3V3ASMF-M to VTVS63GSMF-M

## 400 W TransZorb® Transient Voltage Suppressor (TVS) Diode



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# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

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## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 2. General Product Information

**Product Name** VTVS3V3ASMF-M to VTVS63GSMF-M  
**Function** 400 W TransZorb® Transient Voltage Suppressor (TVS) Diode  
**Package** SMF (DO-219AB)

**Locations:**

Process: Locations:	Wafer Plant	Assembly Plant	Final Test	Quality Assurance
Vishay Voecklabruck, Austria				X
Vishay Heilbronn, Germany	X			X
Vishay Budapest, Hungary				
Vishay Shanghai, China		X	X	X
Vishay Taipei, Taiwan				
Subcon Jinan, China (commercial grade only)			X	

**Quality Management Vöcklabruck / AUSTRIA**

QA Small-Signal-Diodes



## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 3. Technology Information

Features:

- 400 W peak pulse power capability with a 10/1000  $\mu$ s waveform
- Tolerance of the avalanche breakdown voltage
  - $\pm 5\%$  VTVSxxxA
  - $\pm 2\%$  VTVSxxxG...
- Low-profile package
- Wave and reflow solderable
- ESD-protection acc. IEC 61000-4-2
  - $\pm 30$  kV contact discharge
  - $\pm 30$  kV air dischargeLow
- Excellent clamping capability
- "Low-Noise" technology - very fast response time
- MSL level 1 (according J-STD-020)
- Lead (Pb)-free termination finish (e3- Sn)
- AEC Q101 qualified available
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

#### 3.1 Process Technology

Process name:		PET3
Base material:	- material	n-Silicon
	- thickness (finished)	200 $\mu$ m
	- diameter	6 Inch
Passivation:	- material	CVD Layer
Front metallization:	- material	TiPdAg and Ag-bump
Back metallization:	- material	NiVAg

#### 3.2 Chip Description

Chip name	5V0	T3843D
	8V5.....36	T3844D
	40.....63	T3845D
Chip size		1300 $\mu$ m x 1300 $\mu$ m
Number of masks:		4



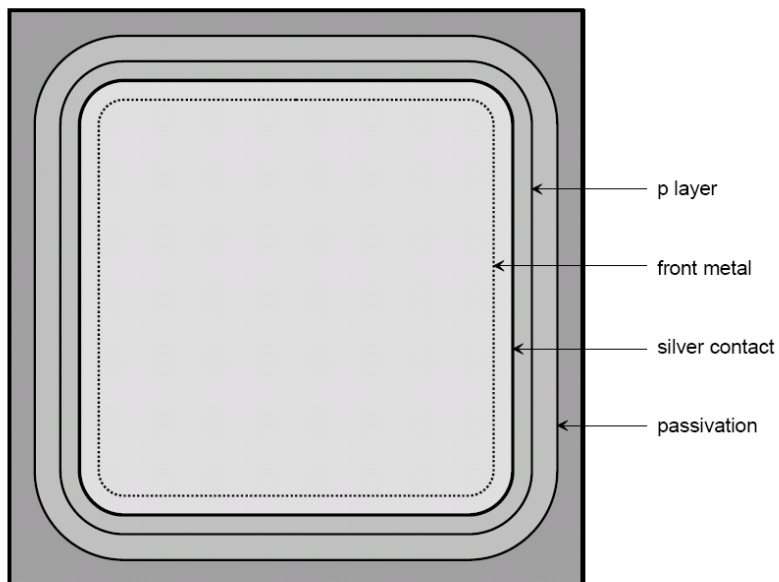
## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### Device Cross Sections

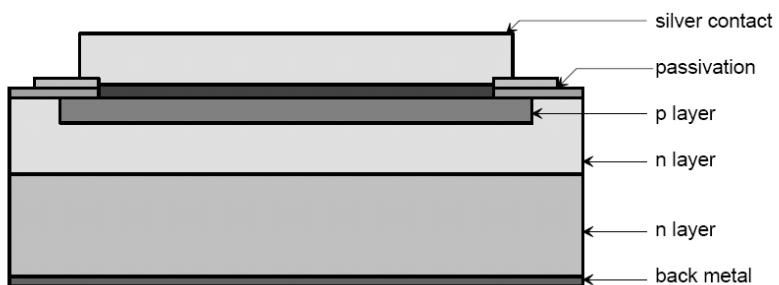
T3843D, T3844D, T3845D

both views are not scaled

Top View:



Sectional View:





## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 3.3 Package Technology

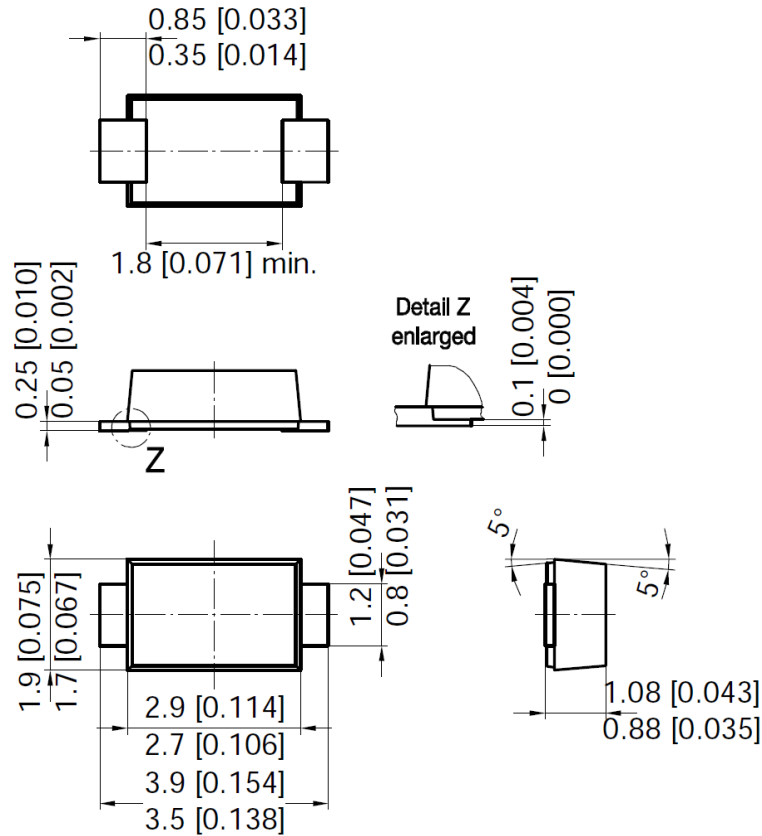
<b>Package type:</b>		<b>SMF (DO-219AB)</b>
Package weight:		14,8 mg
Chip separation method:		Sawing
Leadframe:	<ul style="list-style-type: none"> <li>- material</li> <li>- internal plating</li> <li>- lead finish</li> <li>- thickness of plating</li> </ul>	Cu Fe2 P None Sn – matte ≥ 7 µm annealed 1h / 150°C
Die attach (folded frame with dimple):		Solder paste PbSnAg
Package:	- material	Epoxy
Marking:	- method	CO2 Laser
Coding:	- method	Packing label / Barcode
Packing:	- SPEC	IEC 60286 – 3
	Tape <ul style="list-style-type: none"> <li>- type</li> <li>- material</li> </ul>	Carrier tape 8mm PE or PC, antistatic
	Reel <ul style="list-style-type: none"> <li>- type</li> <li>- material</li> <li>- size</li> <li>- number per</li> </ul>	Reel PS antistatic 180 / 330 mm diameter 3000 / 10000 pieces

### 3.4 Test

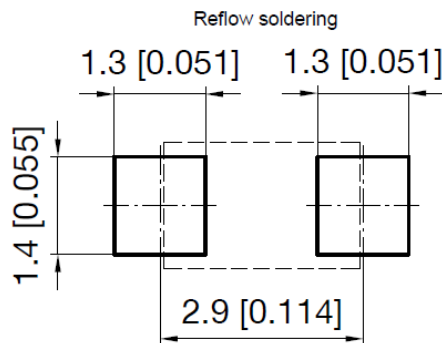
Test equipment:	Purchased
Test temperature	23 ± 3°C
Special tests	none

### 3.5 Package Dimensions

SMF (DO-219AB) (Dimension in mm (Inches))



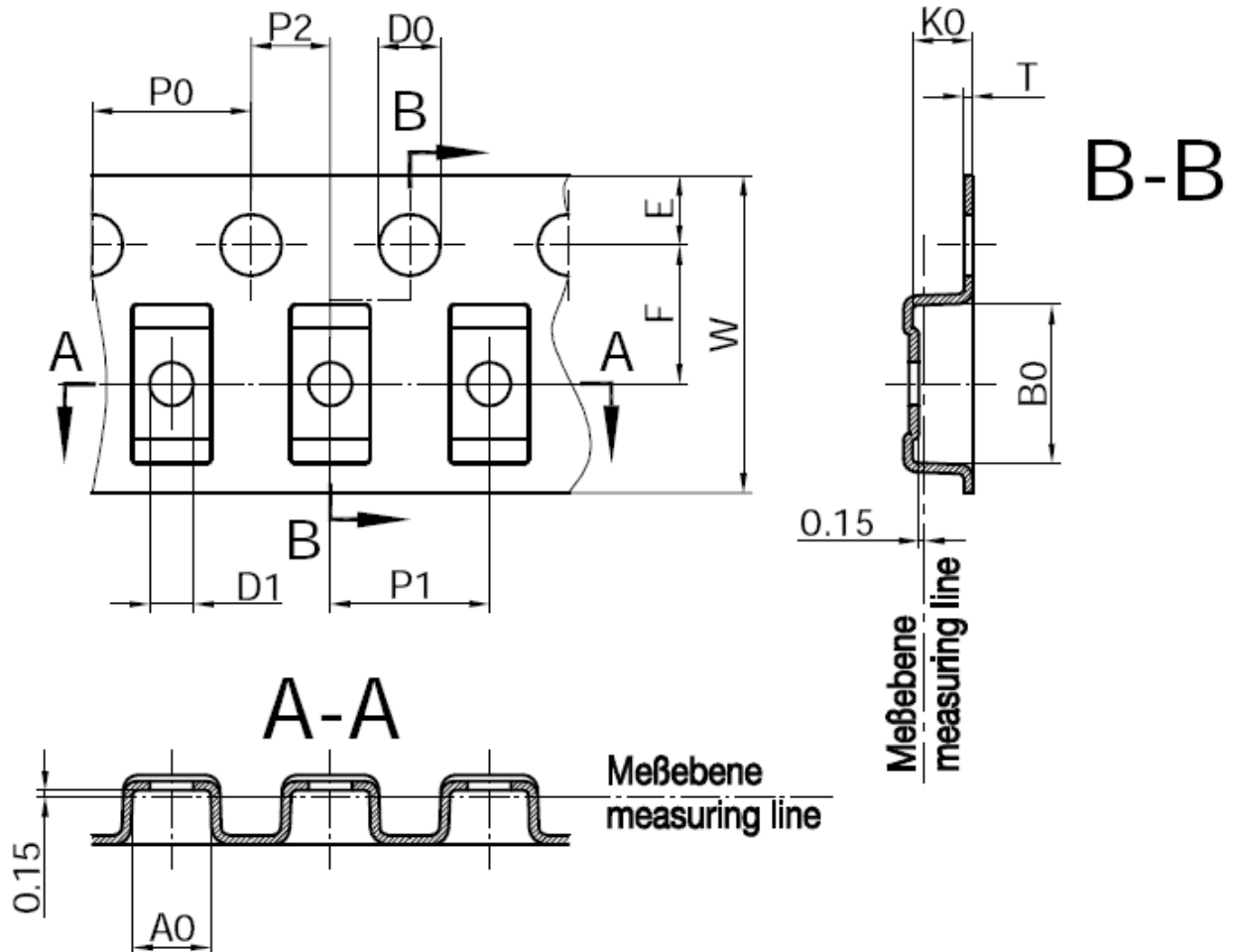
foot print recommendation:





### 3.6 Reel Dimensions

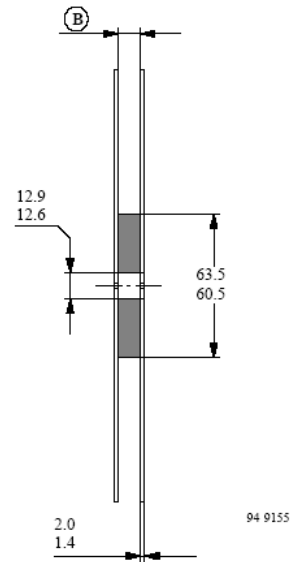
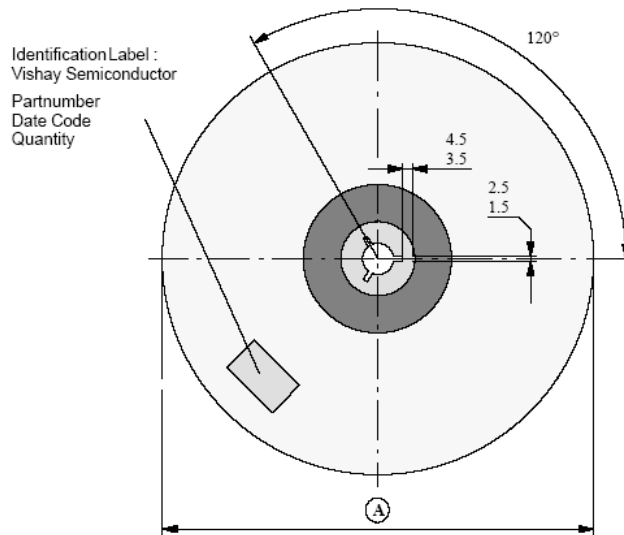
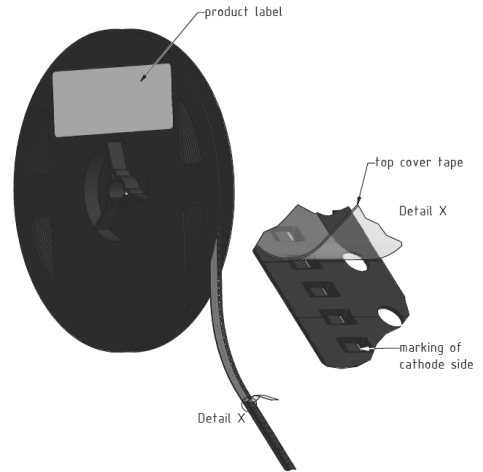
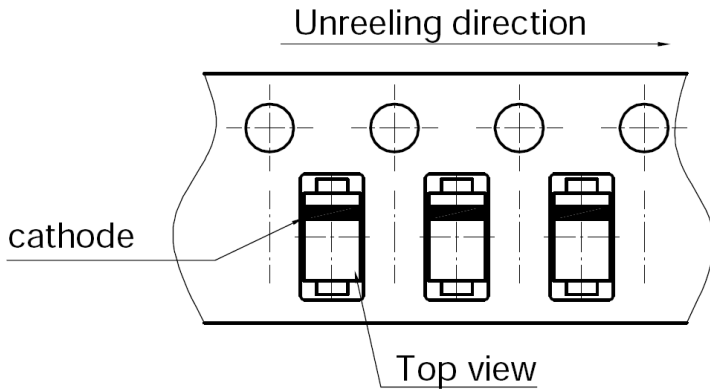
SMF (DO-219AB) (Dimensions in mm)



Mat:	A0	B0	K0	W	T	P0	P2	P1	D0	D1	E	F
C 100	1.97±0.07	4.0±0.1	1.5±0.1	8.0±0.2	0.235±0.03	4.0±0.1	2.0±0.05	4.0±0.1	1.5 <sup>+0.1</sup> <sub>-0</sub>	1 <sup>+0.1</sup> <sub>-0</sub>	1.75±0.1	3.5±0.05
PS 100	1.97±0.07	4.0±0.1	1.5±0.1	8.0±0.2	0.25±0.03	4.0±0.1	2.0±0.05	4.0±0.1	1.5 <sup>+0.1</sup> <sub>-0</sub>	1 <sup>+0.1</sup> <sub>-0</sub>	1.75±0.1	3.5±0.05



# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M



A: 180 –2 mm or 330 – 2 mm  
B: 8.4 to 10.4 mm or 12.4 to 14.4 mm



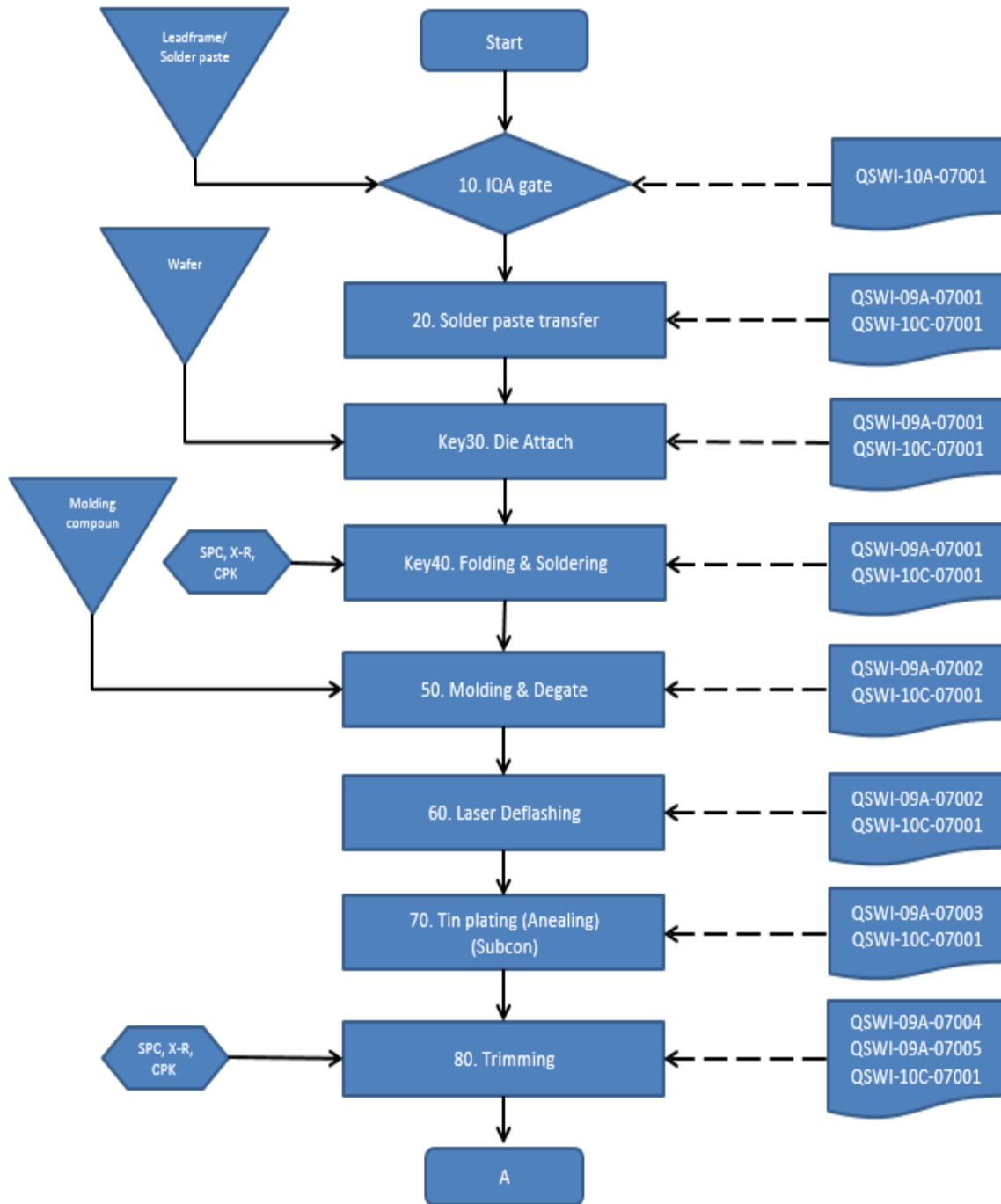
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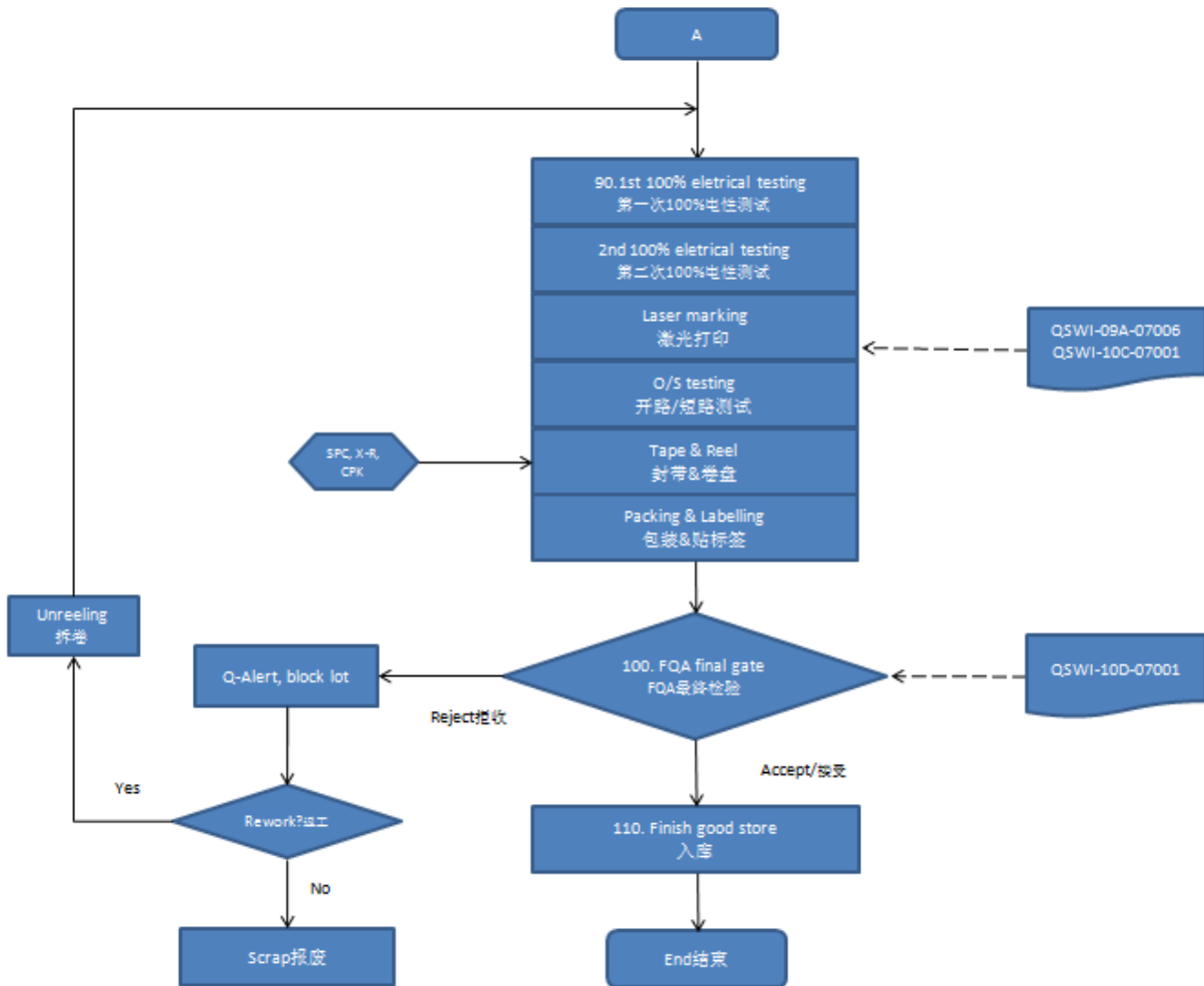
## 3.7 Wafer Process Control

Template 04.09.2009

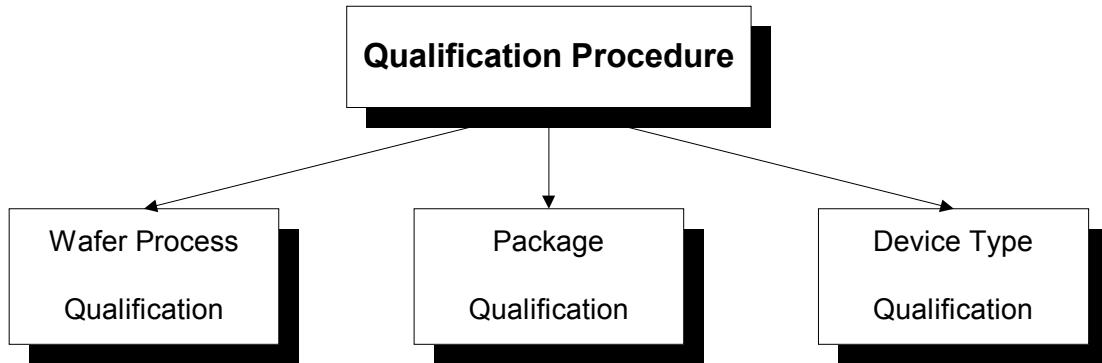
	<b>FAB 4 VSG</b>	<b>PROCESS / INSPECTION FLOWCHART</b>		<b>PF XWAF 083</b>
	<b>HN</b>	<b>ZENER_PET3 (reference type T3224D33-6W)</b>		Release 2 17.12.2015
The information included herein is property of VISHAY Semiconductor GmbH and for use only by the individual or entity to which it is addressed.				
<p style="font-size: x-small;">Legend:    <input type="radio"/> Prototype                      <input type="radio"/> Ramp Up                      <input checked="" type="radio"/> Production  <input type="radio"/> Operation                      <input type="checkbox"/> Transportation                      <input type="checkbox"/> Inspection                      <input type="checkbox"/> Delay                      <input type="checkbox"/> Storage</p>				
<input type="radio"/> Operation or Event <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>		Description of Operation or Event		Evaluation and Analysis Methods
ROUTE : EP20_6000				
x	x	x	oxidation	thickness, Nanospec
x	x	x	lithography	pattern,visual inspection, microscope
x	x	x	etching	QC, visual inspection, microscope
x	x	x	boron implantaion	sheet resistance, Prometrix
x	x	x	boron diffusion	sheet resistance, Prometrix
ROUTE : EP30_6000				
x	x	x	lithography	pattern,visual inspection, microscope
x	x	x	etching	QC, visual inspection, microscope
x	x	x	phosphor predepositon	sheet resistance, Prometrix
x	x	x	phosphor diffusion	sheet resistance, Prometrix
x	x	x	lithography	pattern,visual inspection, microscope
x	x	x	etching	QC, visual inspection, microscope
ROUTE : EP42_6000				
x	x	x	boron implantation	sheet resistance, Prometrix
x	x	x	boron diffusion	sheet resistance, Prometrix
x	x	x	boron implantation	sheet resistance, Prometrix
x	x	x	boron diffusion	sheet resistance, Prometrix
ROUTE : EP50_6000				
confidential				
ROUTE : EP60_6000				
x	x	x	front side metal	thickness
x	x	x	strip photoresist	visual inspection
x	x	x	bump plating	bump height, visual inspection
x	x	x	back side metal	thickness, Fisherscope X-Ray
x	x	x	sample test	electrical parameters
<b>Originator:</b>		K.-H.Beuter		
<b>Released via ECN:</b>		DCCHN-53-2015		

### 3.8 Assembly Process Control





### 4. Qualification



All product qualifications are split into three distinct areas as shown above. This same procedure is also used to qualify a change. Before a product is released for use it must have been manufactured using a qualified process and package. Before a device is released for production processing it must also have successfully completed its required type specific qualification.

The standard tests which are used for this procedure are shown in the **"Qualification Test Plan"**.

The data shown for the various qualifications may be from structurally similar parts. The wafer process may be qualified using the same process but with a similar package. Similarly the package may be qualified using a similar wafer process.



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## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 4.1 Change Procedure

Changes are controlled by ECN (Engineering Change Notice). For major changes a customer notification procedure is installed. All customers using affected products have to be notified by PCN (Product Change Notification) at least 60 days prior to the implementation of the change.

A major change is defined as a change which affects the electrical and/or mechanical specification as defined in the data sheet.

Examples of a major change:

- Maximum and minimum data book specifications
- End of Life / Product obsolescence
- Manufacturing location (Site Change)
- Direct raw material
- Lead frame material/design
- Package material/design
- Solder/lead plating process



## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 4.2 Qualification Test Plan – ESD-Protection in Plastic Package

# DQD3000	STRESS	Abv	# of lots		SS per lot	Reference	Remarks
			device qual.	Family qual.			
	Pre- and Post-Stress Electrical Test	TEST			77	Data Sheet	
6.10	Pre-conditioning	PC				JESD22 A-113	Only performed at Surface Mount Devices (SMD)
1.11	External Visual	EV	1	3	All		
32.10	High Temperature Reverse Bias	HTRB	1	3	77	JESD22 A-108	
10.40	Temperature Cycling	TC	1	3	77	JESD22 A-104	
12.10	Autoclave	AC	1	3	77	JESD22 A-102	
11.11	High Humidity High Temp. Reverse Bias	H <sup>3</sup> TRB	1	3	77	JESD22 A-101	
7.13	ESD Characterization	Contact disc.	1	1	10	IEC 61000-4-2	
7.14	ESD Characterization	Air disc	1	1	10	IEC 61000-4-2	
1.10	Physical Dimension	PD	1	1	30	JESD22 B-100	
10.21	Resistance to Solder Heat	RSH	1	1	30	JESD22 B-106	
3.1X	Solderability	SD	1	3	10	J-STD-002	Only at SMD
4.1x	Dissolution of metallization	SD	1	3	10	J-STD-002	Only at SMD
31.10	High temp. storage	HTS	1	1	77	MIL-STD-750 Method 1031	
31.20	Low temp. storage	LTS	1	1	77	IEC 68-2-2 Ba	
32.10	High Temperature Reverse Bias	HTRB	1	1	77-0	JESD22 A-108	





## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 4.3 Whisker Test Report

WHISKER TEST REPORT	
DIVISION	VISHAY SEMICONDUCTOR, DIODES DIVISION
PRODUCT GROUP	SMALL SIGNAL ZENER DIODES
PACKAGE STYLE:	DO-219AB (SMF)
LEAD FINISH:	Lead (Pb)-free termination finish = "e3" = matte tin (Sn)
ALSO VALID FOR:	
STANDARD:	JESD 201 class 2
DATE	2012-May-21

#### Whisker Testing Report

JESD201 Class	2
Family	
Package outline	DO-219AB(SMF)
P/N	S07G
Mfg loc	gchang Road,200436,S
Plating line	VSS
Plating type	In Line Plating
plating solution	
PB %	1.257PPM

Report Date	05.21.12
Finish	Matte
Underlayer	NA
Underlayer Spec	NA
Min thickness Uinch	354.33~472.44
Actual thickness	425,12
Min thickness Um	9~12
Actual thickness	10,80
Mitigation	Annealed 1h/150°C
DC	1138

SPEC: MAX allowable Tin whisker length 45um

Lot No.	Precondition	TC -55C/85C 10min		
		500C	1000C	1500C
1	Pbfree reflow	0	0	0
1	No reflow	0	0	0
1	Snpb reflow	0	0	0

SPEC: MAX allowable Tin whisker length 40um

Lot No.	Precondition	Temp./Humi. 30C/60%RH			
		1000H	2000H	3000H	4000H
1	Pbfree reflow	0	0	0	0
1	No reflow	0	0	0	0
1	Snpb reflow	0	0	0	0

SPEC: MAX allowable Tin whisker length 40um

Lot No.	Precondition	High Temp./Humi. 55C/85%RH			
		1000H	2000H	3000H	4000H
1	Pbfree reflow	0	0	0	13,7
1	No reflow	0	0	0	23,3
1	Snpb reflow	0	0	0	21



## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### Detail Whisker Testing Data

#### Preconditioning: Pbfree reflow

Lot #	Devi ce No.	Chec k Point	TC -55C/85C 10min			Temp./Humi. 30C/60%RH				High Temp./Humi. 55C/85%RH			
			500C	1000C	1500C	1000H	2000H	3000H	4000H	1000H	2000H	3000H	4000H
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	2	0	0	0	0	0	0	0	0	0	0	0
1	2	3	0	0	0	0	0	0	0	0	0	0	0
1	2	4	0	0	0	0	0	0	0	0	0	0	13,7
1	3	5	0	0	0	0	0	0	0	0	0	0	11,5
1	3	6	0	0	0	0	0	0	0	0	0	0	0
MAX			0	0	0	0	0	0	0	0	0	0	13,7

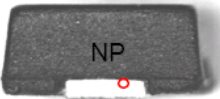
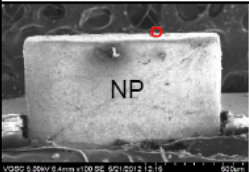
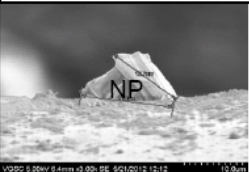
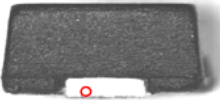
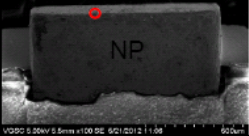
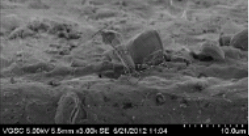
#### Preconditioning: No reflow

Lot #	Devi ce No.	Chec k Point	TC -55C/85C 10min			Temp./Humi. 30C/60%RH				High Temp./Humi. 55C/85%RH			
			500C	1000C	1500C	1000H	2000H	3000H	4000H	1000H	2000H	3000H	4000H
1	1	1	0	0	0	0	0	0	0	0	0	0	13
1	1	2	0	0	0	0	0	0	0	0	0	0	12,8
1	2	3	0	0	0	0	0	0	0	0	0	0	17,4
1	2	4	0	0	0	0	0	0	0	0	0	0	14,1
1	3	5	0	0	0	0	0	0	0	0	0	0	23,3
1	3	6	0	0	0	0	0	0	0	0	0	0	22,5
MAX			0	0	0	0	0	0	0	0	0	0	23,3

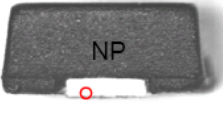
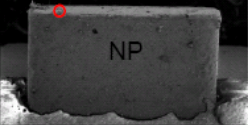

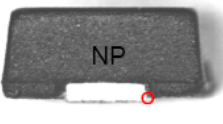
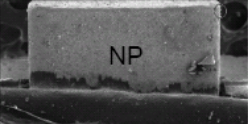
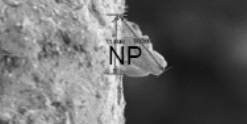
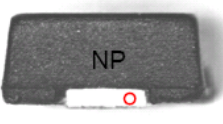


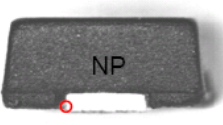
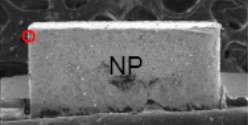
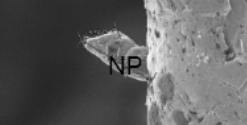
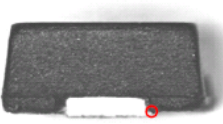
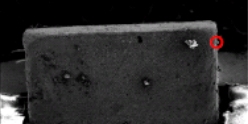
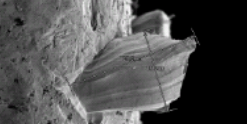
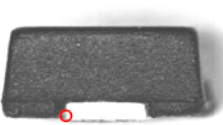
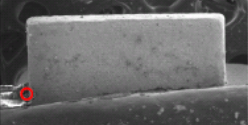
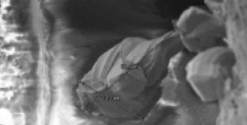
#### Preconditioning: Snpb reflow

Lot #	Devi ce No.	Chec k Point	TC -55C/85C 10min			Temp./Humi. 30C/60%RH				High Temp./Humi. 55C/85%RH			
			500C	1000C	1500C	1000H	2000H	3000H	4000H	1000H	2000H	3000H	4000H
1	1	1	0	0	0	0	0	0	0	0	0	0	21
1	1	2	0	0	0	0	0	0	0	0	0	0	9,92
1	2	3	0	0	0	0	0	0	0	0	0	0	18,6
1	2	4	0	0	0	0	0	0	0	0	0	0	14
1	3	5	0	0	0	0	0	0	0	0	0	0	10,6
1	3	6	0	0	0	0	0	0	0	0	0	0	8,18
MAX			0	0	0	0	0	0	0	0	0	0	21

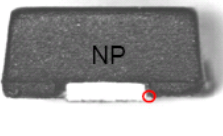
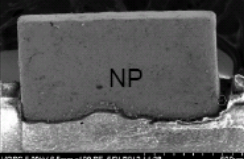

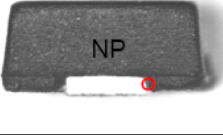
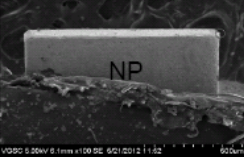
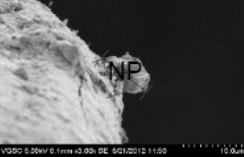
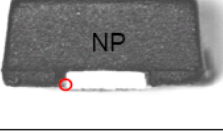
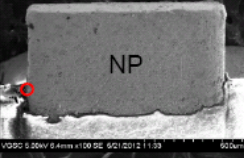
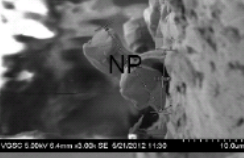
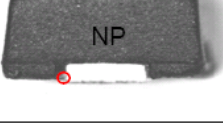
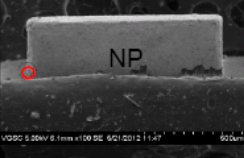

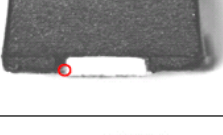
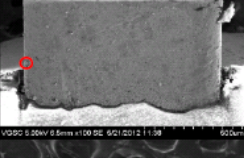

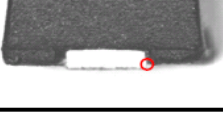
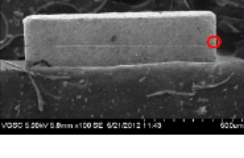

## Preconditioning: Pbfree reflow

Lot #	Device No.	Check Point	High Temp./Humi. 55C/85%RH			4000H
1	1	1	NP	NP	NP	0
1	1	2	NP	NP	NP	0
1	2	3	NP	NP	NP	0
1	2	4				13,7
1	3	5				11,5
1	3	6	NP	NP	NP	0

## Preconditioning: No reflow

Lot #	Device No.	Check Point	High Temp./Humi. 55C/85%RH			4000H
1	1	1				13
1	1	2				12,8
1	2	3				17,4
1	2	4				14,1
1	3	5				23,3
1	3	6				22,5

**Preconditioning: Snpb reflow**

Lot #	Device No.	Check Point	High Temp./Humi. 55C/85%RH			4000H
1	1	1				21
1	1	2				9,92
1	2	3				18,6
1	2	4				14
1	3	5				10,6
1	3	6				8,18

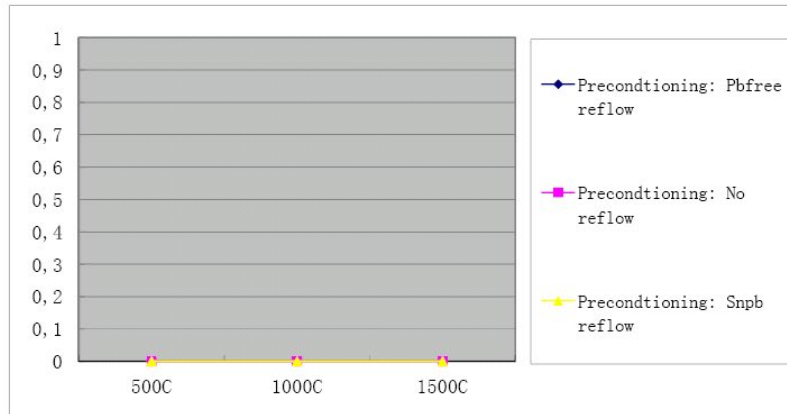




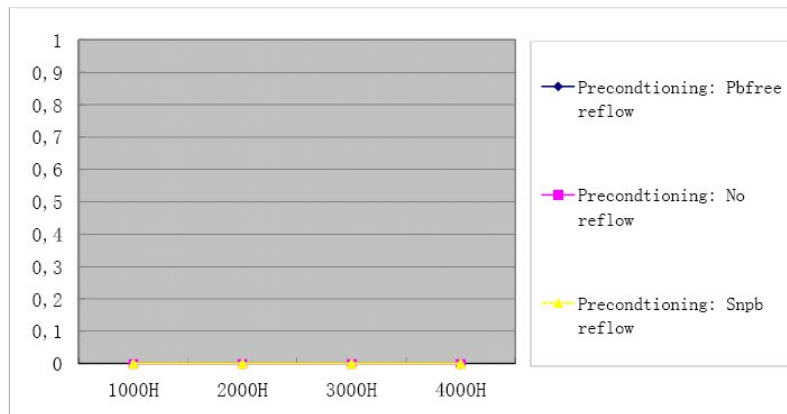
## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

Trend Chart

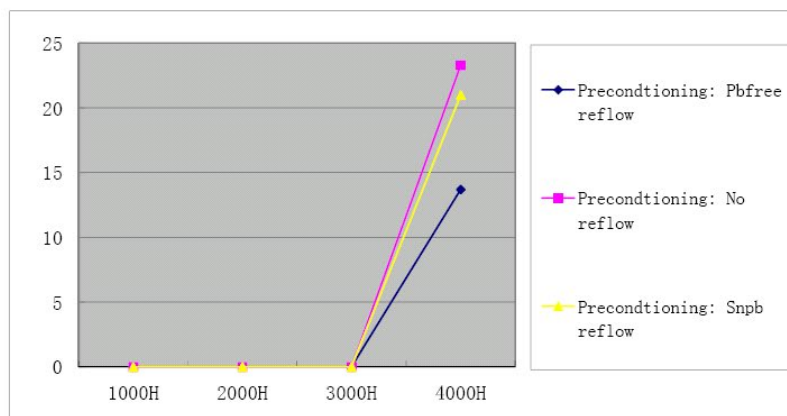
Test condition TC -55C/85C 10min



Test condition Temp./Humi. 30C/60%RH



Test condition High Temp./Humi. 55C/85%RH





## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 4.4 ESD Classification

# ESD – CLASSIFICATION

ESD CLASSIFICATION		RESULT	
		WITHSTAND VOLTAGE	FAIL/PASS
HMB	HUMAN BODY MODEL	$\geq 8000$ V	0/10
MM	MACHINE MODEL	$\geq 800$ V	0/10

#### ESD CLASSIFICATION LEVELS:

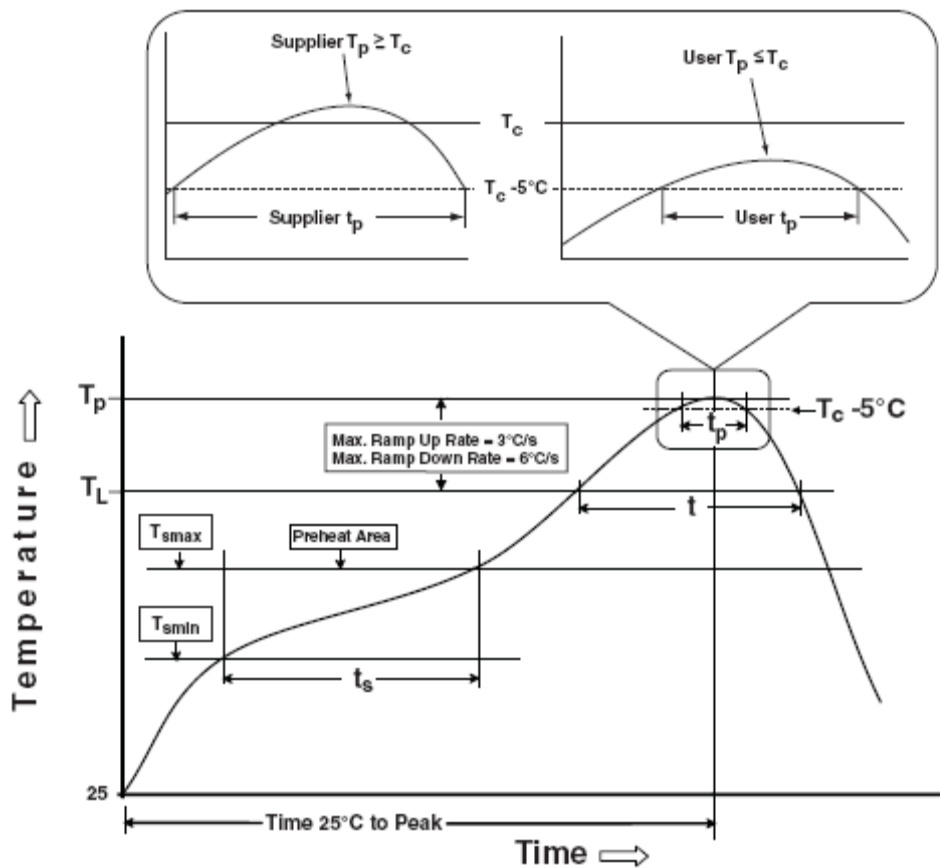
HUMAN BODY MODEL 1500 Ohm / 100 pF	WITHSTAND VOLTAGE	AEC Q101-001	ESD STM5.1 - 1998	Mil-Std-750D JESD22-A114-A
	< 250 V	H0	CLASS 0	CLASS 0
	250 V TO < 500 V	H1A	CLASS 1A	CLASS 1A
	500 V TO < 1000 V	H1B	CLASS 1B	CLASS 1B
	1000 V TO < 2000 V	H1C	CLASS 1C	CLASS 1C
	2000 V TO < 4000 V	H2	CLASS 2	CLASS 2
	4000 V TO < 8000 V	H3A	CLASS 3A	CLASS 3A
	> 8000 V	H3B	CLASS 3B	CLASS 3B
MACHINE MODEL 0 Ohm / 200 pF	WITHSTAND VOLTAGE	AEC Q101-002	ESD STM5.2 - 2009	JESD22-A115-A
	< 25 V	M0	M1A	A
	25 V TO < 50 V	M1A	M1B	A
	50 V TO < 100 V	M1B	M1C	A
	100 V TO < 200 V	M2	M2	A
	200 V TO < 400 V	M3	M3	B
	> 400 V	M4	M4	C

5. User Information  
 5.1 Reflow Soldering

As per IPC/JEDEC J-STD-020E

- total restricted to 3 soldering operations maximum

*Temperature/Time Profile - Infrared-Soldering*



IPC-020d-5-1





# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

**Table 5-2 Classification Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat/Soak</b>		
Temperature Min ( $T_{smin}$ )	100 °C	150 °C
Temperature Max ( $T_{smax}$ )	150 °C	200 °C
Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	60-120 seconds	60-120 seconds
Ramp-up rate ( $T_L$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time ( $t_L$ ) maintained above $T_L$	60-150 seconds	60-150 seconds
Peak package body temperature ( $T_p$ )	For users $T_p$ must not exceed the Classification temp in Table 4-1. For suppliers $T_p$ must equal or exceed the Classification temp in Table 4-1.	For users $T_p$ must not exceed the Classification temp in Table 4-2. For suppliers $T_p$ must equal or exceed the Classification temp in Table 4-2.
Time ( $t_p$ )* within 5 °C of the specified classification temperature ( $T_c$ ), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate ( $T_p$ to $T_L$ )	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		

**Note 1:** All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live bug assembly reflow orientation (i.e., dead-bug),  $T_p$  shall be within  $\pm 2$  °C of the live bug  $T_p$  and still meet the  $T_c$  requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

**Note 2:** Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in this table.

For example, if  $T_c$  is 260 °C and time  $T_p$  is 30 seconds, this means the following for the supplier and the user:

- For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.
- For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

**Note 3:** All components in the test load shall meet the classification profile requirements.

**Note 4:** SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

**Table 4-1 SnPb Eutectic Process – Classification Temperatures ( $T_c$ )**

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

**Table 4-2 Pb-Free Process – Classification Temperatures ( $T_c$ )**

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350 - 2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

**Note 1:** Package “volume” excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks. Package volume includes the external dimensions of the package body, regardless if it has a cavity or is a passive package style.

**Note 2:** At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature ( $T_p$ ) can exceed the values specified in table 4-1 or 4-2. The use of a higher  $T_p$  does not change the classification temperature ( $T_c$ ).

**Note 3:** The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

**Note 4:** Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Tables 4-2 and 5-2, whether or not Pb-free.

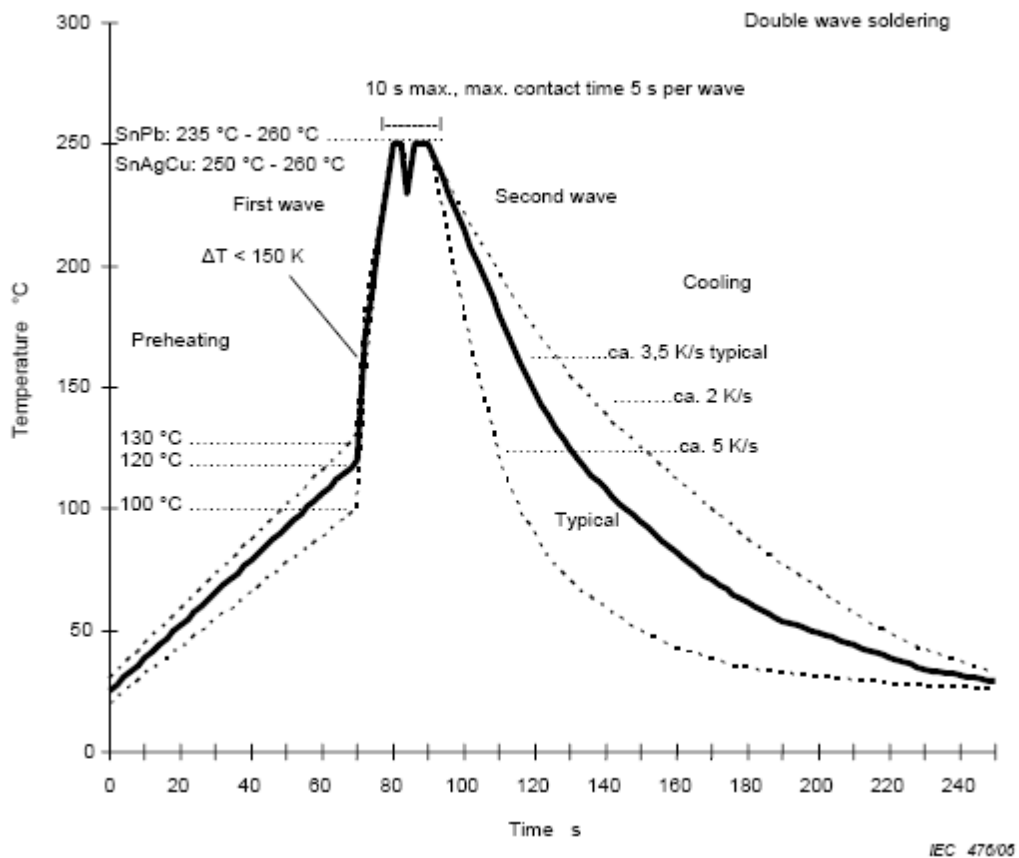
**Note 5:** SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

## 5.2 Double Wave Soldering

As per IEC 61760-1

- maximum 2x
- total restricted to 3 soldering operations maximum

### Temperature/Time Profile – Double Wave





## **6. Environmental Information**

### **6.1 Environmental Policy**

Vishay Small Signal Products has defined Environmental policy aimed at

- reducing the use of harmful chemicals in its processes
- reducing the content of harmful materials in its products
- using recyclable materials wherever possible
- reducing the energy content of its products

As part of that plan no ozone depleting chemicals are known to be used by either Vishay Small Signal Products or its sub-contractors processes.

All production sites are certified according to the international environmental standard ISO 14001.

### **6.2 Declaration of Material Contents**



# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M



## SEMICONDUCTOR Small Signal Products

### MATERIAL CONTENT LIST

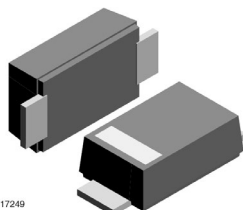
PACKAGE  
FAMILY:  
DATE:  
REVISION:

**DO-219AB-M (SMF)**

21-Jan-2020  
8

**HALOGEN  
FREE**

**RoHS  
COMPLIANT**



17249



MATERIAL CONTENT					
Part	Material	CAS N°	weight mg	% of weight	ppm of total weight
<b>Lead frame</b> 42,8%	Cu	7440-50-8	6,20	97,45%	417218
	Fe	7439-89-6	0,15	2,40%	10275
	Zn	7440-66-6	0,008	0,12%	514
	P	7723-14-0	0,002	0,03%	129
	<b>TOTAL</b>		<b>6,36</b>		
<b>Terminal finish</b> 1,4%	Sn	7440-31-5	0,210	100,0%	14137
	<b>TOTAL</b>		<b>0,21</b>		
<b>Die solder (solder paste)</b> 0,9%	Pb *)	7439-92-1	0,13	92,52%	8415
	Sn	7440-31-5	0,007	4,96%	451
	Ag	7440-22-4	0,003	2,52%	229
	<b>TOTAL</b>		<b>0,14</b>		
<b>Silicon chip</b> 3,2%	Si	7440-21-3	0,47	99,6%	31504
	Silicon dioxide	14808-60-7	0,002	0,43%	135
	And/or traces of Au,As,Ti,Ag,Al, Ni, Pd, Cu				
<b>TOTAL</b>		<b>0,47</b>			
<b>Molding compound</b> 51,7%	Fused Silica	60676-86-0	6,14	80,00%	413595
	Cured polymer (epoxy + phenolic resin reacted)	26834-02-6	1,45	18,93%	97867
	Carbon Balck	1333-86-4	0,04	0,52%	2688
	Mixed Siloxanes	trade secrete	0,04	0,55%	2843
	<b>TOTAL</b>		<b>7,68</b>		
<b>Total weight</b>			<b>14,86</b>		

Remark: Total weight range  $\pm 10\%$

\*) Lead in high melting temperature type solder acc. RoHS exempted

\*\*) N. D. = not detected

Reflow Soldering acc. J-STD-020

Material Analyses Reports available on request



# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

## 7. Other Data

### 7.1 Approval Certificates

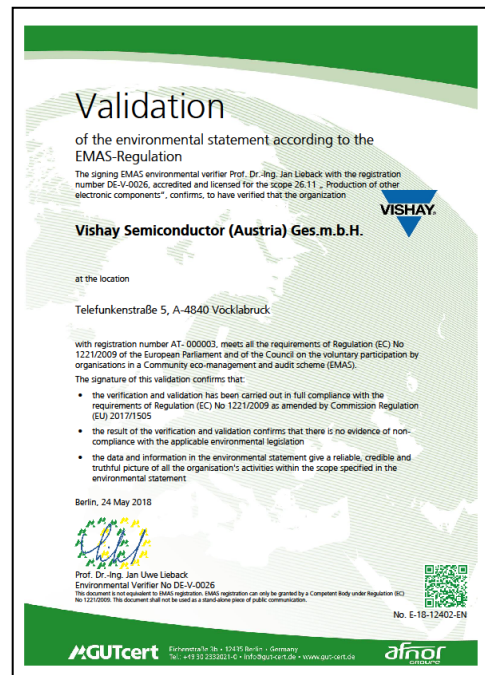
Vishay Semiconductor, Vöcklabruck, Austria

IATF16949 / ISO9001 / ISO14001 / OHSAS18001 / EMAS





# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M







# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

## Vishay Budapest, Hungary IATF16949 / OHSAS18001 (MSZ 28001) / ISO14001





# QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

## Vishay, Heilbronn, Germany IATF16949 / ISO9001 / ISO14001







# QualPack VTVS3V3ASM-F-M to VTVS63GSM-F-M

Vishay Shanghai, China  
IATF16949 / ISO 9001 / ISO14001 / BS OHSAS 18001

**Certificate**

Standard: **IATF 16949:2016**  
(1st edition, 2016-04-01)

Certificate Registr. No. 01 111 89463  
IATF Certificate No. 0317348

Certificate Holder: **Vishay Semiconductor Shanghai Co., Ltd.**  
No. 501 West Jiangchang Road, Jingan District,  
Shanghai 200436, P. R. China

With remote location(s) according to annex

Scope: Design and Manufacturing of Diodes

Proof has been furnished by means of an audit that the requirements of IATF 16949:2016 are met.

Issue date/Expiry date: The certificate is valid from 2018-07-19 until 2021-07-18.

Release date: 2018-07-19

*K. Fiebig*  
TÜV Rheinland Cert. Qualif.  
Am Gleisen Str. 51168 Köln 197W

2140-QMC 01003 102

www.tuv.com Precisely Right.

**Certificate**

Standard: **ISO 9001:2015**

Certificate Registr. No. 01 100 89463

Certificate Holder: **Vishay Semiconductor Shanghai Co., Ltd.**  
Unified Social Credit Code: 913100009073566510  
Registration Address: No. 501, West Jiangchang Road,  
Jingan District, Shanghai City 200436, P. R. China  
Operation Address: same as above

Scope: Design and Manufacturing of Diodes

Proof has been furnished by means of an audit that the requirements of ISO 9001:2015 are met.

Validity: The certificate is valid from 2018-07-16 until 2021-07-15.  
It remains valid subject to satisfactory surveillance audits.  
First certification 2004

This certificate information can be searched on CNCA official website <http://www.cnca.gov.cn>

2018-07-19

*K. Fiebig*  
TÜV Rheinland Cert. Qualif.  
Am Gleisen Str. 51168 Köln

www.tuv.com Precisely Right.

**Certificate**

Standard: **ISO 14001:2015**

Certificate Registr. No. 01 104 000495

Certificate Holder: **Vishay Semiconductor Shanghai Co., Ltd.**  
No. 501, West Jiangchang Road, Jing'an District,  
Shanghai city 200436, P. R. China

Scope: Design and Manufacturing of Diodes

Proof has been furnished by means of an audit that the requirements of ISO 14001:2015 are met.

Validity: The certificate is valid from 2018-09-15 until 2021-09-14.  
It remains valid subject to satisfactory surveillance audits.  
First certification 2001

2018-09-21

*K. Fiebig*  
TÜV Rheinland Cert. Qualif.  
Am Gleisen Str. 51168 Köln

www.tuv.com Precisely Right.

**Certificate**

Standard: **BS OHSAS 18001:2007**

Certificate Registr. No. 01 113 000495

Certificate Holder: **Vishay Semiconductor Shanghai Co., Ltd.**  
No. 501, West Jiangchang Road, Jing'an District,  
Shanghai city 200436, P. R. China

Scope: Design and Manufacturing of Diodes

Proof has been furnished by means of an audit that the requirements of BS OHSAS 18001:2007 are met.

Validity: The certificate is valid from 2018-09-15 until 2021-03-11.  
It remains valid subject to satisfactory surveillance audits.  
First certification 2013

2018-09-21

*K. Fiebig*  
TÜV Rheinland Cert. Qualif.  
Am Gleisen Str. 51168 Köln

www.tuv.com Precisely Right.



## 7.2 Databook Reference

The following data references are available for this device:

1. Vishay Databook
2. Applications Notes
3. Internet homepage: <http://www.vishay.com>

### Reference Address

All enquiries relating to this document should be addressed to the following:

Vishay Semiconductor (Austria) Ges.m.b.H.  
Telefunkenstraße 5  
A-4840 Vöcklabruck / AUSTRIA  
Phone : + 43 7672 72451 0  
Fax : + 43 7672 72451 280

### Vishay

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## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 8. Locations

General Production Locations of the Division Small Signal Products

Location	Country	City	Assessment
Vishay Vöcklabruck	Austria	Vöcklabruck	IATF 16949 ISO 9001 ISO 14001
Vishay Budapest	Hungary	Budapest	IATF 16949 ISO 9001 ISO 14001
Vishay Heilbronn	Germany	Heilbronn	IATF 16949 ISO 9001 ISO 14001
Vishay Shanghai	China	Shanghai	IATF 16949 ISO 9001 ISO 14001
Vishay Tianjin	China	Tianjin	IATF 16949 ISO 9001 ISO 14001
Vishay Taipei	Taiwan	New Taipei City	IATF 16949 ISO 9001 ISO 14001
Subcon	China	Chuzhou	IATF 16949 ISO 9001 ISO 14001
Subcon	China	Suzhou	IATF 16949 ISO 9001 ISO 14001
Subcon	Korea	Iksan	IATF 16949 ISO 9001 ISO 14001
Subcon	China	Shanwei	IATF 16949 ISO 9001 ISO 14001
Subcon	China	Chengdu	IATF 16949 ISO 9001 ISO 14001
Subcon	China	Jinan	ISO 9001
Wafer Foundry	China	Hangzhou	IATF 16949 ISO 9001 ISO 14001



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## QualPack VTVS3V3ASMF-M to VTVS63GSMF-M

### 9. Revision history

Issue	Revision	Modification Notice	Applicable from
FEB-16	Revision 1	1 <sup>st</sup> Edition	February 2016
SEP-16	Revision 2	General Update	September 2016
JAN-20	Revision 3	General Update	January 2020