BCM® Bus Converter
BCM6123TD1E13A3TB1

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 125A continuous secondary output current
- Up to 2208W/in^3 power density
- 97.4% peak efficiency
- 4,242V_{DC} isolation
- Parallel operation for multi-kW arrays
- Primary input undervoltage and overvoltage, Secondary output overcurrent and shortcircuit and thermal protection
- 6123 through-hole ChiP™ package
  - 2.402 x 0.990 x 0.284" [61.00 x 25.14 x 7.21mm]
- PMBus™ management interface [b]

Typical Applications

- 380V_{DC} Power Distribution
- High-End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High-Density Power Supplies
- Communications Systems
- Transportation

Product Ratings	
V_{PRI} = 384V (260 – 410V) [a]	I_{SEC} = up to 125A
V_{SEC} = 12V (8.1 – 12.8V) [a] (NO LOAD)	K = 1/32

Product Description

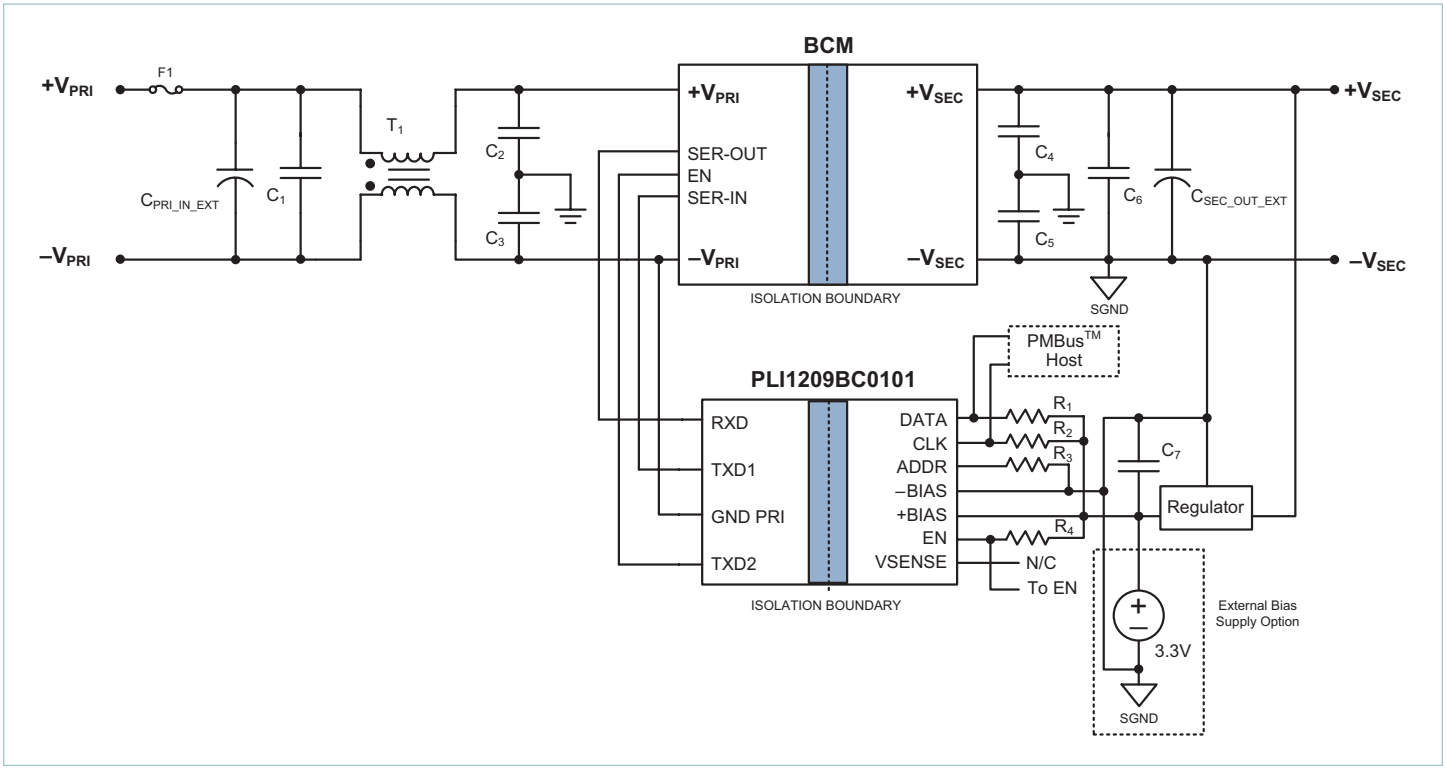
The BCM6123TD1E13A3TB1 is a high efficiency Bus Converter, operating from a 260 to 410V_{DC} [a] primary input bus to deliver an isolated, ratiometric secondary output voltage from 8.1 to 12.8V_{DC}.

The BCM6123TD1E13A3TB1 offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a PoL regulator to be located at the primary input side of the BCM. With a primary input to secondary output K factor of 1/32, that capacitance value can be reduced by a factor of 1024x, resulting in savings of board area, material and total system cost.

Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the BCM offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

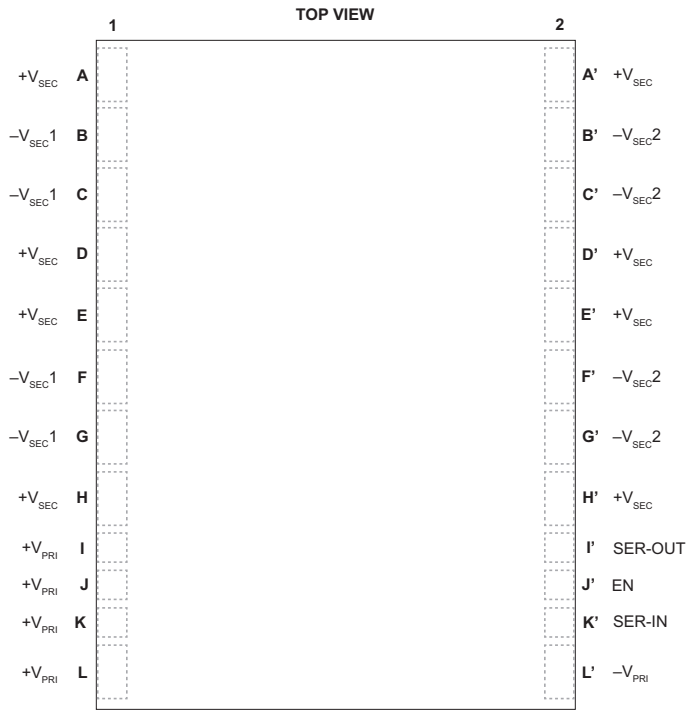
[a] Specified range when undervoltage lockout protections are disabled through PMBus, see page 5.
[b] When used with D44TL1A0 , or PLI1209BCxyzz.

Typical Application



BCM6123TD1E13A3TB1 at point-of-load with PLI1209BC0101 interface for PMBus communication

Pin Configuration



6123 ChiP™ Package

Pin Descriptions

Power Pins			
Pin Number	**Signal Name**	**Type**	**Function**
I1, J1, K1, L1	$+V_{PRI}$	PRIMARY INPUT POWER	Positive primary input transformer power terminal
L'2	$-V_{PRI}$	PRIMARY INPUT POWER RETURN	Negative primary input transformer power terminal
A1, D1, E1, H1, A'2, D'2, E'2, H'2	$+V_{SEC}$	SECONDARY OUTPUT POWER	Positive secondary output transformer power terminal
B1, C1, F1, G1 B'2, C'2, F'2, G'2	$-V_{SEC}$ [c]	SECONDARY OUTPUT POWER RETURN	Negative secondary output transformer power terminal
PMBus™ Control Signal Pins			
Pin Number	**Signal Name**	**Type**	**Function**
I'2	SER-OUT	OUTPUT	UART transmit pin; Primary input-side referenced signals
J'2	EN	INPUT	Enables and disables power supply; Primary input-side referenced signals
K'2	SER-IN	INPUT	UART receive pin; Primary input-side referenced signals

[c] For proper operation an external low impedance connection must be made between listed $-V_{SEC}1$ and $-V_{SEC}2$ terminals.

Part Ordering Information

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Output Voltage	Secondary Output Current	Temperature Grade	Option
BCM	6123	T	D1	E	13	A3	T	B1
Bus Converter Module	61 = L 23 = W	**T** = TH	410V	260 – 410V	13V No Load	125A	**T** = –40 to 125°C	**B1** = PMBus™ Ctrl

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
$+V_{PRI\_DC}$ to $-V_{PRI\_DC}$		–1	480	V
V_{PRI_DC} Slew Rate	Operational		1	V/µs
$+V_{SEC\_DC}$ to $-V_{SEC\_DC}$		–1	15	V
SER-OUT to $-V_{PRI\_DC}$		–0.3	4.6	V
EN to $-V_{PRI\_DC}$			5.5	V
SER-IN to $-V_{PRI\_DC}$			4.6	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specifications						
Primary Input Voltage Range, Continuous	V_{PRI_DC}	Supervisory input undervoltage lockout protections disabled through PMBus™ (DISABLE_FAULT, see p. 10)	**260**		**410**	V
		Supervisory input undervoltage lockout protections enabled (default)	**365**		**410**	
V_{PRI} µController	$V_{\mu C\_ACTIVE}$	V_{PRI_DC} voltage where µC is initialized			130	V
Primary Input Quiescent Current	I_{PRI_Q}	Disabled, EN Low, V_{PRI_DC} = 384V		2		mA
		$T_{INTERNAL}$ ≤ 100°C			4	
Primary Input No Load Power Dissipation	P_{PRI_NL}	V_{PRI_DC} = 384V, $T_{INTERNAL}$ = 25°C		11	17	W
		V_{PRI_DC} = 384V	**5.9**		**25**	
		V_{PRI_DC} = 260 – 410V, $T_{INTERNAL}$ = 25°C			19	
		V_{PRI_DC} = 260 – 410V			**27**	
Primary Input Inrush Current Peak	$I_{PRI\_INR\_PK}$	Enable start up, V_{PRI_DC} = 384V, C_{SEC_EXT} = 0uF, no load			5	A
		V_{PRI_DC} = 410V, C_{SEC_EXT} = 1000µF, R_{LOAD_SEC} = 50% of full load current		10		
		$T_{INTERNAL}$ ≤ 100°C			15	
Secondary Output Voltage Rise Time	t_{SEC_RISE}	Enable start up, V_{PRI_DC} = 384V, C_{SEC_EXT} = 0µF, no load		38.5		µs
DC Primary Input Current	$I_{PRI\_IN\_DC}$	At $I_{SEC\_OUT\_DC}$ = 125A, $T_{INTERNAL}$ ≤ 100°C			4.1	A
Transformation Ratio	K	Primary input to secondary output, K = V_{SEC_DC} / V_{PRI_DC}, at no load		1/32		V/V
Secondary Output Current (Continuous)	$I_{SEC\_OUT\_DC}$				125	A
Secondary Output Current (Pulsed)	$I_{SEC\_OUT\_PULSE}$	10ms pulse, 25% duty cycle, $I_{SEC\_OUT\_AVG}$ ≤ 50% rated $I_{SEC\_OUT\_DC}$			167	A
Secondary Output Power (Continuous)	$P_{SEC\_OUT\_DC}$	Specified at V_{PRI_DC} = 410V			1500	W
Secondary Output Power (Pulsed)	$P_{SEC\_OUT\_PULSE}$	Specified at V_{PRI_DC} = 410V; 10ms pulse, 25% duty cycle, P_{SEC_AVG} ≤ 50% rated $P_{SEC\_OUT\_DC}$			2000	W
Efficiency (Ambient)	η_{AMB}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 125A	96.2	97		%
		V_{PRI_DC} = 260 – 410V, $I_{SEC\_OUT\_DC}$ = 125A	95.2			
		V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 62.5A	96.5	97.4		
Efficiency (Hot)	η_{HOT}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 125A	95.8	97		%
Efficiency (Over Load Range)	$\eta_{20\%}$	25A < $I_{SEC\_OUT\_DC}$ < 125A	**90**			%
Secondary Output Resistance	R_{SEC_COLD}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 125A, $T_{INTERNAL}$ = –40°C	1.10	1.50	1.80	mΩ
	R_{SEC_AMB}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 125A	1.50	1.85	2.30	
	R_{SEC_HOT}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 125A, $T_{INTERNAL}$ = 100°C	2.2	2.45	2.70	
Switching Frequency	F_{SW}	Frequency of the output voltage ripple = 2x F_{SW}	**0.95**	1.00	**1.05**	MHz
Secondary Output Voltage Ripple	$V_{SEC\_OUT\_PP}$	C_{SEC_EXT} = 0µF, $I_{SEC\_OUT\_DC}$ = 125A, V_{PRI_DC} = 384V, 20MHz BW		195		mV
		$T_{INTERNAL}$ ≤ 100°C			250	
Primary Input Leads Inductance (Parasitic)	$L_{PRI\_IN\_LEADS}$	Frequency 2.5MHz (double switching frequency), simulated lead model		7		nH
Secondary Output Leads Inductance (Parasitic)	$L_{SEC\_OUT\_LEADS}$	Frequency 2.5MHz (double switching frequency), simulated lead model		0.64		nH
Primary Input Series Inductance (Internal)	L_{IN_INT}	Reduces the need for input decoupling inductance in BCM arrays		0.56		µH

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specifications (Cont.)						
Effective Primary Input Capacitance (Internal)	C_{PRI_INT}	Effective Value at 384V_{PRI_DC}		0.37		µF
Effective Secondary Output Capacitance (Internal)	C_{SEC_INT}	Effective Value at 12V_{SEC_DC}		208		µF
Rated Secondary Output Capacitance (External)	$C_{SEC\_OUT\_EXT}$	Excessive capacitance may prevent module start up			**1000**	µF
Rated Secondary Output Capacitance (External), Parallel Array Operation	$C_{SEC\_OUT\_AEXT}$	$C_{SEC\_OUT\_AEXT}$ Max = N • 0.5 • $C_{SEC\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Protections						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given V_{PRI_DC} > V_{PRI_UVLO+}	**292.5**		**357.5**	ms
Primary Input Overvoltage Lockout Threshold	V_{PRI_OVLO+}		**420**	434.5	**450**	V
Primary Input Overvoltage Recovery Threshold	$V_{PRI\_OVLO–}$		**410**	424	**440**	V
Primary Input Overvoltage Lockout Hysteresis	$V_{PRI\_OVLO\_HYST}$			10.5		V
Primary Input Overvoltage Lockout Response Time	t_{PRI_OVLO}			100		µs
Secondary Output Soft-Start Ramp Time	$t_{SEC\_SOFT\text{-}START}$	From powertrain active. Fast current limit protection disabled during soft start		1		ms
Secondary Output Overcurrent Trip Threshold	$I_{SEC\_OUT\_OCP}$		**145**	170	**210**	A
Secondary Output Overcurrent Response Time Constant	$t_{SEC\_OUT\_OCP}$	Effective internal RC filter		3		ms
Secondary Output Short Circuit Protection Trip Threshold	$I_{SEC\_OUT\_SCP}$		**187**			A
Secondary Output Short Circuit Protection Response Time	$t_{SEC\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits						
Primary Input Overvoltage Lockout Threshold	V_{PRI_OVLO+}		**420**	434.5	**450**	V
Primary Input Overvoltage Recovery Threshold	$V_{PRI\_OVLO–}$		**410**	424	**440**	V
Primary Input Overvoltage Lockout Hysteresis	$V_{PRI\_OVLO\_HYST}$			10.5		V
Primary Input Overvoltage Lockout Response Time	t_{PRI_OVLO}			100		µs
Primary Input Undervoltage Lockout Threshold	$V_{PRI\_UVLO–}$	Supervisory input undervoltage lockout protections disabled through PMBus™ (DISABLE_FAULT, see p. 10)	**104**	122	**140**	V
		Supervisory input undervoltage lockout protections enabled (default)	**285**	320	**355**	
Primary Input Undervoltage Recovery Threshold	V_{PRI_UVLO+}	Supervisory input undervoltage lockout protections disabled through PMBus (DISABLE_FAULT, see p. 10)	**114**	132	**150**	V
		Supervisory input undervoltage lockout protections enabled (default)	**325**	350	**360**	
Primary Input Undervoltage Lockout Hysteresis	$V_{PRI\_UVLO\_HYST}$	Supervisory input undervoltage lockout protections disabled through PMBus (DISABLE_FAULT, see p. 10)		10		V
		Supervisory input undervoltage lockout protections enabled (default)		30		
Primary Input Undervoltage Lockout Response Time	t_{PRI_UVLO}			100		µs
Primary Input to Secondary Output Start-Up Delay	$t_{PRI\_TO\_SEC\_DELAY}$	From V_{PRI_DC} = V_{PRI_UVLO+} to powertrain active, EN floating (i.e., one-time start-up delay from application of V_{PRI_DC} to V_{SEC_DC})		20		ms
Secondary Output Overcurrent Trip Threshold	$I_{SEC\_OUT\_OCP}$		**145**	170	**210**	A
Secondary Output Overcurrent Response Time Constant	$t_{SEC\_OUT\_OCP}$	Effective internal RC filter		3		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$		105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC; Protection not available for M-Grade units.			–45	°C
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Start up into a persistent fault condition. Non-Latching fault detection given V_{PRI_DC} > V_{PRI_UVLO+}		3		s

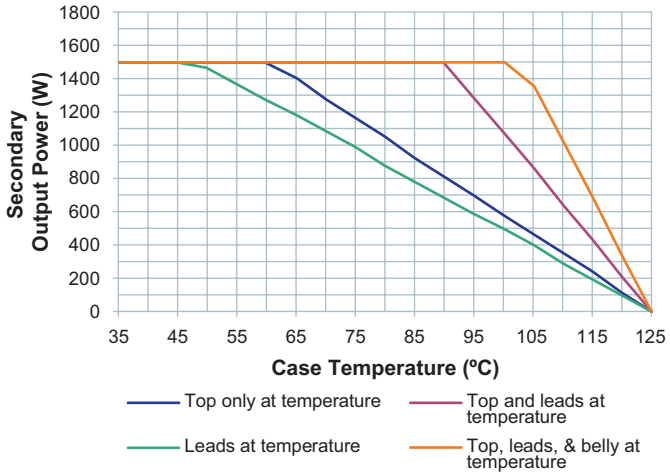


Figure 1 — *Specified thermal operating area*

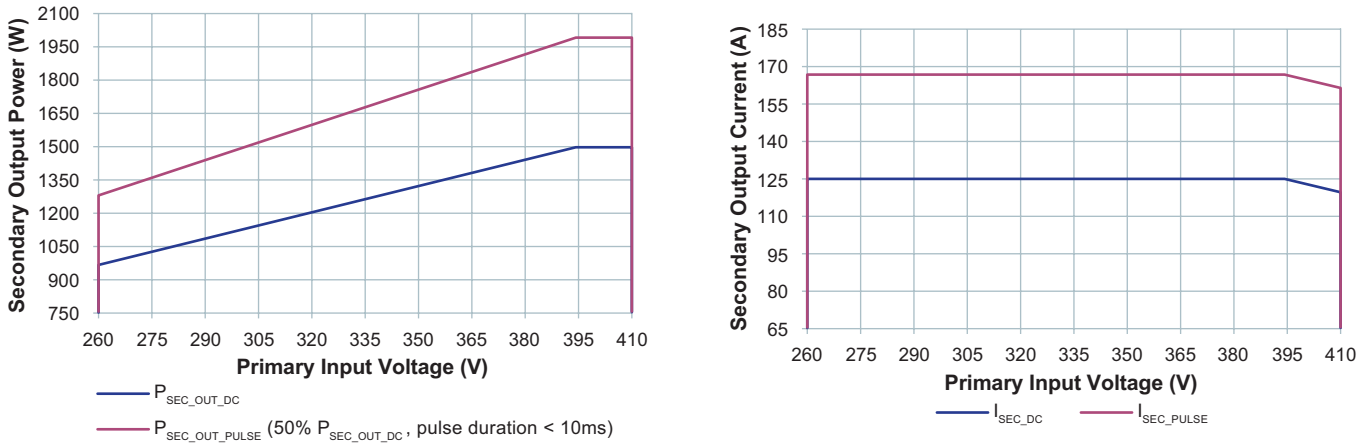


Figure 2 — *Specified electrical operating area using rated R_{SEC_HOT}*

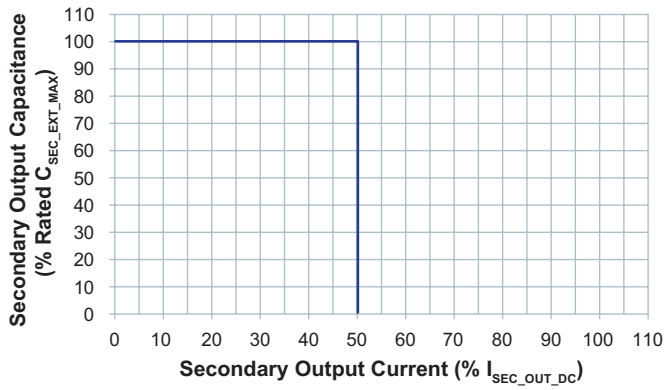


Figure 3 — *Specified primary input and enable start up into load current and external capacitance*

PMBus™ Control Signal Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

UART SER-IN / SER-OUT Pins

- Universal Asynchronous Receiver/Transmitter (UART) pins.
- The BCM communication version is not intended to be used without a Digital Supervisor or Point-of-Load Isolator.
- Isolated I^2C communication and telemetry is available when using Vicor Digital Isolator and Vicor Digital Supervisor or Point-of-Load Isolator. Please see specific product data sheet for more details.
- UART SER-IN pin is internally pulled high using a 1.5kΩ to 3.3V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
GENERAL I/O	Regular Operation	Baud Rate	BR_{UART}	Rate		**750**		Kbit/s
DIGITAL INPUT		**SER-IN Pin**						
		SER-IN Input Voltage Range	V_{SER-IN_IH}		2.3			V
			V_{SER-IN_IL}				1	V
		SER-IN Rise Time	t_{SER-IN_RISE}	10 – 90%		400		ns
		SER-IN Fall Time	t_{SER-IN_FALL}	10 – 90%		25		ns
		SER-IN R_{PULLUP}	R_{SER-IN_PLP}	Pull up to 3.3V		1.5		kΩ
		SER-IN External Capacitance	C_{SER-IN_EXT}				400	pF
DIGITAL OUTPUT		**SER-OUT Pin**						
		SER-OUT Output Voltage Range	$V_{SER-OUT\_OH}$	0mA ≥ I_{OH} ≥ –4mA	2.8			V
			$V_{SER-OUT\_OL}$	0mA ≤ I_{OL} ≤ 4mA			0.5	V
		SER-OUT Rise Time	$t_{SER-OUT\_RISE}$	10 – 90%		55		ns
		SER-OUT Fall Time	$t_{SER-OUT\_FALL}$	10 – 90%		45		ns
		SER-OUT Source Current	$I_{SER-OUT}$	$V_{SER-OUT}$ = 2.8V			6	mA
		SER-OUT Output Impedance	$Z_{SER-OUT}$			**120**		Ω

Enable / Disable Control

- The EN pin is a standard analog I/O configured as an input to an internal µC.
- It is internally pulled high to 3.3V.
- When held low, the BCM internal bias will be disabled and the powertrain will be inactive.
- In an array of BCMs, EN pins should be interconnected to synchronize start up.
- PMBus ON/OFF command has no effect if the BCM EN pin is not in the active state. This BCM has active high EN pin logic.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Start Up	EN to Powertrain Active Time	t_{EN_START}	V_{PRI_DC} > V_{PRI_UVLO+}, EN held low both conditions satisfied for t > $t_{PRI\_UVLO+\_DELAY}$		**250**		µs
	Regular Operation	EN Voltage Threshold	V_{ENABLE}		**2.3**			V
		EN Resistance (Internal)	R_{EN_INT}	Internal pull-up resistor		1.5		kΩ
		EN Disable Threshold	$V_{EN\_DISABLE\_TH}$				1	V

PMBus™ Reported Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Monitored Telemetry

- The BCM communication version is not intended to be used without a Digital Supervisor or Point-of-Load Isolator.
- The current telemetry is only available in forward operation. The input and output current reported value is not supported in reverse operation.

Attribute	Digital Supervisor / PLI PMBus™ READ Command	Accuracy (Rated Range)	Functional Reporting Range	Update Rate	Reported Units
Input Voltage	(88h) READ_VIN	±5% (LL – HL)	130 – 450V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Input Current	(89h) READ_IIN	±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	0 – 5.9A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-3}$
Output Voltage [d]	(8Bh) READ_VOUT	±5% (LL – HL)	4.25 – 14V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Output Current	(8Ch) READ_IOUT	±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	0 – 190A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
Output Resistance	(D4h) READ_ROUT	±5% (50 – 100% of FL) at NL ±10% (50 – 100% of FL) (LL – HL)	1 – 3mΩ	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature [e]	(8Dh) READ_TEMPERATURE_1	±7°C (Full Range)	–55 to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[d] Default READ Output Voltage returned when unit is disabled = –300V.
[e] Default READ Temperature returned when unit is disabled = –273°C.

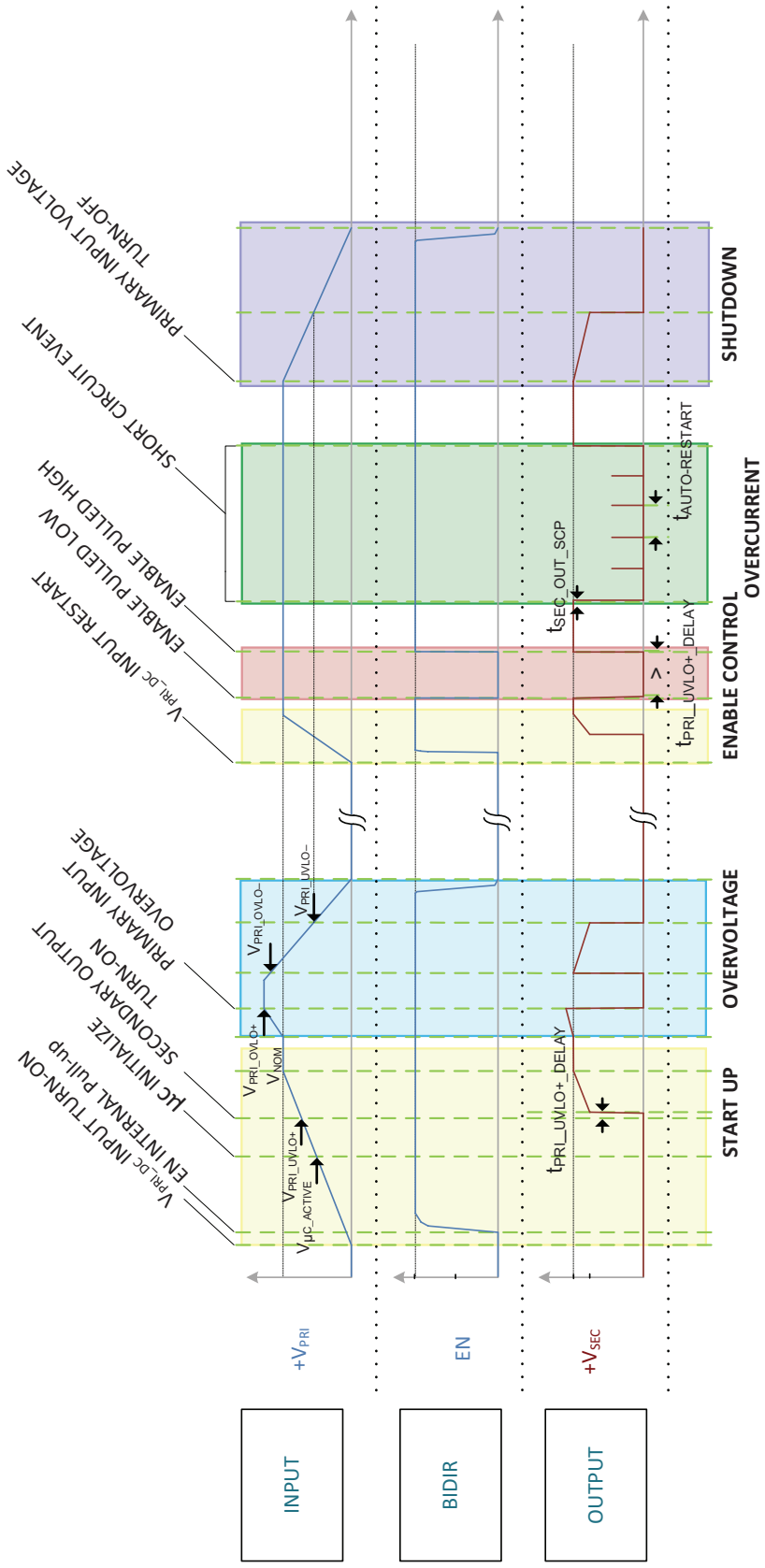
Variable Parameter

- Factory setting of all below Thresholds and Warning limits are 100% of listed protection values.
- Variables can be written only when module is disabled either EN pulled low or $V_{IN} < V_{IN\_UVLO–}$.
- Module must remain in a disabled mode for 3ms after any changes to the below variables allowing ample time to commit changes to EEPROM.

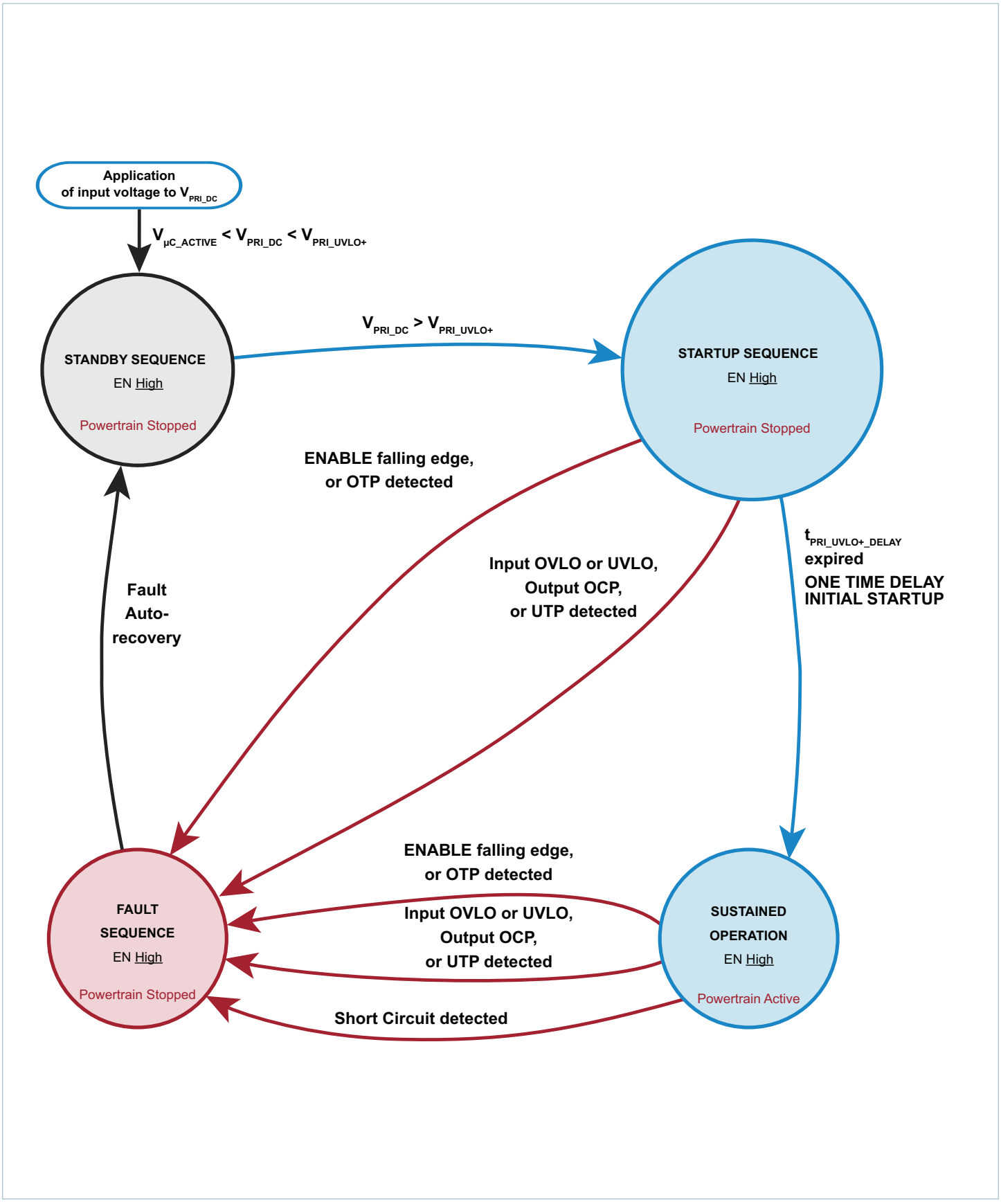
Attribute	Digital Supervisor / PLI PMBus™ Command [f]	Conditions / Notes	Accuracy (Rated Range)	Functional Reporting Range	Default Value
Input / Output Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	$V_{IN\_OVLO–}$ is automatically 3% lower than this set point	±5% (LL – HL)	130 – 435V	100%
Input / Output Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		±5% (LL – HL)	130 – 435V	100%
Input / Output Undervoltage Protection Limit	(D7h) DISABLE_FAULT	Can only be disabled to a preset default value	±5% (LL – HL)	130 or 365V	100%
Input Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	0 – 5.25A	100%
Input Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	0 – 5.25A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT		±7°C (Full Range)	0 – 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT		±7°C (Full Range)	0 – 125°C	100%
Turn-On Delay	(60h) TON_DELAY	Additional time delay to the primary input to secondary output start-up delay	±50µs	0 – 100ms	0ms

[f] Refer to Digital Supervisor or PLI1209BCxyzz datasheet for complete list of supported commands.

BCM Timing Diagram



High-Level Functional State Diagram



Application Characteristics

Temperature controlled via top side cold plate, unless otherwise noted. See associated figures for general trend data.

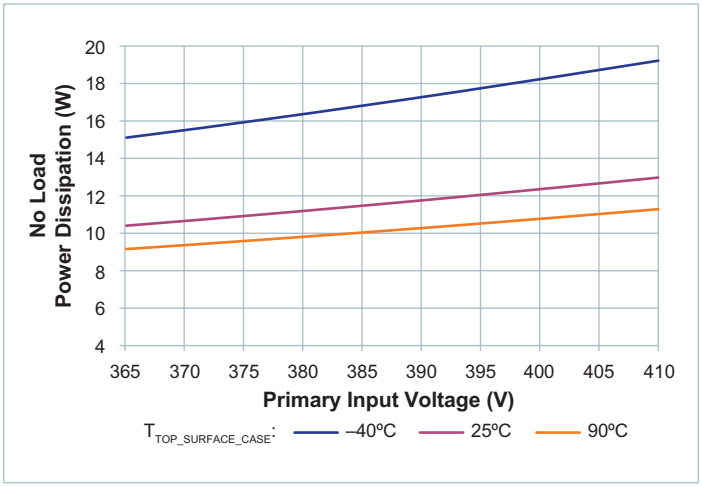


Figure 4 — *No load power dissipation vs. V_{PRI_DC}*

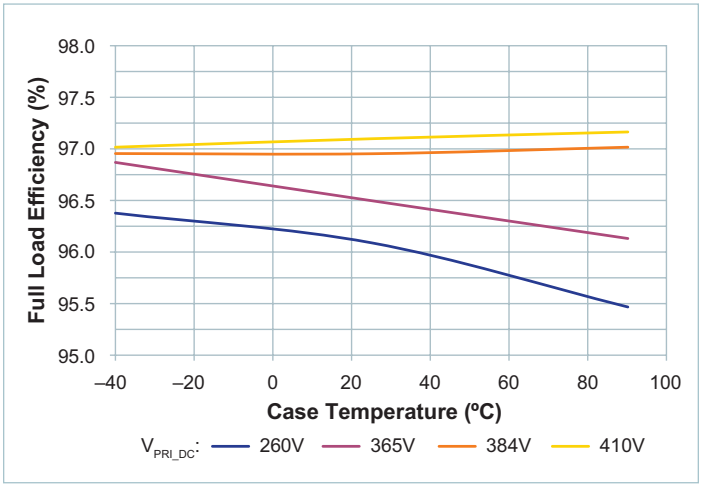


Figure 5 — *Full load efficiency vs. temperature; V_{PRI_DC}*

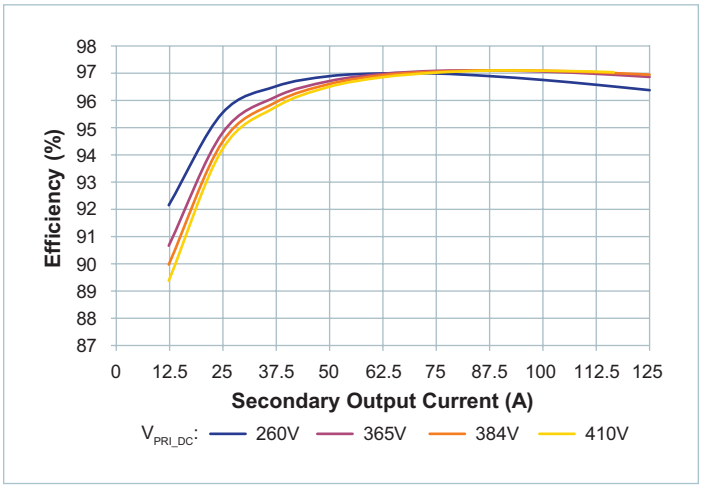


Figure 6 — *Efficiency at T_{CASE} = –40°C*

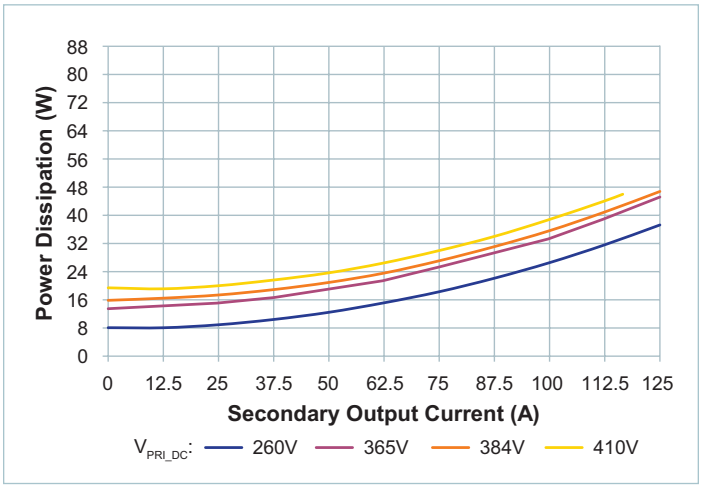


Figure 7 — *Power dissipation at T_{CASE} = –40°C*

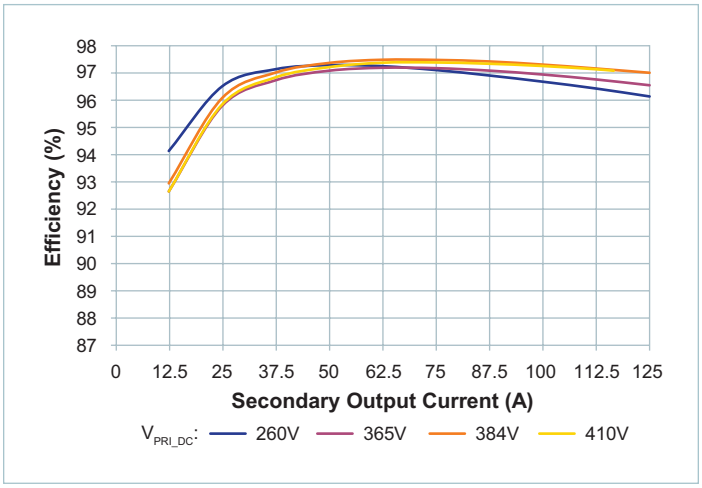


Figure 8 — *Efficiency at T_{CASE} = 25°C*

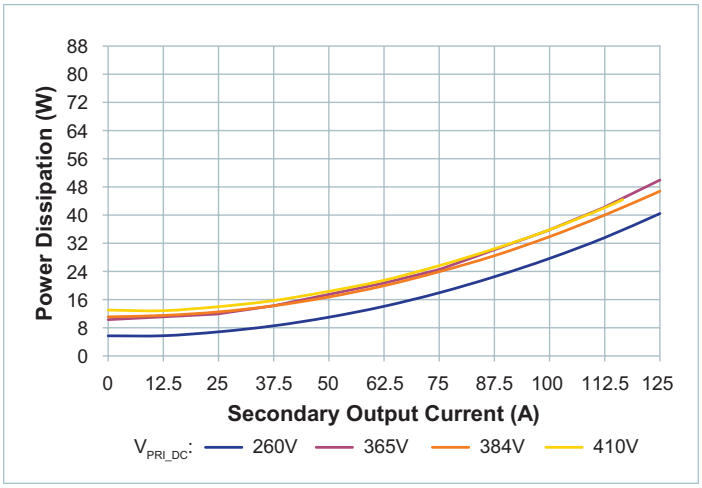


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. See associated figures for general trend data.

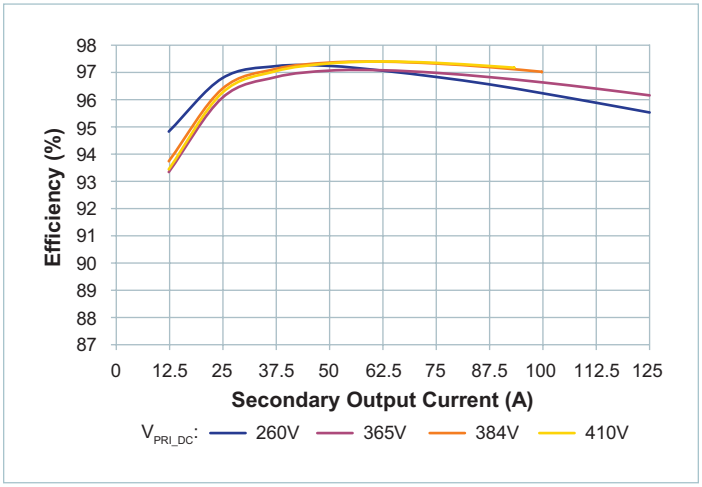


Figure 10 — *Efficiency at T_{CASE} = 90°C*

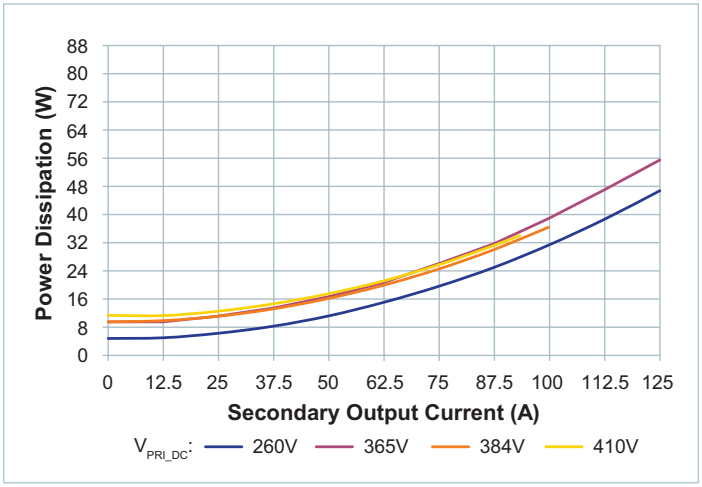


Figure 11 — *Power dissipation at T_{CASE} = 90°C*

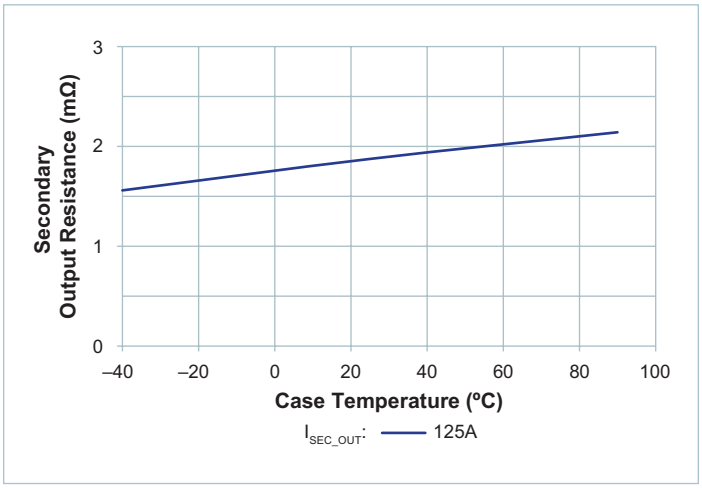


Figure 12 — *R_{SEC} vs. temperature; nominal V_{PRI_DC} I_{SEC_DC} = 100A at T_{CASE} = 90°C*

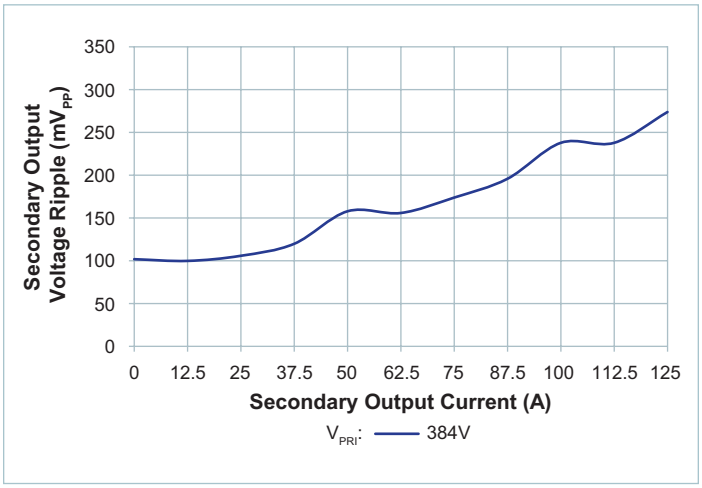


Figure 13 — *$V_{SEC\_OUT\_PP}$ vs. I_{SEC_DC}; no external $C_{SEC\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

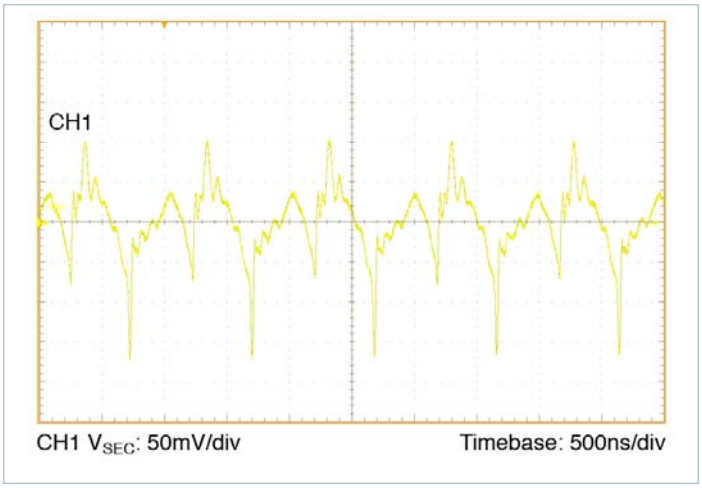


Figure 14 — *Full load secondary output voltage ripple, 10µF $C_{PRI\_IN\_EXT}$; no external $C_{SEC\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

Application Characteristics (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. See associated figures for general trend data.

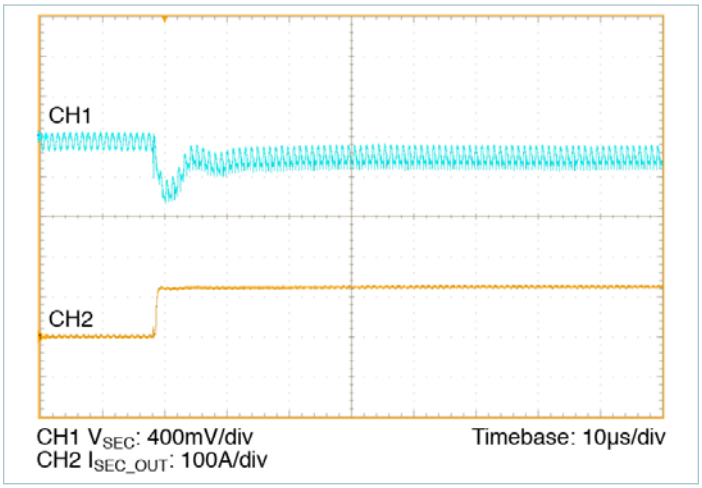


Figure 15 — *0 – 125A transient response: $C_{PRI\_IN\_EXT}$ = 10µF, no external $C_{SEC\_OUT\_EXT}$*

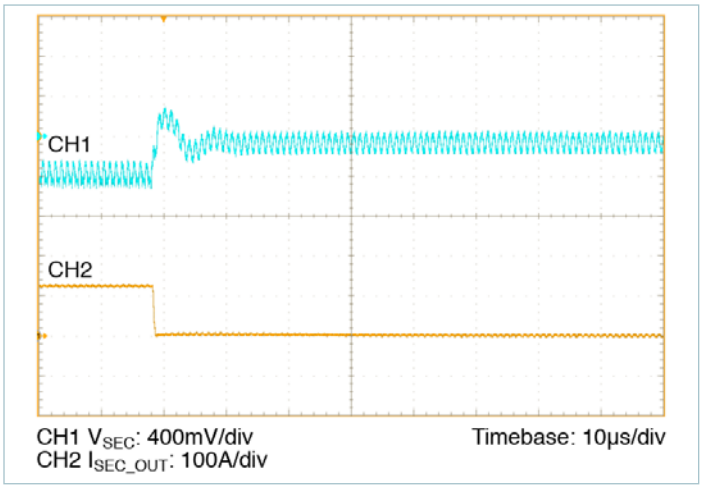


Figure 16 — *125 – 0A transient response: $C_{PRI\_IN\_EXT}$ = 10µF, no external $C_{SEC\_OUT\_EXT}$*

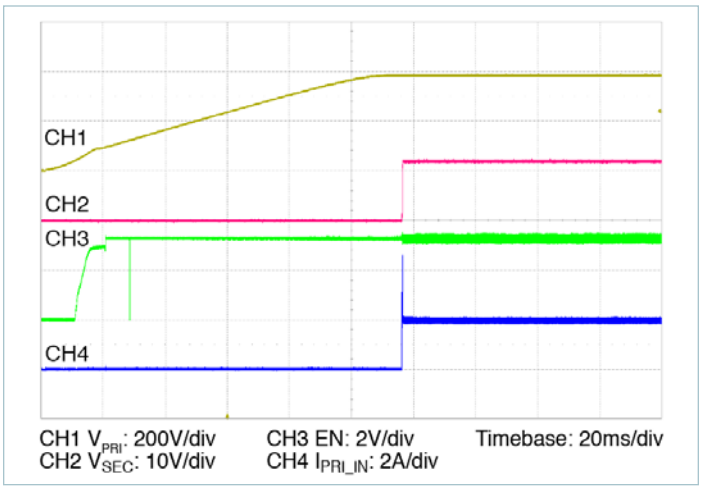


Figure 17 — *Start up from application of V_{PRI_DC} = 384V, 50% $I_{SEC\_OUT\_DC}$, 100% $C_{SEC\_OUT\_EXT}$*

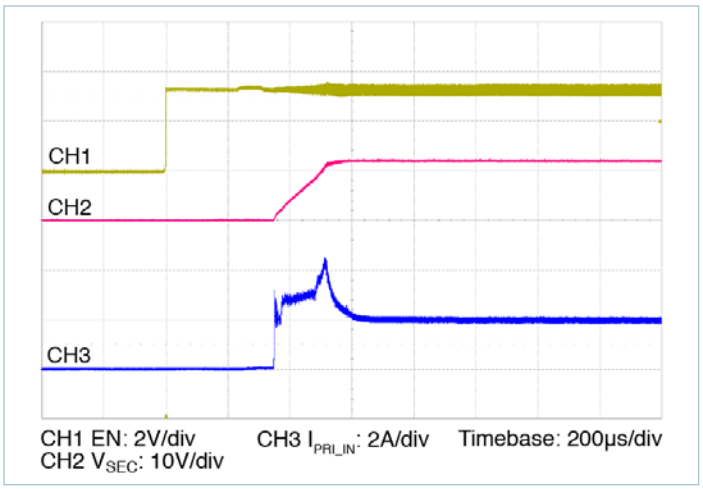


Figure 18 — *Start up from application of EN with pre-applied V_{PRI_DC} = 384V, 50% $I_{SEC\_OUT\_DC}$, 100% $C_{SEC\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		60.87 [2.396]	61.00 [2.402]	61.13 [2.407]	mm [in]
Width	W		24.76 [0.975]	25.14 [0.990]	25.52 [1.005]	mm [in]
Height	H		7.11 [0.280]	7.21 [0.284]	7.31 [0.288]	mm [in]
Volume	Vol	Without heatsink		11.06 [0.675]		cm^3 [in^3]
Weight	W			41 [1.45]		g [oz]
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating Temperature	$T_{INTERNAL}$	BCM6123TD1E13A3TB1 (T-Grade)	–40		125	°C
Thermal Resistance Top Side	$\theta_{INT-TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.14		°C/W
Thermal Resistance Leads	$\theta_{INT-LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		1.35		°C/W
Thermal Resistance Bottom Side	$\theta_{INT-BOTTOM}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.07		°C/W
Thermal Capacity				34		Ws/°C
Assembly						
Storage Temperature		BCM6123TD1E13A3TB1 (T-Grade)	–55		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to <2kV)				
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to <500V)				

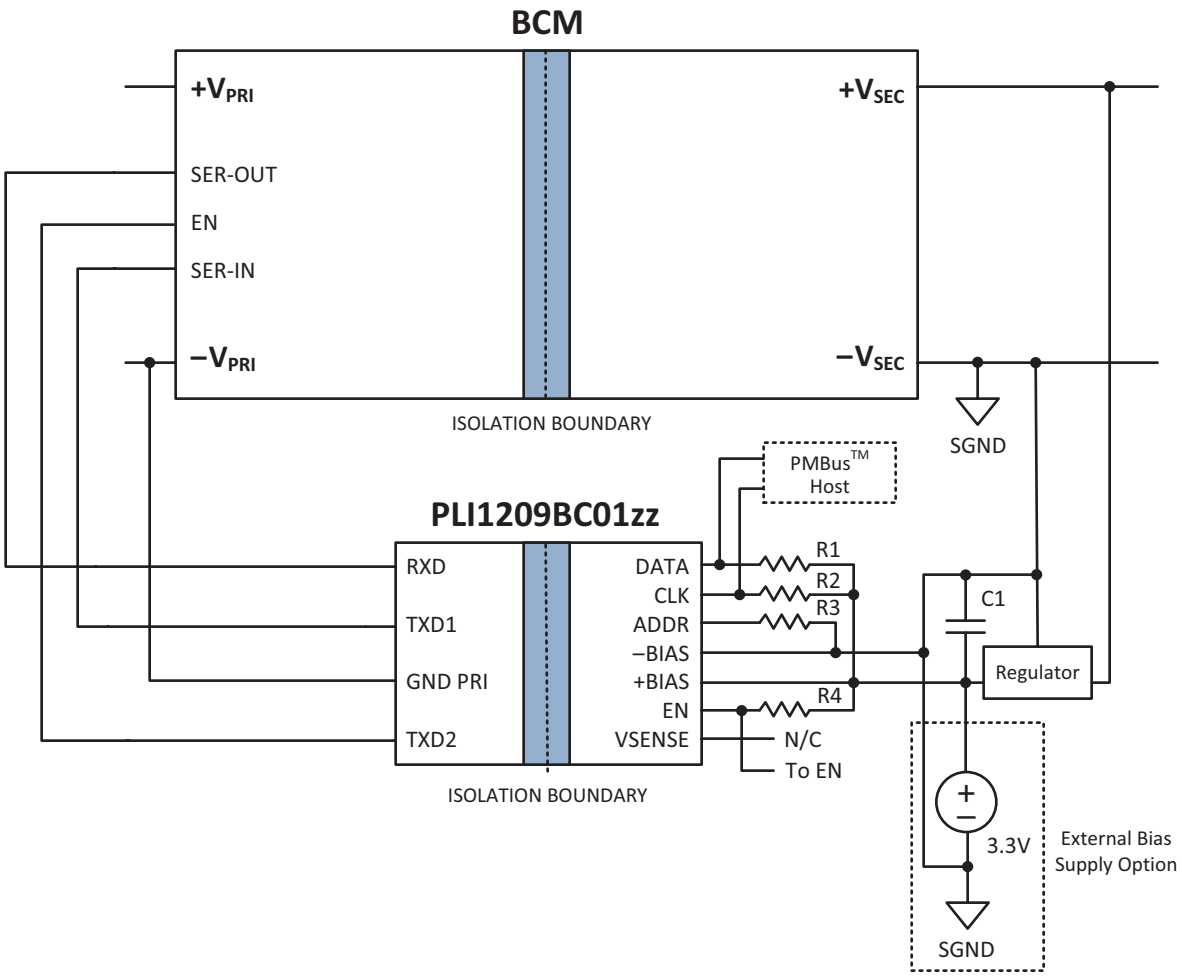
General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Soldering [f]						
Peak Temperature Top Case					135	°C
Safety						
Isolation voltage / Dielectric test	V_{HIPOT}	PRIMARY INPUT to SECONDARY OUTPUT	**4,242**			V_{DC}
		PRIMARY INPUT to CASE	**2,121**			
		SECONDARY OUTPUT to CASE	**2,121**			
Isolation Capacitance	C_{PRI_SEC}	Unpowered Unit	**620**	780	**940**	pF
Insulation Resistance	R_{PRI_SEC}	At 500V_{DC}	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.31		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.41		MHrs
Agency Approvals / Standards		cTÜVus EN 60950-1				
		cURus UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

[f] Product is not intended for reflow solder attach.

PMBus™ System Diagram



The PMBus communication enabled bus converter provides accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags.

The BCM internal µC is referenced to primary input-side ground. The PLI1209BCxyzz UART interface operates at a typical speed of 750kHz across the isolation barrier.

The PLI provides the host system µC with access to a single BCM. This BCM is constantly polled for status by the PLI. Direct communication to the individual BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the PLI data and page (0x01) prior to a telemetry inquiry points to the connected BCM data. The PLI constantly polls the BCM data through the UART interface.

The PLI enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The PLI follows the PMBus command structure and specification.

Please refer to the PLI1209BCxyzz data sheet for more details.

BCM in a ChiP™

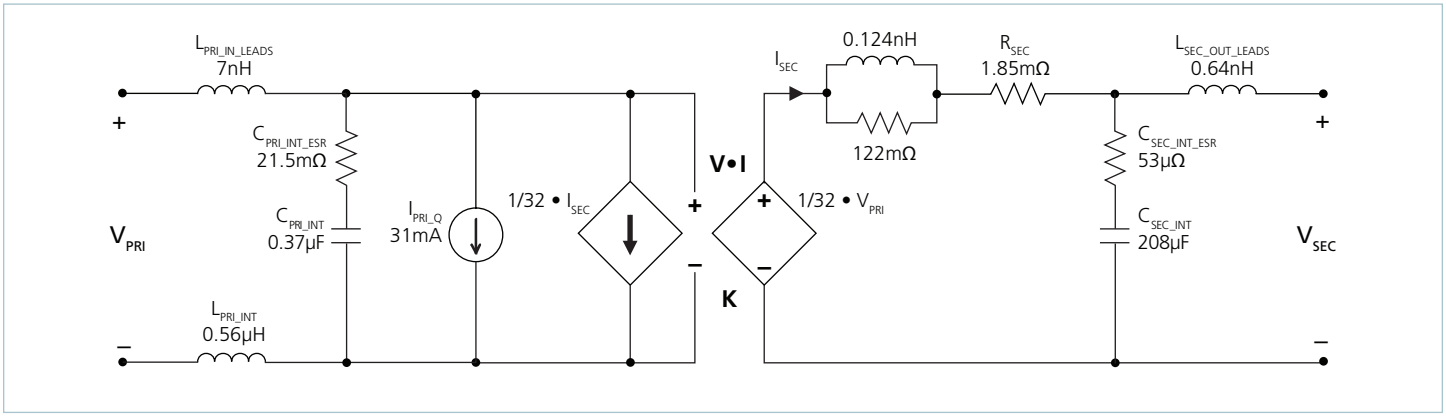


Figure 19 — *BCM AC model*

The BCM uses a high frequency resonant tank to move energy from primary input to secondary output and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the primary input voltage and the secondary output current. A small amount of capacitance embedded in the primary input-side and secondary output-side stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM6123TD1E13A3TB1 can be simplified into the model shown in Figure 19.

$$V_{SEC} = V_{PRI} \bullet K \qquad (1)$$

At no load:

$$K = \frac{V_{SEC}}{V_{PRI}} \qquad (2)$$

K represents the "turns ratio" of the BCM.
Rearranging Eq (1):

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC} \qquad (3)$$

In the presence of a load, V_{SEC} is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_{PRI\_Q}}{K} \qquad (4)$$

and I_{SEC} is represented by:

R_{SEC} represents the impedance of the BCM, and is a function of the R_{DS_ON} of the primary input and secondary output MOSFETs and the winding resistance of the power transformer. I_{PRI_Q} represents the quiescent current of the BCM controller, gate drive circuitry and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that R_{SEC} = 0Ω and I_{PRI_Q} = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{PRI}.

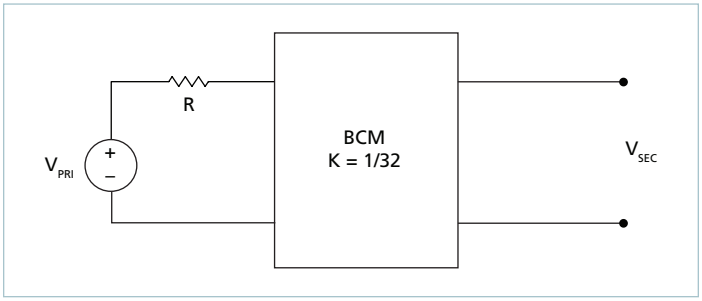


Figure 20 — *K = 1/32 BCM with series primary input-side resistor*

The relationship between V_{PRI} and V_{SEC} becomes:

$$V_{SEC} = \left(V_{PRI} - I_{PRI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_{PRI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{SEC} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R, on the primary input side of the BCM is effectively scaled by K^2 with respect to the secondary output side.

Assuming that R = 1Ω, the effective R as seen from the secondary output side is 0.98mΩ, with K = 1/32.

A similar exercise can be performed with the additon of a capacitor or shunt impedance at the primary input side of the BCM. A switch in series with V_{PRI} is added to the circuit. This is depicted in Figure 21.

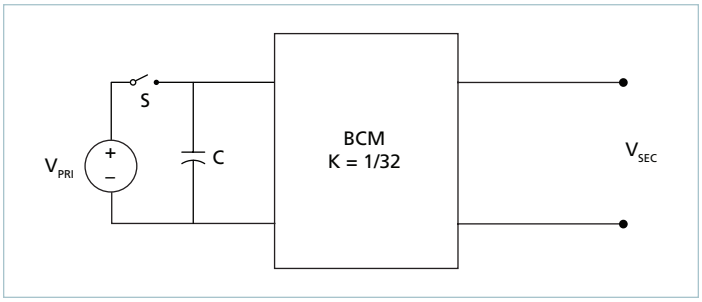


Figure 21 — *BCM with primary input-side capacitor*

A change in V_{PRI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\,\frac{dV_{PRI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{PRI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{SEC} \bullet K \qquad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{SEC}(t) = \frac{C}{K^2} \bullet \frac{dV_{SEC}}{dt} \qquad (9)$$

The equation in terms of the secondary output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the secondary output side when expressed in terms of the primary input side. With K = 1/32 as shown in Figure 21, C = 1µF would appear as C = 1024µF when viewed from the secondary output side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM are:

- No load power dissipation (P_{PRI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{SEC}}$): refers to the power loss across the BCM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{PRI\_NL} + P_{R_{SEC}} \qquad (10)$$

Therefore,

$$P_{SEC\_OUT} = P_{PRI\_IN} - P_{DISSIPATED} = P_{PRI\_IN} - P_{PRI\_NL} - P_{R_{SEC}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{SEC\_OUT}}{P_{PRI\_IN}} = \frac{P_{PRI\_IN} - P_{PRI\_NL} - P_{R_{SEC}}}{P_{PRI\_IN}} \qquad (12)$$

$$= \frac{V_{PRI} \bullet I_{PRI} - P_{PRI\_NL} - (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}$$

$$= 1 - \left(\frac{P_{PRI\_NL} + (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}\right)$$

Input and Output Filter Design

A major advantage of BCM systems versus conventional PWM converters is that the transformer based BCM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of primary input voltage and secondary output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the primary input-side and secondary output-side stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the BCM's dynamic response, the impedance presented to its primary input terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- *Further reduce primary input and/or secondary output voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the primary input source will appear at the secondary output of the module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:*

  The module primary input voltage range shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal primary input operating range. Even when disabled, the powertrain is exposed to the applied voltage and the power MOSFETs must withstand it.

Total load capacitance at the secondary output of the BCM shall not exceed the specified maximum. Owing to the wide bandwidth and low secondary output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the primary input of the module. At frequencies <500kHz the module appears as an impedance of R_{SEC} between the source and load.

Within this frequency range, capacitance at the primary input appears as effective capacitance on the secondary output per the relationship

$$C_{SEC\_EXT} = \frac{C_{PRI\_EXT}}{K^2} \qquad (13)$$

defined in Equation 13.

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The ChiP™ provides a high degree of flexibility in that it presents three pathways to remove heat from the internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component in determining the maximum current that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for a 6123 ChiP BCM in an application where the top, bottom, and leads are cooled. In this case, the BCM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation provide an estimate of heat flow through the various dissipation pathways as well as internal temperature.

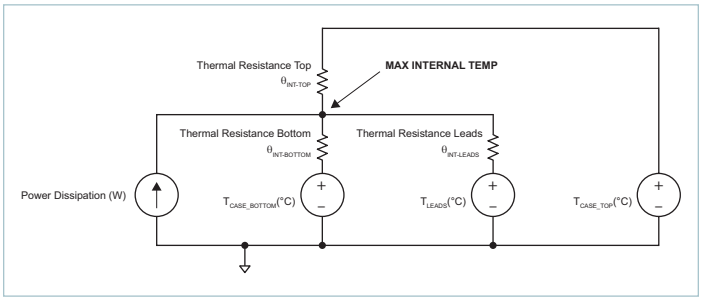


Figure 22 — *Top case, Bottom case and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$T_{INT} - PD_2 \bullet \theta_{INT\text{-}BOTTOM} = T_{CASE\_BOTTOM}$$

$$T_{INT} - PD_3 \bullet \theta_{INT\text{-}LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where T_{INT} represents the internal temperature and PD_1, PD_2, and PD_3 represent the heat flow through the top side, bottom side, and leads, respectively.

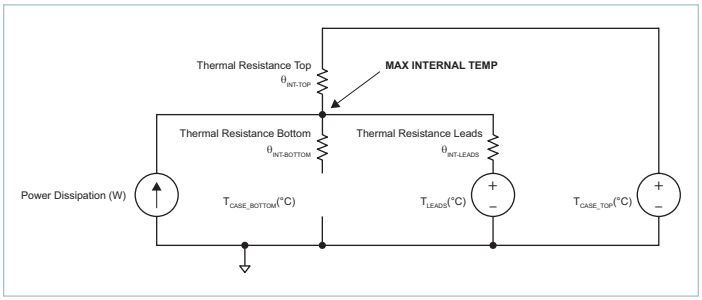


Figure 23 — *Top case and leads thermal model*

Figure 23 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$T_{INT} - PD_3 \bullet \theta_{INT\text{-}LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_3$$

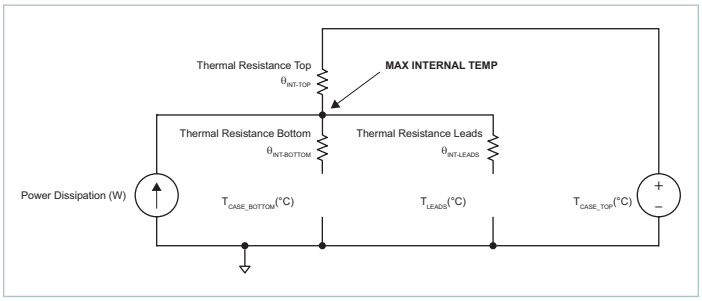


Figure 24 — *Top case thermal model*

Figure 24 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow paths to the bottom and leads are left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$PD_{TOTAL} = PD_1$$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator that greatly simplify the task of determining whether or not a BCM thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench..

Current Sharing

The performance of the BCM topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCMs of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- A dedicated input filter for each BCM in an array is required to prevent circulating currents.

For further details see:
AN:016 Using BCM Bus Converters in High Power Arrays.

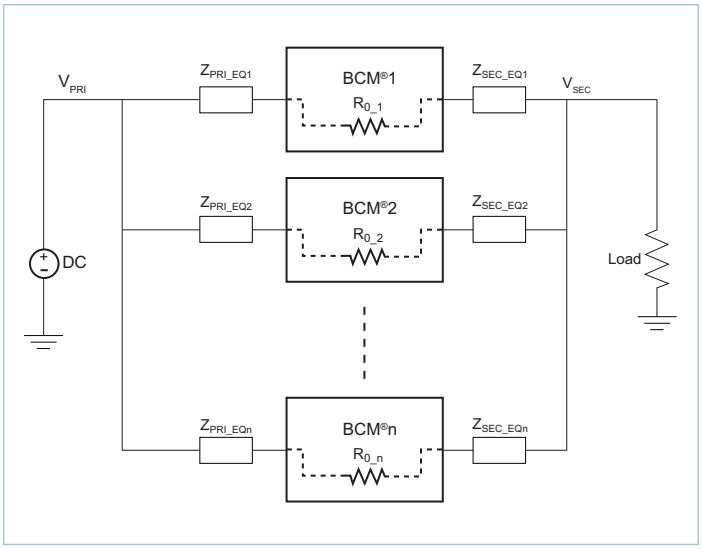


Figure 25 — *BCM array*

Fuse Selection

In order to provide flexibility in configuring power systems, ChiP modules are not internally fused. Input line fusing of ChiP products is recommended at a system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

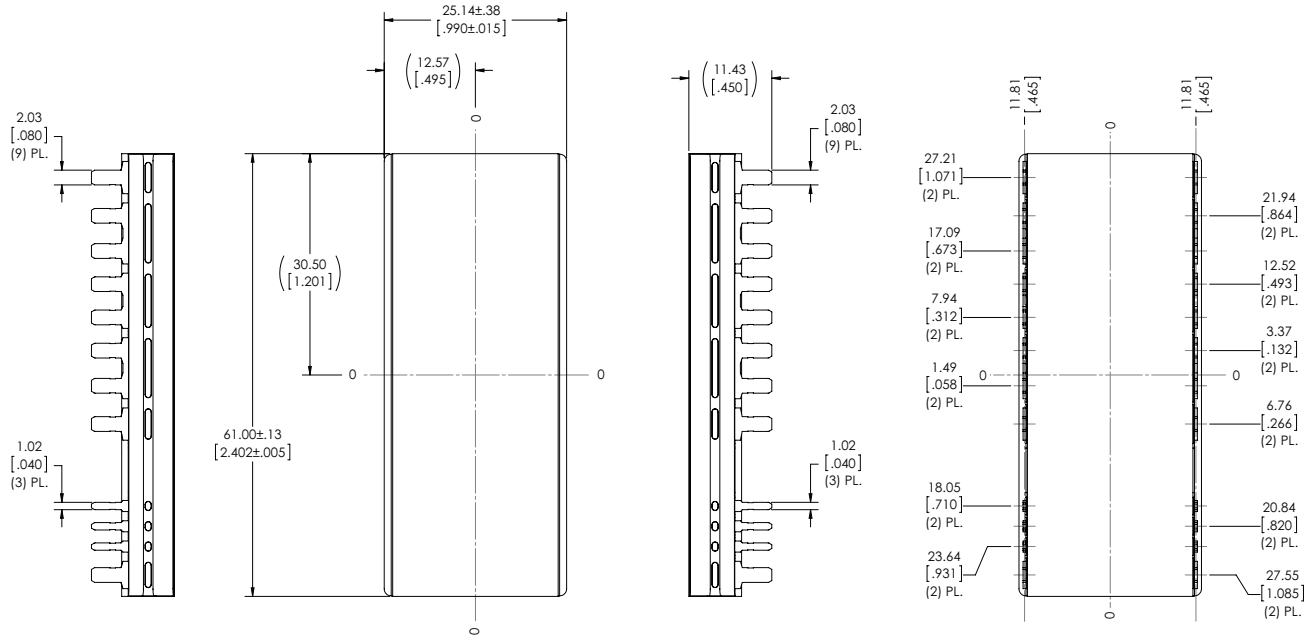
- Current rating
  (usually greater than maximum input current of BCM)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: See safety agency approvals.

Reverse Operation

BCMs are capable of reverse power operation. Once the unit is started, energy will be transferred from the secondary output back to the primary input whenever the secondary output voltage exceeds $V_{PRI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

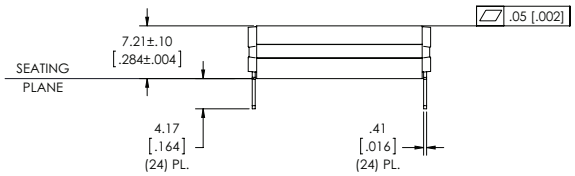
Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input.

BCM Through Hole Package Mechanical Drawing and Recommended Land Pattern



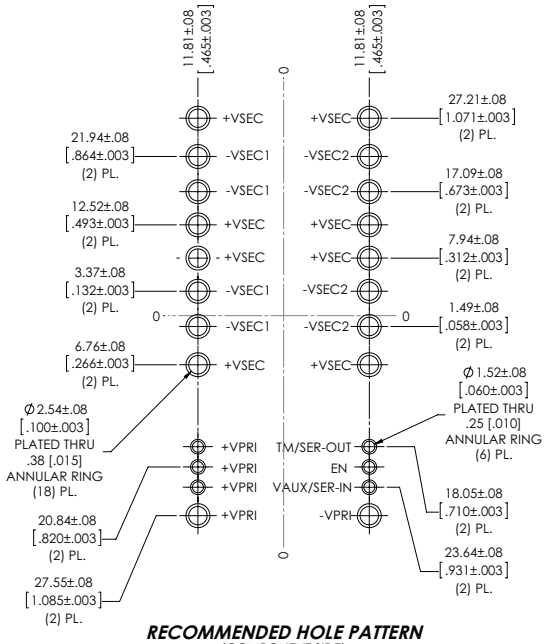
TOP VIEW (COMPONENT SIDE)

BOTTOM VIEW



NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.



RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	06/01/18	Initial release	n/a

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