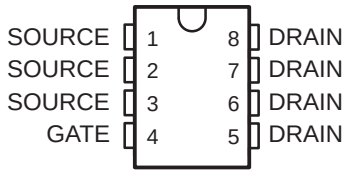
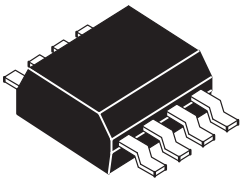
- **Low $r_{DS(on)}$ . . . 0.18 Ω Typ at V_{GS} = –10 V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = –1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV Per MIL-STD-883C, Method 3015**

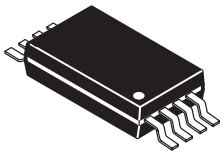
D OR PW PACKAGE
(TOP VIEW)



D PACKAGE



PW PACKAGE

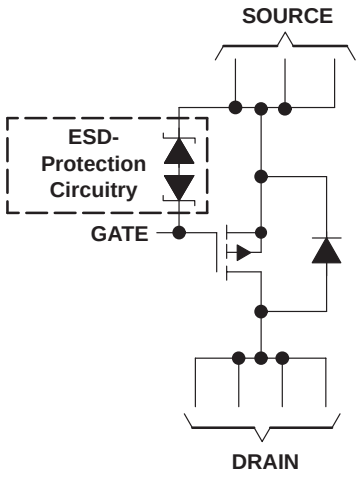


description

The TPS1100 is a single P-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of –1.5 V and an I_{DSS} of only 0.5 μA, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version with its smaller footprint and reduction in height fits in places where other P-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for a small-outline integrated circuit (SOIC) package.

schematic



NOTE A: For all applications, all source pins should be connected and all drain pins should be connected.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
–40°C to 85°C	TPS1100D	TPS1100PWLE	TPS1100Y

The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE). The chip form is tested at 25°C.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

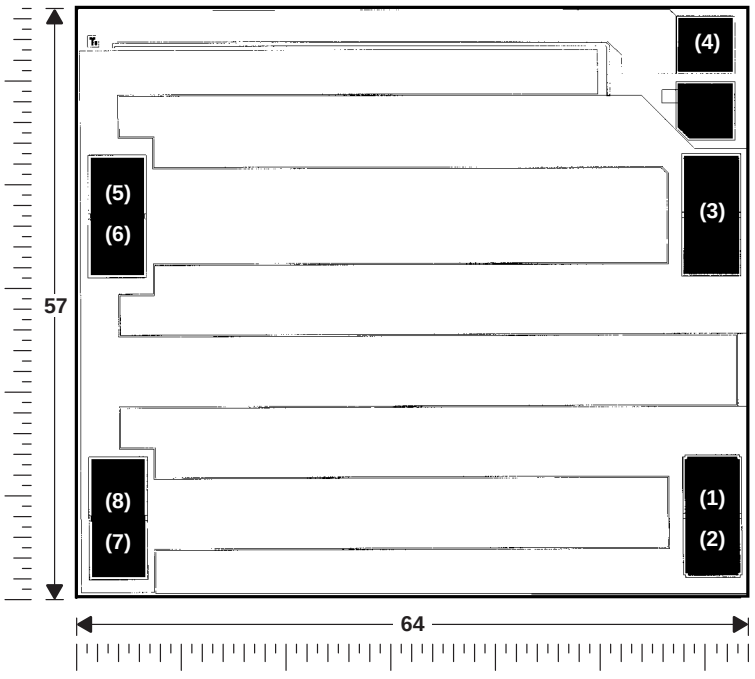
description (continued)

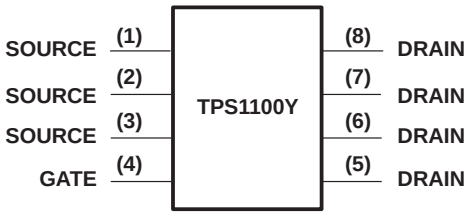
Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

TPS1100Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1100. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				–15	V
Gate-to-source voltage, V_{GS}				2 or –15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = –2.7 V	D package	T_A = 25°C	±0.41	A
			T_A = 125°C	±0.28	
		PW package	T_A = 25°C	±0.4	
			T_A = 125°C	±0.23	
	V_{GS} = –3 V	D package	T_A = 25°C	±0.6	
			T_A = 125°C	±0.33	
		PW package	T_A = 25°C	±0.53	
			T_A = 125°C	±0.27	
	V_{GS} = –4.5 V	D package	T_A = 25°C	±1	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.81	
			T_A = 125°C	±0.37	
	V_{GS} = –10 V	D package	T_A = 25°C	±1.6	
			T_A = 125°C	±0.72	
		PW package	T_A = 25°C	±1.27	
			T_A = 125°C	±0.58	
Pulsed drain current, I_D‡			T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S			T_A = 25°C	–1	A
Storage temperature range, T_{stg}				–55 to 150	°C
Operating junction temperature range, T_J				–40 to 150	°C
Operating free-air temperature range, T_A				–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on a FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/°C	323 mW	262 mW	101 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations when tested.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			TPS1100			TPS1100Y			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS},	I_D = –250 µA		–1	–1.25	–1.50		–1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	I_S = –1 A,	V_{GS} = 0 V			–0.9			–0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = –12 V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = –12 V,	V_{GS} = 0 V	T_J = 25°C			–0.5				µA
				T_J = 125°C			–10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = –10 V	I_D = –1.5 A			180			180		mΩ
		V_{GS} = –4.5 V	I_D = –0.5 A			291	400		291		
		V_{GS} = –3 V	I_D = –0.2 A			476	700		476		
		V_{GS} = –2.7 V				606	850		606		
g_{fs}	Forward transconductance†	V_{DS} = –10 V,	I_D = –2 A			2.5			2.5		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1100, TPS1100Y			UNIT
					MIN	TYP	MAX	
Q_g	Total gate charge	V_{DS} = –10 V,	V_{GS} = –10 V,	I_D = –1 A		5.45		nC
Q_{gs}	Gate-to-source charge					0.87		
Q_{gd}	Gate-to-drain charge					1.4		
$t_{d(on)}$	Turn-on delay time	V_{DD} = –10 V, R_G = 6 Ω,	R_L = 10 Ω, See Figures 1 and 2	I_D = –1 A,		4.5		ns
$t_{d(off)}$	Turn-off delay time					13		ns
t_r	Rise time					10		ns
t_f	Fall time					2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	I_F = 5.3 A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

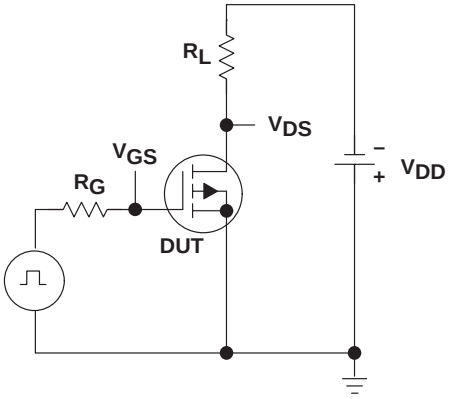


Figure 1. Switching-Time Test Circuit

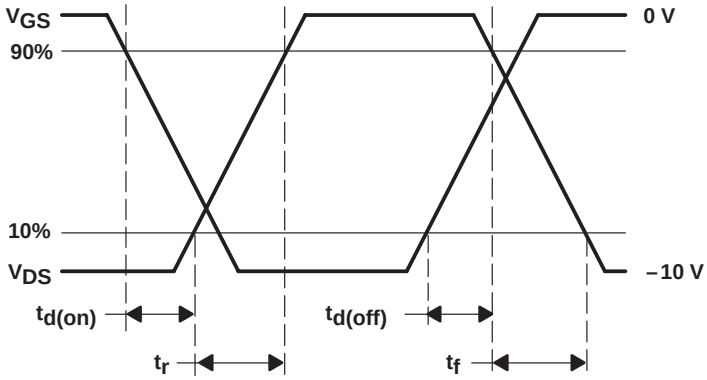


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

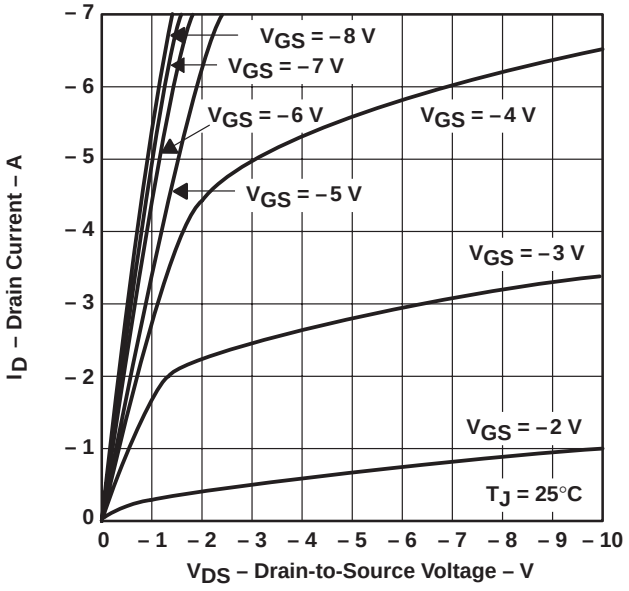


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

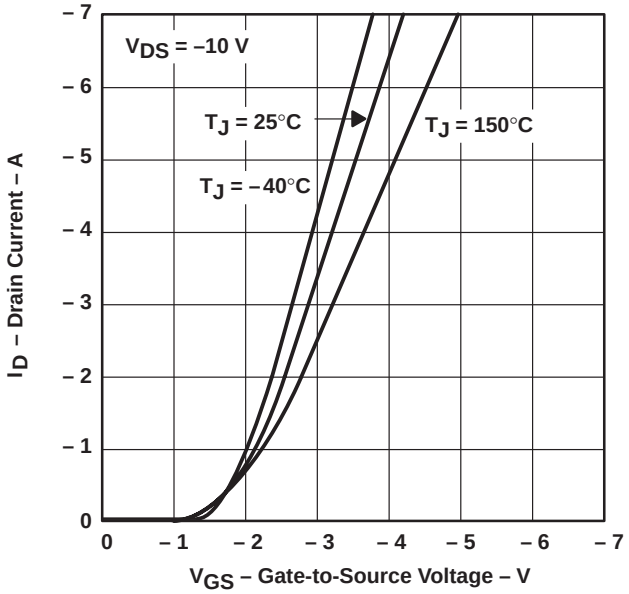


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

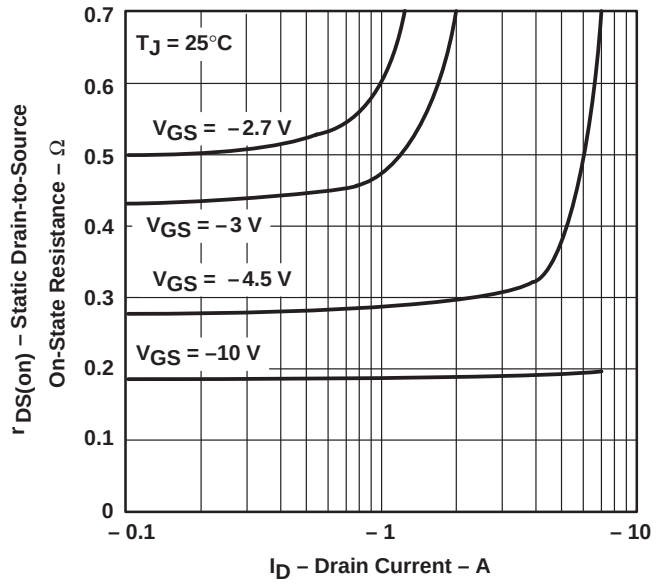
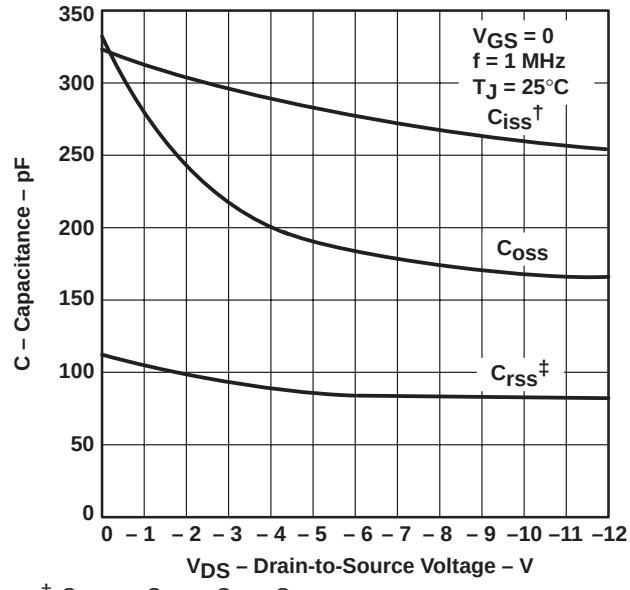


Figure 5

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + \dfrac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

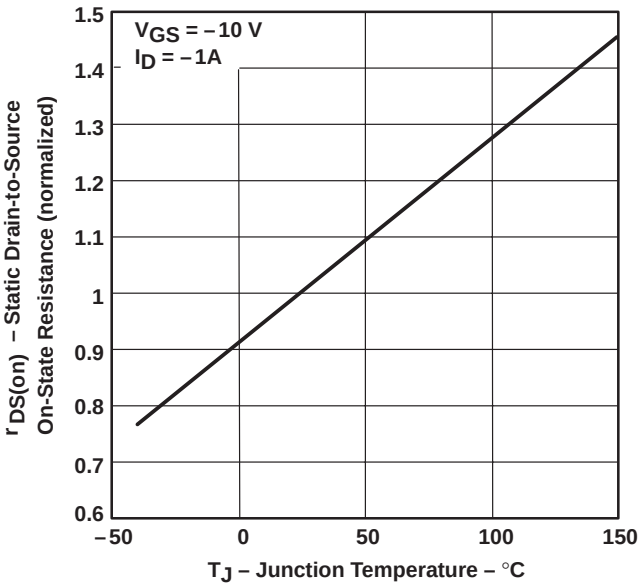


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

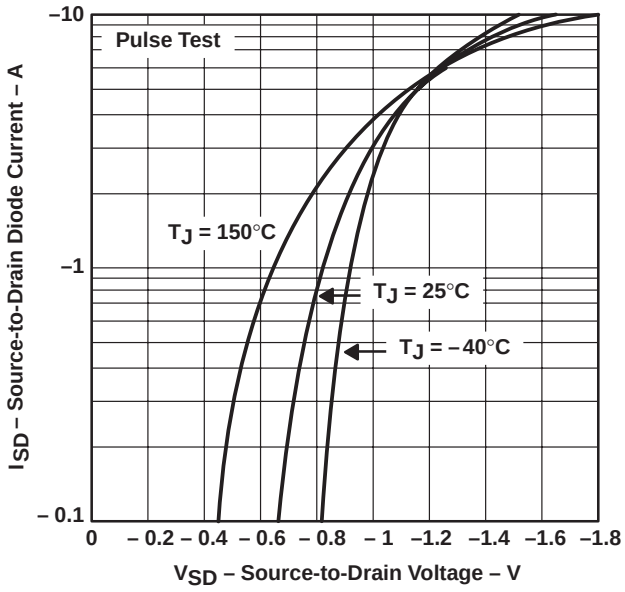


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

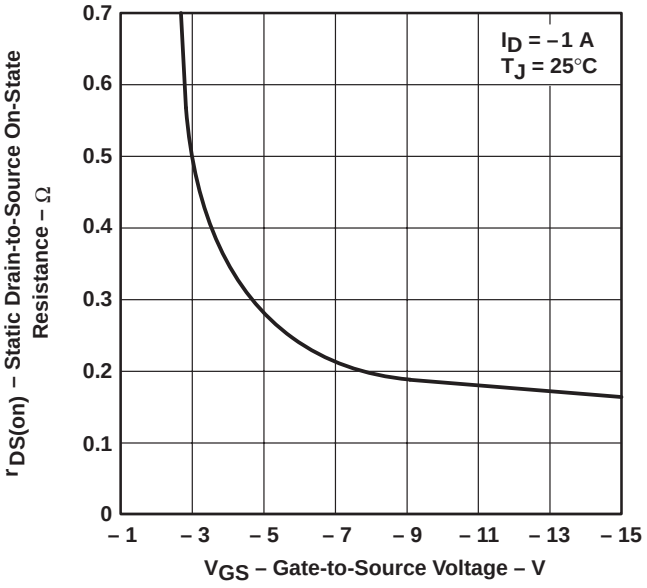


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

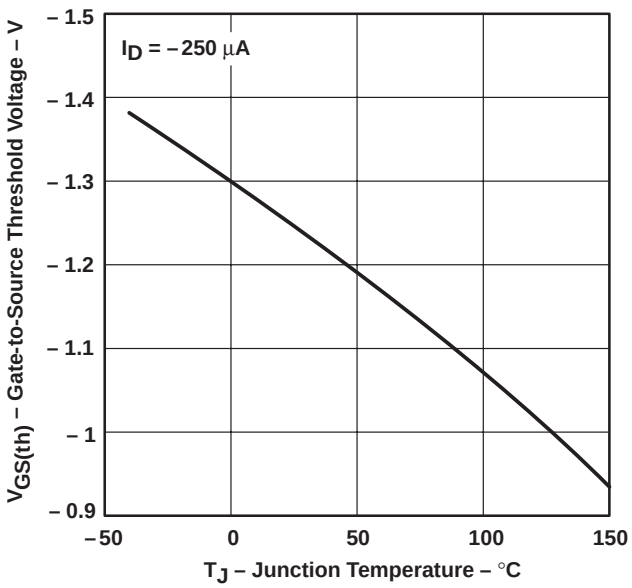


Figure 10

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

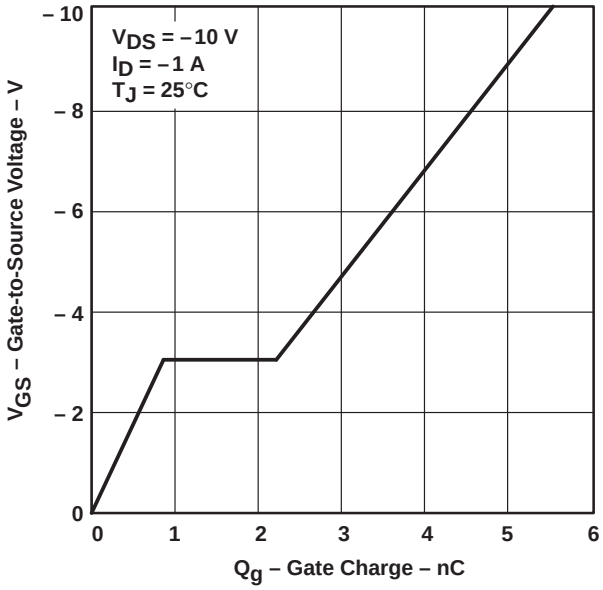


Figure 11

THERMAL INFORMATION

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

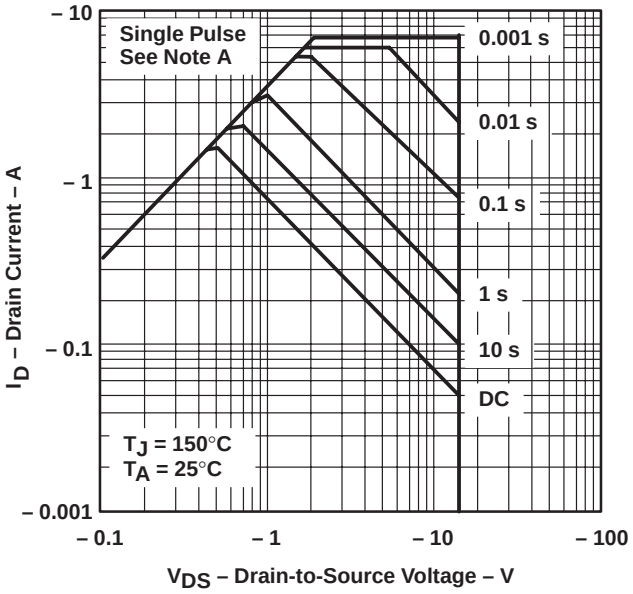


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT THERMAL IMPEDANCE vs PULSE DURATION

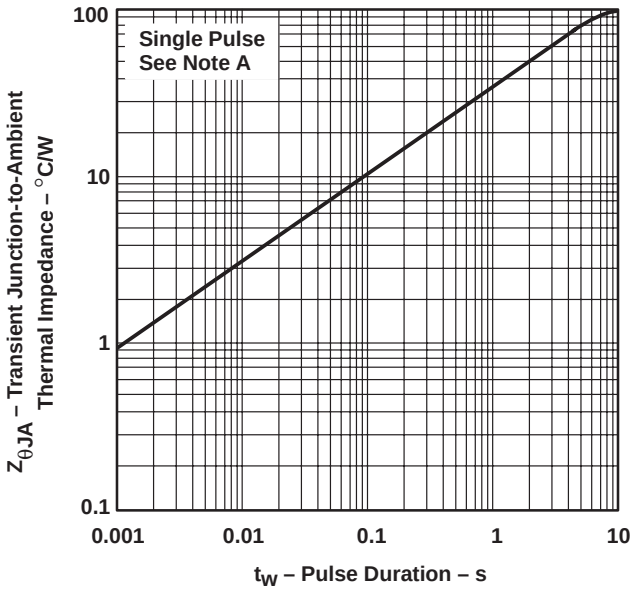


Figure 13

NOTE A: Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION

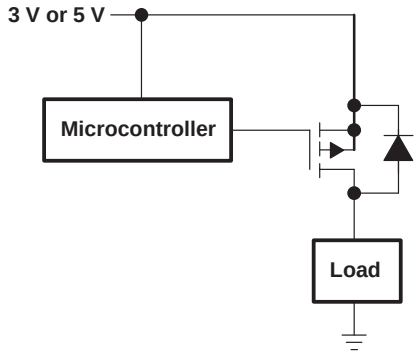


Figure 14. Notebook Load Management

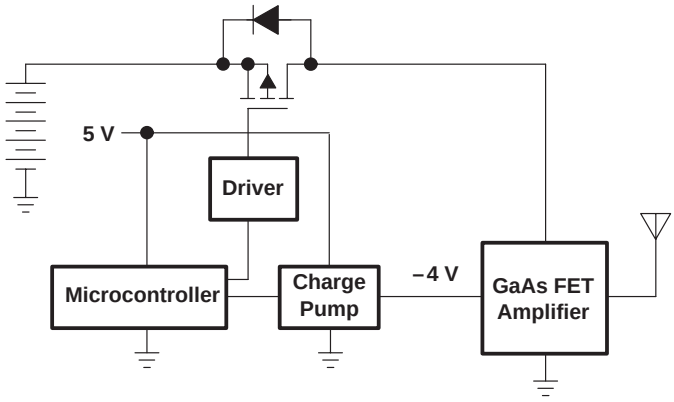


Figure 15. Cellular Phone Output Drive

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS1100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DRG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI			Samples
TPS1100PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1100	Samples
TPS1100PWG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI			Samples
TPS1100PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI			
TPS1100PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1100	Samples
TPS1100PWRG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

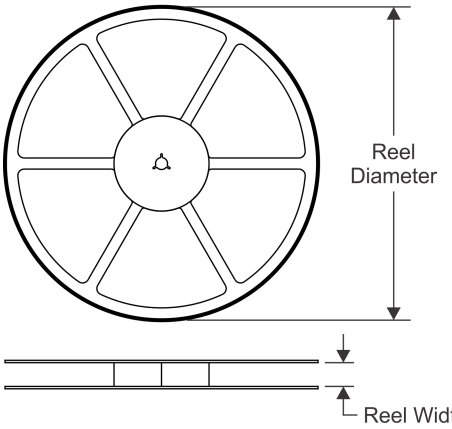
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

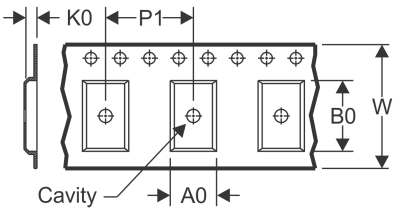
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

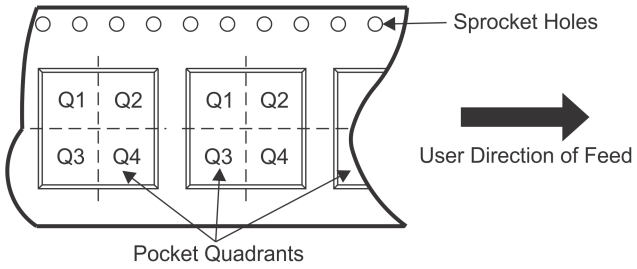


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

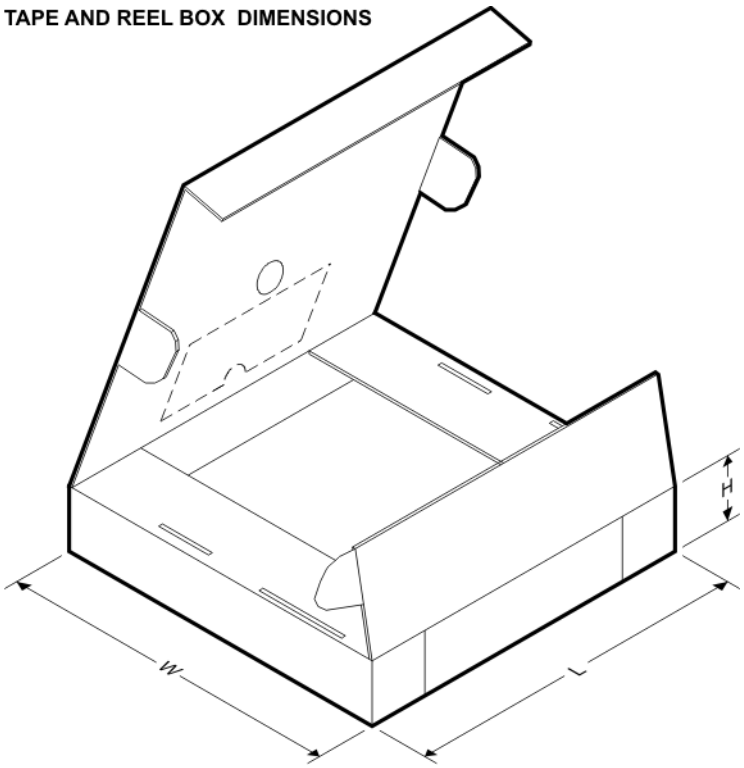
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS1100PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1100DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS1100PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

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