

LM5026 Active Clamp Current Mode PWM Controller

Check for Samples: [LM5026](#)

FEATURES

- Current Mode Control
- Internal 100V Start-up Bias Regulator
- 3A Compound Main Gate Driver
- High Bandwidth Opto-coupler Interface
- Programmable Line Under-Voltage Lockout (UVLO) with Adjustable Hysteresis
- Versatile Dual Mode Over-Current Protection with hiccup delay timer
- Programmable Overlap or Deadtime between the Main and Active Clamp Outputs
- Programmable Maximum Duty Cycle Clamp
- Programmable Soft-start
- Leading Edge Blanking
- Resistor Programmed 1MHz Capable Oscillator
- Oscillator Sync I/O Capability
- Precision 5V Reference

PACKAGES

- TSSOP-16
- WSON-16 (5x5 mm) Thermally Enhanced

DESCRIPTION

The LM5026 PWM controller contains all of the features necessary to implement power converters utilizing the active clamp / reset technique with current mode control. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The device can be configured to control either a P-Channel or N-Channel clamp switch. The main gate driver features a compound configuration, consisting of both MOS and Bipolar devices, providing superior gate drive characteristics. The LM5026 can be configured to operate with bias voltages over a wide input range of 8V to 100V. Additional features include programmable maximum duty cycle, line under-voltage lockout, cycle-by-cycle current limit, hiccup mode fault operation with adjustable timeout delay, PWM slope compensation, soft-start, 1MHz capable oscillator with synchronization input / output capability, precision reference and thermal shutdown.

Typical Application Circuit

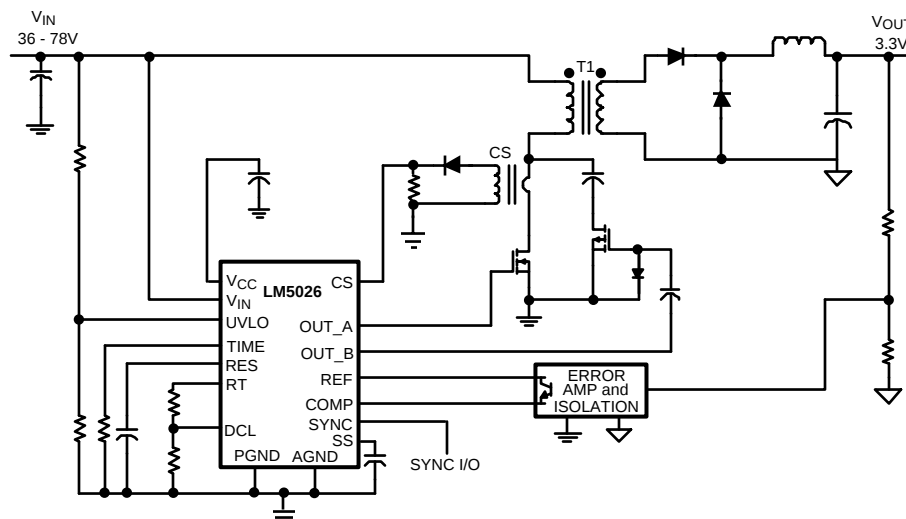


Figure 1. Simplified Forward Power Converter with Active Clamp Reset



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Connection Diagram

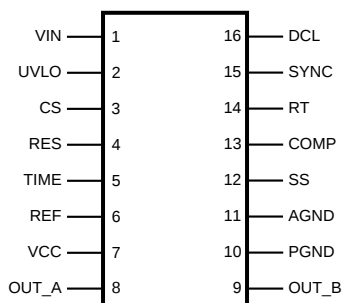


Figure 2. 16-Lead TSSOP

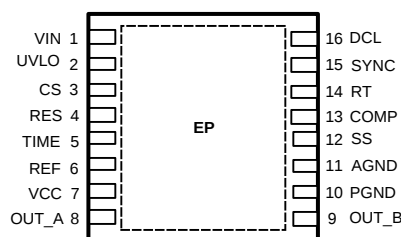


Figure 3. 16-Lead WSON

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	VIN	Input Voltage Source	Input to the Start-up Regulator. Operating input range is 13V to 100V with transient capability to 105V. For power sources outside of this range, the LM5026 can be biased directly at VCC by an external regulator.
2	UVLO	Line Under-Voltage Lockout	An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4V threshold the VCC and REF regulators are enabled. At the 1.25V threshold the SS pin is released and the device enters the active mode.
3	CS	Current Sense input for current mode control and current limit	If CS exceeds 0.5V the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 100nS after OUT_A switches high to blank leading edge transients.
4	RES	Restart Timer	If cycle-by-cycle current limit is reached during any cycle, a 10uA current is sourced to the RES pin capacitor. If the RES capacitor voltage reaches 2.5V, the soft-start capacitor will be fully discharged and then released with a pull-up current of 1uA. After the first output pulse at OUT_A (when SS = 1.4V), the SS pin charging current will revert back to 50 µA.
5	TIME	Gate Drive Overlap or Deadtime Control	An external resistor (RSET) sets either the overlap time or deadtime for the active clamp output. An RSET resistor connected between TIME and AGND produces in-phase OUT_A and OUT_B pulses with overlap. An RSET resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime.
6	REF	Output of 5V Reference	Maximum output current is 10mA. Locally decouple with a 0.1µF capacitor.
7	VCC	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.6 V.	If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, thus reducing the IC power dissipation.
8	OUT_A	Main Output Driver	Output of the main switch PWM gate driver. Capable of 3A peak sink current.
9	OUT_B	Active Clamp Output Driver	Output of the active clamp switch gate driver. Capable of 0.5A peak source and sink current.
10	PGND	Power Ground	Connect directly to Analog Ground
11	AGND	Analog Return	Connect directly to Power Ground.
12	SS	Soft-start	An external capacitor and an internal 50 µA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event. The soft-stop discharge current is 50 µA.
13	COMP	Input to the Pulse Width Modulator	The external opto-coupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is maximum with zero input current, while 1mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the ac voltage across the opto-coupler detector.
14	RT	Oscillator Frequency Control	Normally biased at 2V. The total external resistance connected between RT and AGND sets the internal oscillator frequency.
15	SYNC	Oscillator Synchronization Input/Output	The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM5026 devices can be synchronized together by connection of their SYNC pins.
16	DCL	Maximum Duty Cycle Control	An external resistor divider connected from RT to AGND sets the maximum output duty cycle for OUT_A.

PIN DESCRIPTIONS (continued)

Pin	Name	Description	Application Information
EP	Exposed Pad (WSON Package Only)	Exposed Pad, underside of WSON package	Connect to system ground plane for reduced thermal resistance.

Block Diagram

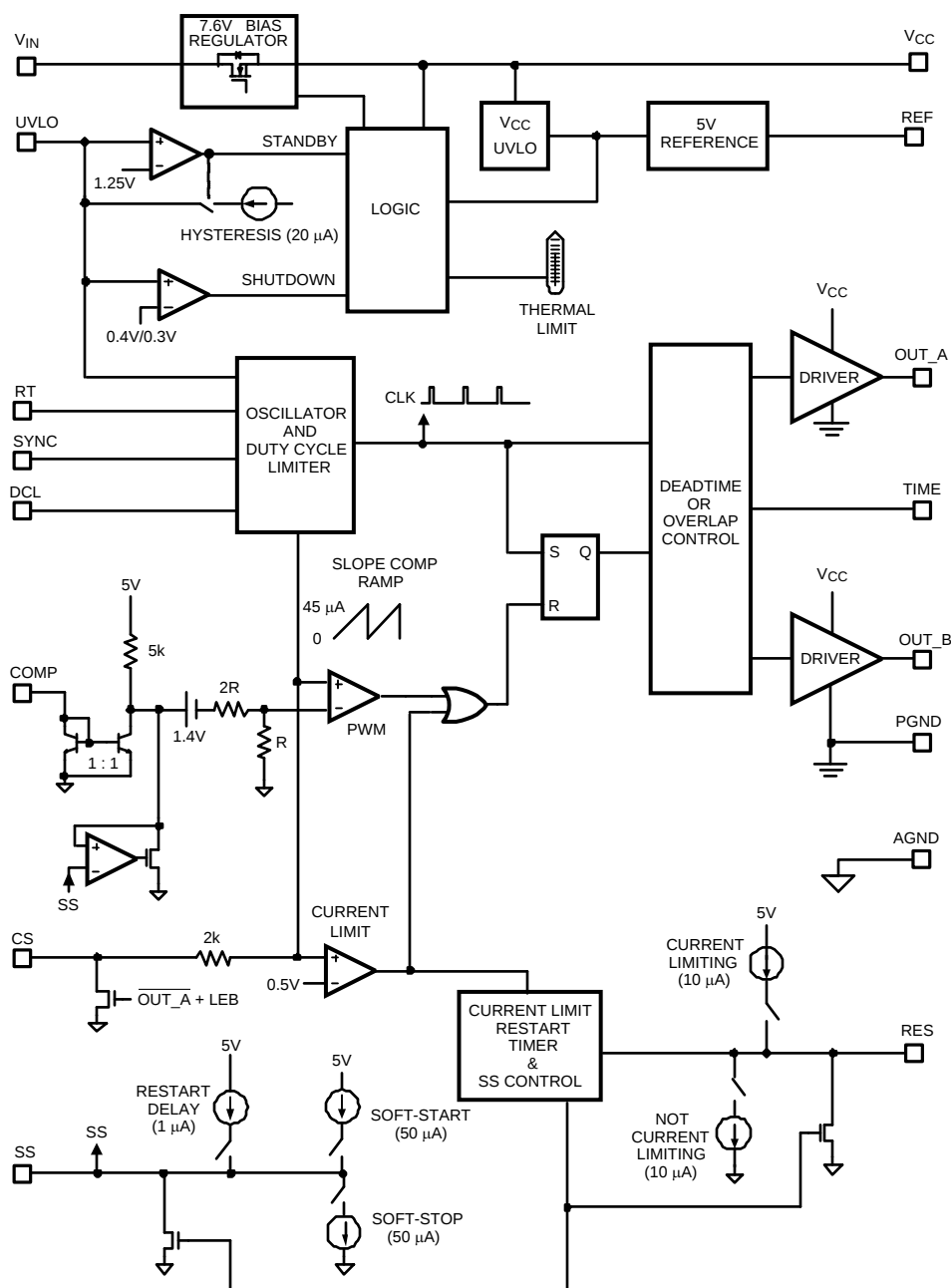


Figure 4. Simplified Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

V_{IN} to GND	-0.3V to 105V
V_{CC} to GND	-0.3V to 16V
CS to GND	-0.3 to 1.0V
COMP Input Current	10mA
All other inputs to GND	-0.3 to 7V
ESD Rating ⁽³⁾	Human Body Model
Storage Temperature Range	-65°C to 150°C
Junction Temperature	150°C

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5 k Ω resistor into each pin.

Operating Ratings⁽¹⁾

V_{IN} Voltage	13 to 100V
External Voltage Applied to V_{CC}	8V to 15V
Operating Junction Temperature	-40°C to +125°C

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard typeface are for $T_J = 25^\circ\text{C}$, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN} = 48\text{V}$, $V_{CC} = 10\text{V}$, $R_T = 30.0\text{k}\Omega$, $R_{SET} = 34.8\text{k}\Omega$ unless otherwise stated ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator						
V_{CC} Reg	V_{CC} Regulation	No Load	7.3	7.6	7.9	V
	V_{CC} Current Limit	See ⁽²⁾	20	25		mA
$I-V_{IN}$	Startup Regulator Leakage (external V_{CC} Supply)	$V_{IN} = 100\text{V}$		165	500	μA
	Shutdown Current (lin)	UVLO = 0V		350	450	μA
V_{CC} Supply						
	V_{CC} Under-voltage Lockout Voltage (positive going V_{CC})		V_{CC} Reg - 220mV	V_{CC} Reg - 120mV		V
	V_{CC} Under-voltage Hysteresis		1.0	1.5	2.0	V
	V_{CC} Supply Current (I_{CC})	$C_{gate} = 0$, UVLO = 1.3V			4.2	mA
Reference Supply						
V_{REF}	Ref Voltage	$I_{REF} = 0$ mA	4.85	5	5.15	V
	Ref Voltage Regulation	$I_{REF} = 0$ to 10mA		25	50	mV
	Ref Current Limit		10	20		mA
UVLO Shutdown/Standby						
	Undervoltage Shutdown Threshold		0.3	0.4	0.5	V

- (1) Min and Max limits are 100% production tested at 25 °C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Device thermal limitations may limit usable range.

Electrical Characteristics (continued)

Specifications with standard typeface are for $T_j = 25^\circ\text{C}$, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN} = 48\text{V}$, $V_{CC} = 10\text{V}$, $R_T = 30.0\text{k}\Omega$, $R_{SET} = 34.8\text{k}\Omega$ unless otherwise stated ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Undervoltage Shutdown Hysteresis			0.1		V
	Undervoltage Standby Threshold		1.21	1.25	1.29	V
	Undervoltage Standby Hysteresis Current Source		16	20	24	μA
Current Limit						
	Cycle by Cycle Threshold Voltage		0.45	0.5	0.55	V
	ILIM Delay to Output	CS step from 0 to 0.6V Time to onset of OUT transition (90%) Cgate=0		40		ns
	Leading Edge Blanking Time		70	100	130	ns
	CS Sink Impedance (clocked)	I _{CS} = 10mA		30	65	Ω
Over Current Restart						
	Restart Threshold		2.4	2.55	2.7	V
	Fault Charging Current		7.5	10	12.5	μA
	Discharging Current		7.5	10	12.5	μA
Soft-Start						
	Soft-start Current Source		38	50	58	μA
	Soft-stop Current Sink		38	50	58	
	Soft-start Current Source following a restart event		0.6	1	1.3	
Oscillator						
	Frequency1	RT = 30.0 kΩ	180	200	220	kHz
	Frequency2	RT = 10.0 kΩ	520	590	660	kHz
	SYNC Source Current			200		μA
	SYNC Sink Impedance	Can sync up to 5 like controllers minimum		100		Ω
	Sync Threshold (falling)			1.4		V
	Sync Pulse Width Minimum		15			ns
PWM Comparator						
	Delay to Output	CS stepped, Time to onset of OUT_A transition low		40		ns
	Mimimum Duty Cycle	I _{COMP} = 1mA			0	%
	Maximum Duty Cycle Limit 1	UVLO=1.3V, COMP = open, V _{DCL} = 2.5V		80		%
	Maximum Duty Cycle Limit 2	UVLO=1.3V, COMP = open, V _{DCL} = V _{RT} x 0.875		70		%
	Maximum Duty Cycle Limit 3	UVLO=2.92V, COMP = open, V _{DCL} = 2.5V		40		%
	SS to PWM Offset			1.4		V
	COMP Input Impedance	Small signal impedance		1700		Ω
	Slope Compensation Amplitude	Delta increase at PWM comparator to CS	75	90	115	mV
Output Section						

Electrical Characteristics (continued)

Specifications with standard typeface are for $T_j = 25^\circ\text{C}$, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN} = 48\text{V}$, $V_{CC} = 10\text{V}$, $R_T = 30.0\text{k}\Omega$, $R_{SET} = 34.8\text{k}\Omega$ unless otherwise stated ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	OUT_A High Saturation	MOS Device @ $I_{out} = -10\text{mA}$,		5	10	Ω
	OUTPUT_A Peak Current Sink	Bipolar Device @ $V_{CC}/2$		3		A
	OUT_A Low Saturation	MOS Device @ $I_{out} = 10\text{mA}$,		6	9	Ω
	OUTPUT_A Rise Time	$C_{gate} = 2.2\text{nF}$		20		ns
	OUTPUT_A Fall Time	$C_{gate} = 2.2\text{nF}$		15		ns
	OUT_B High Saturation	$I_{out} = -10\text{mA}$,		10	20	Ω
	OUT_B Low Saturation	$I_{out} = 10\text{mA}$,		10	20	Ω
	OUTPUT_B Rise Time	$C_{gate} = 470\text{pF}$		15		ns
	OUTPUT_B Fall Time	$C_{gate} = 470\text{pF}$		15		ns
Output Timing Control						
	Overlap Time	$R_{SET} = 34.8\text{ k}\Omega$ connected to GND, 50% to 50% transitions	70	100	130	ns
	Deadtime	$R_{SET} = 30.0\text{ k}\Omega$ connected to REF, 50% to 50% transitions	70	100	130	ns
Thermal Shutdown						
T_{SD}	Thermal Shutdown Temp.		150	165		$^\circ\text{C}$
	Thermal Shutdown Hysteresis			25		$^\circ\text{C}$
Thermal Resistance						
θ_{JA}	Junction to Ambient	PW0016A Package		125		$^\circ\text{C/W}$
		NHQ0016A Package		32		$^\circ\text{C/W}$

Typical Performance Characteristics

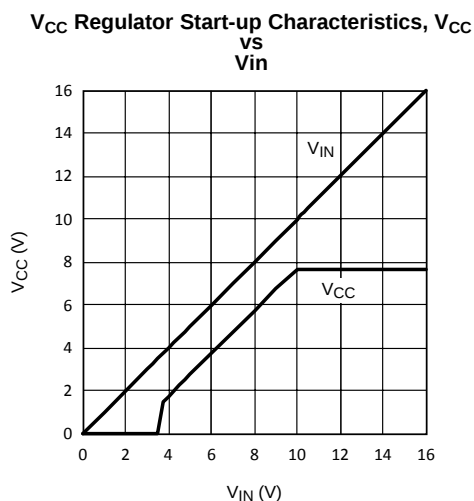


Figure 5.

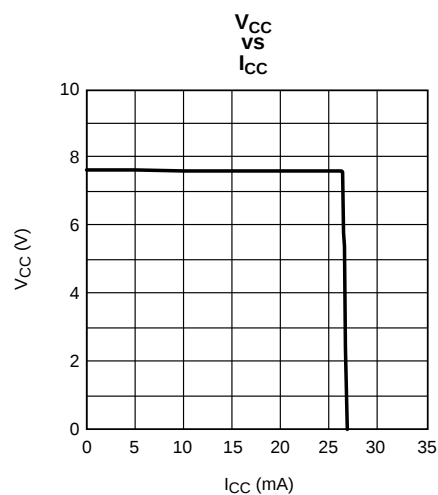


Figure 6.

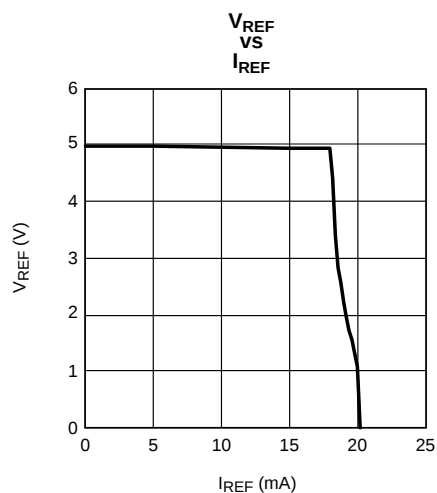


Figure 7.

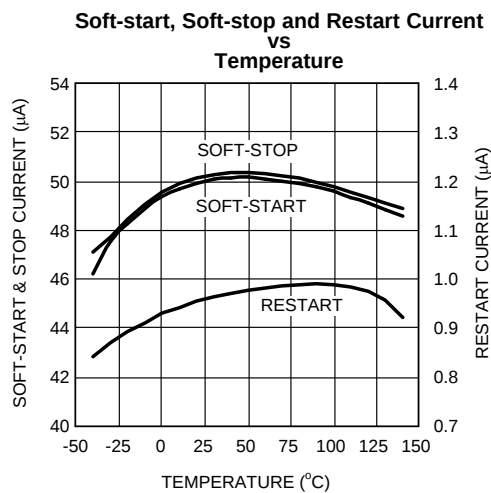


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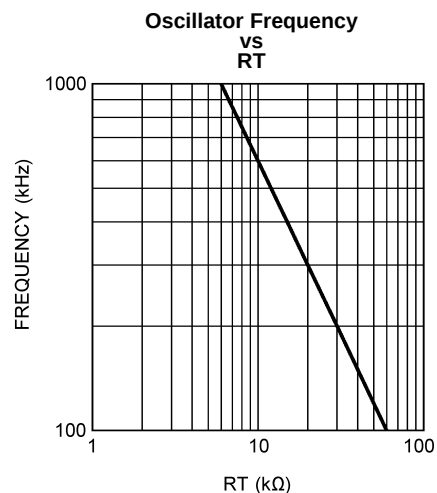


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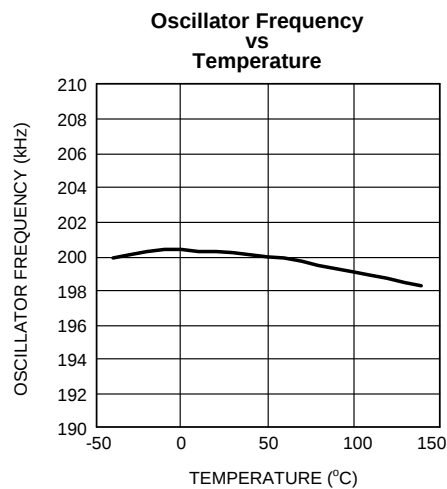


Figure 10.

Typical Performance Characteristics (continued)

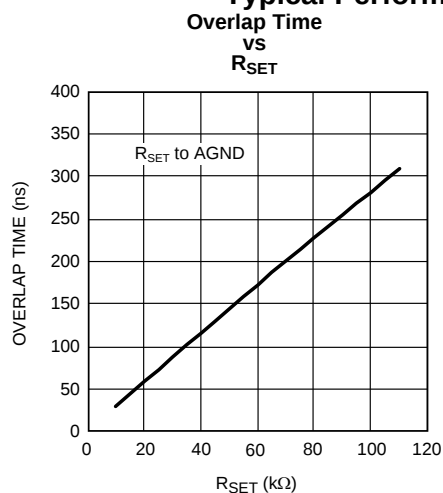


Figure 11.

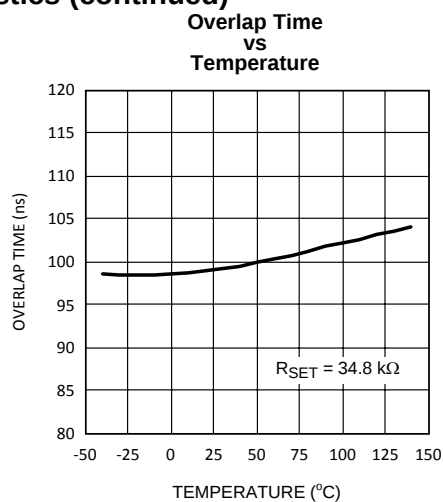


Figure 12.

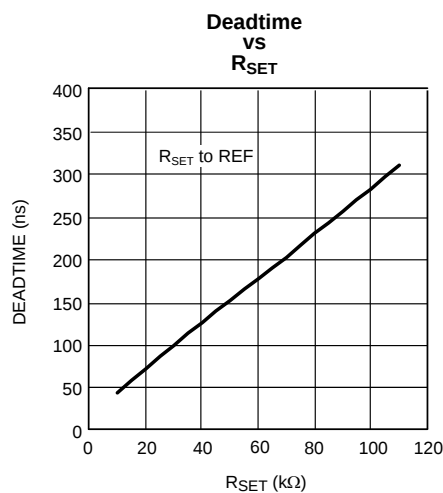


Figure 13.

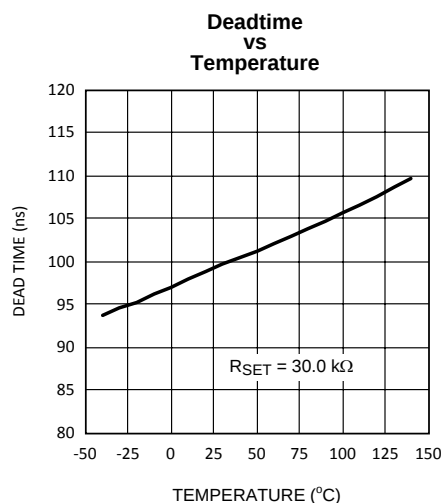


Figure 14.

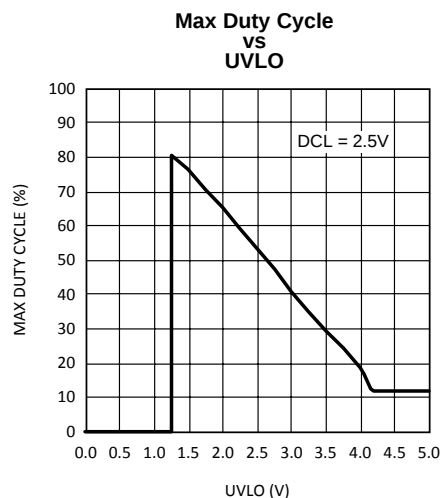


Figure 15.

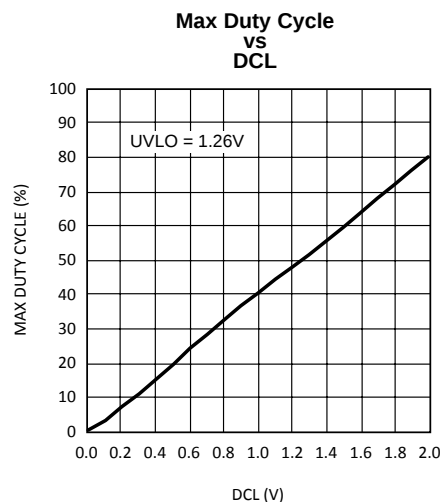


Figure 16.

Typical Performance Characteristics (continued)

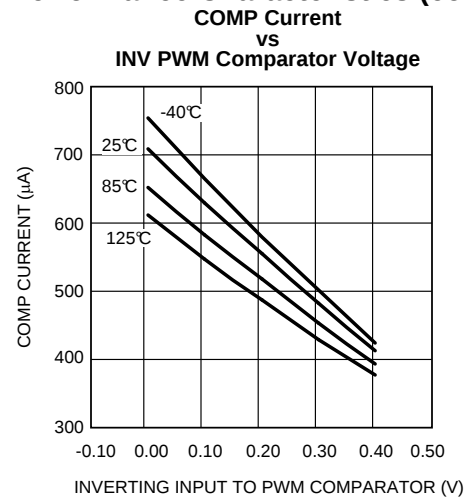


Figure 17.

DETAILED OPERATING DESCRIPTION

The LM5026 PWM controller contains all of the features necessary to implement power converters utilizing the active clamp reset technique with current mode control. With the active clamp reset, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp reset techniques. The LM5026 provides two control outputs, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The device can be configured to drive either a P-Channel or N-Channel clamp switch. The main switch gate driver features a compound configuration consisting of both MOS and bipolar devices, which provide superior gate drive characteristics. The LM5026 can be configured to operate with bias voltages over a wide input range from 8V to 100V. Additional features include programmable maximum duty cycle, line under-voltage lockout, cycle-by-cycle current limit, hiccup mode fault protection with adjustable delays, PWM slope compensation, soft-start, a 1MHz capable oscillator with synchronization Input / Output capability, precision reference and thermal shutdown.

High Voltage Start-Up Regulator

The LM5026 contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48V dc line voltage. The regulator output (VCC) is internally current limited to 20mA. When power is applied and the UVLO pin potential is greater than 0.4V, the regulator is enabled and sources current into an external capacitor connected to the VCC pin. The recommended capacitance range for the VCC regulator is 0.1 μ F to 100 μ F. The VCC regulator provides power to the internal voltage reference, PWM controller and gate drivers. The controller outputs are enabled when the voltage on the VCC pin reaches the regulation point of 7.6V, the internal voltage reference (REF) reaches its regulation point of 5V and the UVLO voltage is greater than 1.25V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation.

The external VCC capacitor must be sized such that the current delivered from the capacitor and the VCC regulator will maintain a VCC voltage greater than 6.2V during the initial start-up. During a fault mode when the converter auxiliary winding is inactive, external current draw on the VCC line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the IC package. An external start-up or bias regulator can be used to power the LM5026 instead of the internal start-up regulator by connecting the VCC and the VIN pins together and connecting an external bias supply to these two pins.

Line Under-Voltage Detector

The LM5026 contains a dual level Under-Voltage Lockout (UVLO) circuit. When the UVLO pin voltage is below 0.4V the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4V but less than 1.25V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed the VCC and REF under-voltage thresholds and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when VIN is in the desired operating range. UVLO hysteresis is accomplished with an internal 20 μ A current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The hysteresis of the 0.4V shutdown comparator is fixed at 100mV.

The UVLO pin can also be used to implement various remote enable / disable functions. Pulling the UVLO pin below the 0.4V threshold totally disables the controller. Pulling the UVLO pin to a potential between 1.25 and 0.4V places the controller in standby with the VCC and REF regulators operating. Turning off a converter by forcing the UVLO pin to the standby condition provides a controlled soft-stop. The controller outputs are not directly disabled in standby mode, rather the soft-start capacitor is discharged with a 50 μ A sink current. Discharging the soft-start capacitor gradually reduces the PWM duty cycle to zero, providing a slow controlled discharge of the power converter output filter. This controlled discharge can help prevent uncontrolled behavior of self-driven synchronous rectifiers during turn-off.

PWM Outputs

The relative phase of the main switch gate driver OUT_A and active clamp gate driver OUT_B can be configured for multiple applications. For active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase, with the active clamp output overlapping the main output. For active clamp configurations utilizing a high side N-Channel switch, the active clamp output should be out of phase with main output and there should be a dead time between the two gate drive pulses. A distinguishing feature of the LM5026 is the ability to accurately configure either deadtime (both off) or overlap time (both on) of the gate driver outputs. The overlap / deadtime magnitude is controlled by the resistor value (R_{SET}) connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for deadtime control or to AGND for overlap control. The internal configuration detector senses the direction of current flow in the TIME pin resistor and configures the phase relationship of the main and active clamp outputs.

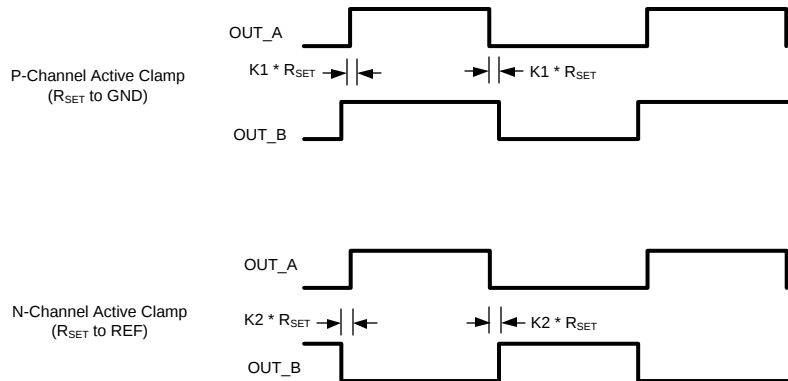


Figure 18. PWM Output Phasing / Timing

The rising edge overlap or deadtime and the falling edge overlap or deadtime are identical and are independent of operating frequency or duty cycle. The magnitude of the overlap/deadtime can be calculated as follows:

$$\text{Overlap Time} = 2.8 \times R_{\text{SET}} + 2$$

where

- R_{SET} in kΩ
- overlap is in ns

(1)

$$\text{Deadtime} = 2.9 \times R_{\text{SET}} + 14$$

where

- R_{SET} in kΩ
- deadtime is in ns

(2)

Gate Driver Outputs

The LM5026 provides two gate driver outputs, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The main gate driver features a compound configuration, consisting of both MOS and bipolar devices, which provide superior gate drive characteristics. The bipolar device provides most of the drive current capability and sinks a relatively constant current, which is ideal for driving large power MOSFETs. As the switching event nears conclusion and the bipolar device saturates, the internal MOS device provides a low impedance to complete the switching event.

During turn-off at the Miller plateau region, typically between 2V - 4V, the voltage differential between the output and PGND is small and the current source characteristic of the bipolar device is beneficial to reduce the transition time. During turn-on, the resistive characteristics of a purely MOS gate driver is adequate since the supply to output voltage differential is fairly large in the Miller region.

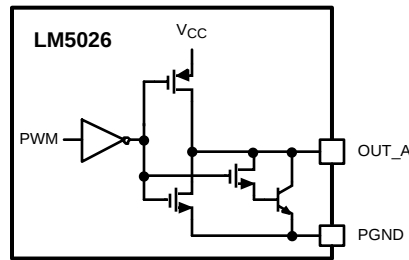


Figure 19. Compound Gate Driver

PWM Comparator/Slope Compensation

The PWM comparator modulates the pulse width of the controller output by comparing the current sense ramp signal to the loop error signal. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The loop error signal is input into the controller in the form of a control current into the COMP pin. The COMP pin control current is internally mirrored by a matched pair of NPN transistors which sink current through a 5 kΩ resistor connected to the 5V reference. The resulting error signal passes through a 1.4V level shift and a gain reducing 3:1 resistor divider before being applied to the pulse width modulator.

The opto-coupler detector can be connected between the REF pin and the COMP pin. Because the COMP pin is controlled by a current input, the potential difference across the optocoupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the opto-coupler is greatly reduced. Greater system loop bandwidth can be realized, since the bandwidth-limiting pole associated with the opto-coupler is now at a much higher frequency. The PWM comparator polarity is configured such that with no current into the COMP pin, the controller produces the maximum duty cycle at the main gate driver output.

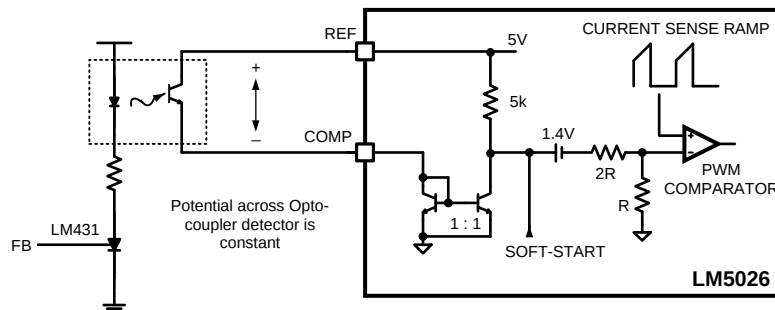


Figure 20. Opto-Coupler to LM5026 COMP Interface

For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. The LM5026 integrates this slope compensation by summing a current ramp generated by the oscillator with the current sense signal. The PWM comparator ramp signal is a combination of the current waveform at the CS pin, and an internally generated slope compensation ramp derived from the oscillator. The internal ramp has an amplitude of 0 to 45 μA which is sourced into an internal 2 kΩ resistor, plus the external impedance at the CS pin. Additional slope compensation may be added by increasing the source impedance of the current sense signal.

Maximum Duty Cycle Clamp

Controlling the maximum duty cycle of an active clamp reset PWM controller is necessary to limit the voltage stress on the main and active clamp MOSFETs. The relationship between the maximum drain-source voltage of the MOSFETs and the maximum PWM duty cycle is provided by the following equation:

$$V_{ds(max)} = \frac{V_{IN}}{1 - D(max)} \quad (3)$$

The main output (OUT_A) duty cycle is normally controlled by the control current sourced into the COMP pin from the external feedback circuit. When the feedback demands maximum output from the converter, the duty cycle will be limited by one of two circuits within the LM5026: the user programmable duty cycle clamp and the voltage-dependent duty cycle limiter, which varies inversely with the input line voltage.

Programmable Duty Cycle Clamp – The maximum allowed duty cycle can be programmed by setting a voltage at the DCL pin to a value less than 2V. The recommended method to set the DCL pin voltage is with a resistor divider connected from the RT pin to AGND. The voltage at the RT pin is internally regulated to 2V, while the current sourced from the RT pin sets the oscillator frequency. The maximum duty can be programmed, according to the following equation:

$$\text{Programmable Duty Cycle Clamp} = 80\% \times \frac{RT2}{RT1 + RT2} \quad (4)$$

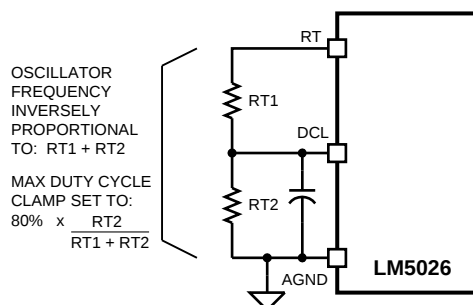


Figure 21. Programming oscillator Frequency and Maximum Duty Cycle Clamp

Line Voltage Duty Cycle Limiter - The maximum duty cycle for the main output driver is also limited by the voltage at the UVLO pin, which is normally proportional to VIN. The controller outputs are disabled until the UVLO pin voltage exceeds 1.25V. At the minimum operating voltage (when UVLO = 1.25V) the maximum duty cycle starts at the duty cycle clamp level programmed by the DCL pin voltage (80% or less). As the line voltage increases, the maximum duty cycle decreases linearly with increasing UVLO voltage, as illustrated in Figure 22. Ultimately the duty cycle of the main output is controlled to the least of the following three variables: the duty cycle controlled by the PWM comparator, the programmable maximum duty cycle clamp, or the line voltage dependent duty cycle limiter.

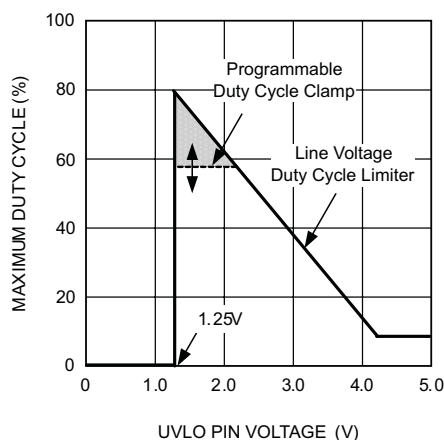


Figure 22. Maximum Duty Cycle vs UVLO Voltage

Soft-Start/Soft-Stop

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turn-on, the SS pin capacitor is discharged by an internal switch. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 50uA current source. The PWM comparator control voltage is clamped to the SS pin voltage. When the PWM input reaches 1.4V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5V, while the voltage at the PWM comparator increases to the value required for regulation determined by the voltage feedback loop.

If the UVLO pin voltage falls below the 1.25V standby threshold but above the 0.4V shutdown threshold, the 50uA SS pin source current is disabled and a 50uA sink current discharges the soft-start capacitor. As the SS voltage falls and clamps the PWM comparator input, the PWM duty cycle will gradually fall to zero. This soft-stop feature produces a gradual reduction of the power converter output voltage. This gradual discharge of the output filter prevents oscillations in the self-driven synchronous rectifiers on the secondary side of the converter during turn-off.

Current Sense/Current Limit

The CS input provides a control ramp for the pulse width modulator and current limit detection for overload protection. If the sensed voltage at the CS comparator exceeds 0.5V the present cycle is terminated (cycle-by-cycle current limit mode).

A small RC filter, located near the controller, is recommended for the CS input pin. An internal FET connected to the CS input discharges the current sense filter capacitor at the conclusion of every cycle to improve dynamic performance. This same FET remains on for an additional 100nS at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal.

The CS comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the LM5026 (CS and AGND pins). If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network, which should be located close to the IC. If a sense resistor located in the source of the main switch MOSFET is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the AGND pin and a single connection should be made to the power ground (sense resistor ground point).

Overload Protection Timer

The LM5026 provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmable by means of an external capacitor at the RES pin. During each PWM cycle the LM5026 either sources or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 10uA discharge current sink is enabled to hold the RES pin at ground. If a current limit is detected, the 10uA sink current is disabled and a 10 uA current source causes the voltage at RES pin to gradually increase. In the event of an extended overload condition, the LM5026 protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.5V threshold, the following restart sequence occurs (see [Figure 23](#)):

- The RES capacitor and SS capacitors are fully discharged.
- The soft-start current source is reduced from 50 μ A to 1 μ A
- The SS capacitor voltage slowly increases. When the SS voltage reaches 1.4V, the PWM comparator will produce the first output pulse. After the first pulse occurs, the SS source current reverts to the normal 50 μ A level. The SS voltage increases at its normal rate gradually increasing the duty cycle of the output drivers
- If the overload condition persists after restart, cycle-by-cycle current limiting will cause the voltage on the RES capacitor to increase again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 10 μ A current sink and normal operation resumes.

The overload timer function is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-cycle only:** The hiccup mode can be completely disabled by connecting the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup

sequences will occur.

2. **Hiccup only:** The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit.
3. **Delayed Hiccup:** The most common configuration as previously described, is a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart. The advantage of this configuration is short term overload conditions will not cause a hiccup mode restart, however during extended overload conditions the average dissipation of the power converter will be very low.
4. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.5V hiccup threshold, the controller will be forced into the delayed restart sequence. If the RES pin is used as an input, the driving source should be current limited to less than 5 mA. For example, the external trigger for a delayed restart sequence could come an over-temperature protection circuit.

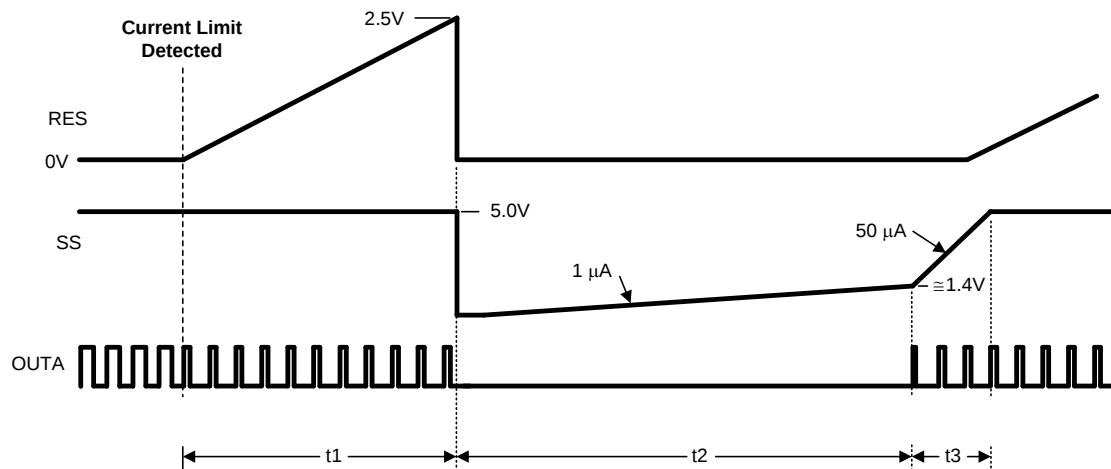


Figure 23. Hiccup Over-Load Restart Timing

Oscillator and Sync Capability

The LM5026 oscillator frequency is set by the external resistance connected between the RT pin and ground (AGND). To set a desired oscillator frequency (F) the necessary value of total R_T resistance can be calculated from:

$$R_T = \frac{1}{F \times 167 \times 10^{-12}} \quad (5)$$

The R_T resistor(s) should be located very close to the device and connected directly to the pins of the IC (RT and AGND).

The SYNC pin can be used to synchronize the internal oscillator to an external clock. An open drain output is the recommended interface between the external clock to the LM5026 SYNC pin as illustrated in Figure 24. The clock pulse width must be greater than 15 ns. The external clock frequency must be a higher than the free running frequency set by the R_T resistance.

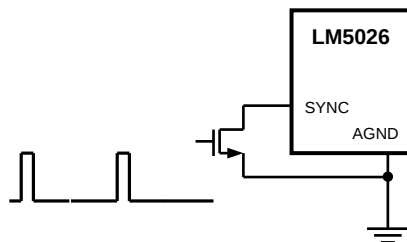


Figure 24. Sync from External Clock

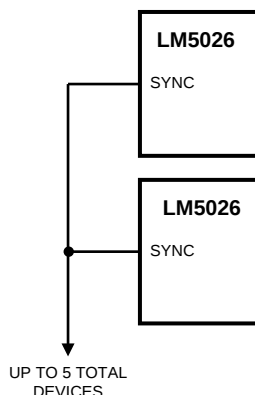


Figure 25. Sync from Multiple Devices

Multiple LM5026 devices can be synchronized together simply by connecting the devices SYNC pins together as shown in [Figure 25](#). Care should be taken to ensure the ground potential differences between devices are minimized. In this configuration all of the devices will be synchronized to the highest frequency device. The internal block diagram of the oscillator and synchronization circuit is shown in [Figure 26](#). The SYNC I/O pin is a CMOS buffer with pull-up current limited to 200 μ A. If an external device forces the SYNC pin low before the internal oscillator ramp completes its charging cycle, the ramp will be reset and another cycle begins. If the SYNC pins of multiple LM5026 devices are connected together, the first SYNC pin that pulls low will reset the oscillator RAMP of all other devices. All controllers will operate in phase when synchronized using the SYNC I/O feature. Up to five LM5026 devices can be synchronized using this technique.

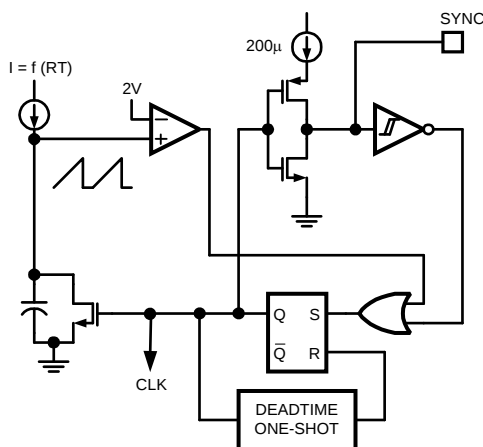


Figure 26. Oscillator Sync I/O Block Diagram

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart after the thermal hysteresis (typically 25°C). During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level.

Applications Information

LINE INPUT (VIN)

The LM5026 contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48V line voltage. The voltage applied to the VIN pin can vary in the range of 13 to 100V with transient capability to 105V. When power is applied and the UVLO pin potential is greater than 0.4V, the VCC regulator is enabled and sources current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.7V, the internal voltage reference (REF) is enabled. The reference regulation set point is 5V. The controller outputs are enabled when the UVLO pin potential is greater than 1.25V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8V to shut off the internal start-up regulator. It is recommended a filtering circuit shown in Figure 27 be used to suppress transients, which may occur at the input supply, in particular when VIN is operated close to the maximum operating rating.

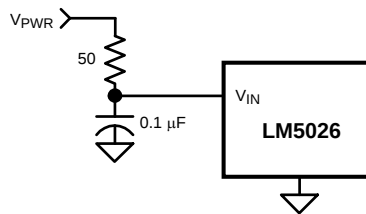


Figure 27. Input Transient Protection

FOR APPLICATION > 100V

For applications where the system input voltage exceed 100V or IC power dissipation is a concern, the LM5026 can be powered from an external start-up regulator as shown in Figure 28. In this configuration, the VIN and the VCC pins should be connected together, which allows the LM5026 to be operated below 13V. The voltage at the VCC pin must be greater than 8V yet not exceed 15V. An auxiliary winding can be used to reduce the dissipation in the external regulator once the power converter is active.

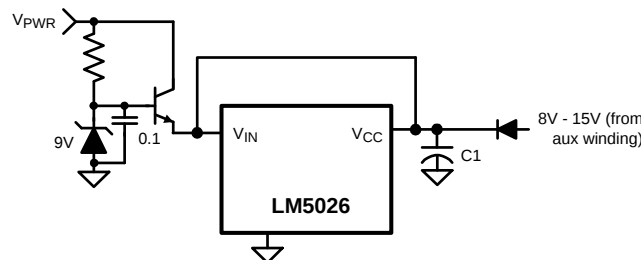


Figure 28. Start-Up Regulator for $V_{PWR} > 100V$

UNDER-VOLTAGE LOCKOUT (UVLO)

When the UVLO pin voltage is below 0.4V the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4V but less than 1.25V the controller is in standby mode. When the UVLO pin voltage is greater than 1.25V the controller is fully enabled. Typically, two external resistors program the minimum operational voltage for the power converter as shown in Figure 29. When UVLO pin voltage is above the 1.25V threshold, an internal 20 μ A current source is enabled to raise the voltage at the UVLO pin, thus providing threshold hysteresis. Resistance values for R1 and R2 can be determined from:

$$R1 = \frac{V_{HYS}}{20\mu A}$$

where

- V_{HYS} is the desired UVLO hysteresis at V_{PWR}

(6)

$$R2 = \frac{1.25 \times R1}{V_{PWR} - 1.25}$$

where

- V_{PWR} is the desired turn-on voltage

(7)

For example, if the LM5026 is to be enabled when V_{PWR} reaches 33V, and disabled when V_{PWR} is decreased to 30V, R1 calculates to 150 k Ω , and R2 calculates to 5.9 k Ω . The voltage at the UVLO pin should not exceed 6V at any time. Be sure to check both the power and voltage rating for the selected R1 resistor.

Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in Figure 30.

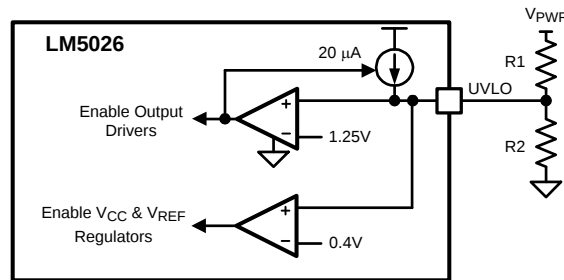


Figure 29. Basic UVLO Configuration

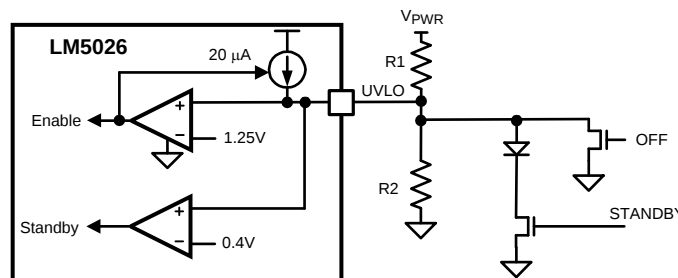


Figure 30. Remote Standby and Disable Control

OSCILLATOR (RT, SYNC)

Oscillator (RT, SYNC) The oscillator frequency is generally selected in conjunction with the design of the system magnetic components along with the volume and efficiency goals for a given power converter design. The total RT resistance at the RT pin sets the oscillator frequency. The RT resistors should be one of the first components placed and connected when designing the PC board. Direct, short connections to each side of the RT resistors (RT, DCL and AGND pins) are recommended.

The SYNC pin can be used to synchronize the internal oscillator to an external clock. An open drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse width should be greater than 15 ns. The external clock must be a **higher frequency** than the free running frequency set by the RT resistor. Multiple LM5026 devices can be synchronized together simply by connecting the devices SYNC pins together. Care should be taken to ensure the ground potential differences between devices are minimized. In this configuration all of the devices will be synchronized to the highest frequency device.

VOLTAGE FEEDBACK (COMP)

The COMP pin is designed to accept the voltage loop feedback error signal from the regulated output via an error amplifier and (typically) an optocoupler. In a typical configuration, VOUT is compared to a precision reference voltage by the error amplifier. The amplifier's output drives the optocoupler, which in turn drives the COMP pin. The parasitic capacitance of the optocoupler often limits the achievable loop bandwidth for a given power converter. The optocoupler LED and detector junction capacitance produce a low frequency pole in the voltage regulation loop. The LM5026 current controlled optocoupler interface (COMP) previously described, greatly increases the pole frequency associated with the optocoupler.

CURRENT SENSE (CS)

The CS pin receives an input signal representative of the transformer primary current, either from a current sense transformer (Figure 31) or from a resistor in series with the source of the primary switch (Figure 32). In both cases the sensed current creates a ramping voltage across R1, while the R_F/C_F filter suppresses noise and transients. R1, R_F and C_F should be as physically close to the LM5026 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current sense components must provide >0.5V at the CS pin when an over-current condition exists.

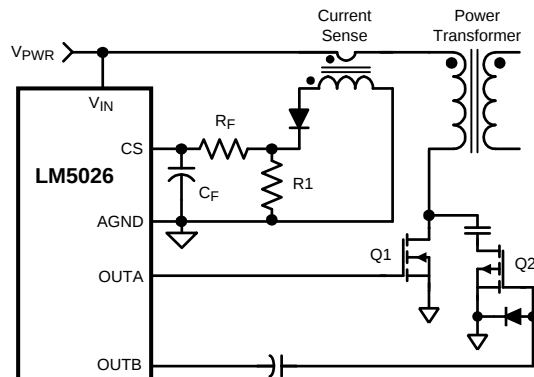


Figure 31. Current Sense Using a Current Sense Transformer

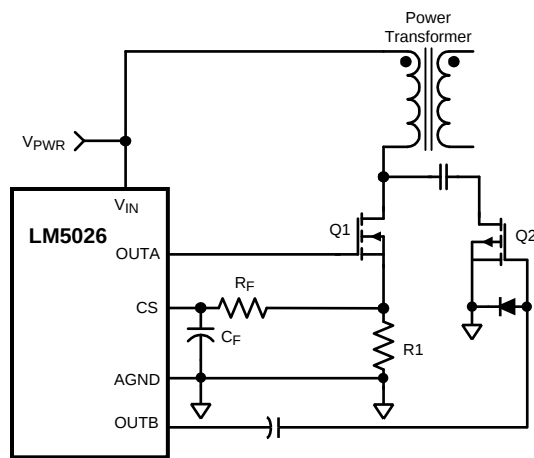


Figure 32. Current Sense Using a Source Sense Resistor (R1)

HICCUP MODE CURRENT LIMIT RESTART (RES)

The basic operation of the hiccup mode current limit restart is described in the functional description. The delay time to restart is programmed with the selection of the RES pin capacitor C_{RES} as illustrated in [Figure 23](#). In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 2.5V hiccup mode threshold is:

$$t1 = \frac{C_{RES} \times 2.5}{10 \mu A} = 2.5 \times 10^5 \times C_{RES} \quad (8)$$

For example, if $C_{RES} = 0.01 \mu F$ the time $t1$ is approximately 2.5 ms.

The cool down time, t_2 is set by the soft-start capacitor (C_{SS}) and the internal 1 μA SS current source, and is equal to:

$$t_2 = \frac{C_{SS} \times 1.4\text{V}}{1 \mu\text{A}} = 1.4 \times 10^6 \times C_{SS} \quad (9)$$

If $C_{SS} = 0.01 \mu\text{F}$, t_2 is $\approx 14 \text{ ms}$.

The soft-start time t_3 is set by the internal 50 μA current source, and is equal to:

$$t_3 = \frac{C_{SS} \times 3.5\text{V}}{50 \mu\text{A}} = 7 \times 10^4 \times C_{SS} \quad (10)$$

The time t_2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This results in lower average input current and lower power dissipated within the power components. It is recommended that the ratio of $t_2/(t_1 + t_3)$ be in the range of 5 to 10 to make good use of this feature. If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode ($t_1 = 0$), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode current limit operation, the RES pin should be connected to ground (AGND).

SOFT-START (SS)

An internal current source and an external soft-start capacitor determines the time required for the output duty cycle to increase from zero to its final value for regulation. The minimum acceptable time is dependent on the output capacitance and the response of the feedback loop. If the soft-start time is too quick, the output could overshoot its intended voltage before the feedback loop can regulate the PWM controller. After power is applied and the controller is fully enabled, the voltage at the SS pin ramps up as C_{SS} is charged by an internal 50 μA current source. The voltage at the output of the COMP pin current mirror is clamped to the same potential as the SS pin by a voltage buffer with a sink-only output stage. When the SS voltage reaches $\approx 1.4\text{V}$, PWM pulses appear at the driver output with very low duty cycle. The PWM duty cycle gradually increases as the voltage at the SS pin charges to $\approx 5.0\text{V}$.

VOLTAGE DEPENDENT MAXIMUM DUTY CYCLE

As the input source V_{PWR} increases the voltage at the UVLO pin increases proportionately. To limit the Volt x Seconds applied to the transformer, the maximum allowed PWM duty cycle decreases as the UVLO voltage increases. If it is desired to increase the slope of the voltage limited duty cycle characteristic, two possible configurations are shown in [Figure 33](#). After the LM5026 is enabled, the zener diode causes the UVLO pin voltage to increase more rapidly with increasing input voltage (V_{PWR}). The voltage dependent maximum duty cycle clamp varies with the UVLO pin voltage according to the following equation:

$$\text{Voltage-Dependent Duty Cycle (\%)} = 107 - 21.8 \times \text{UVLO} \quad (11)$$

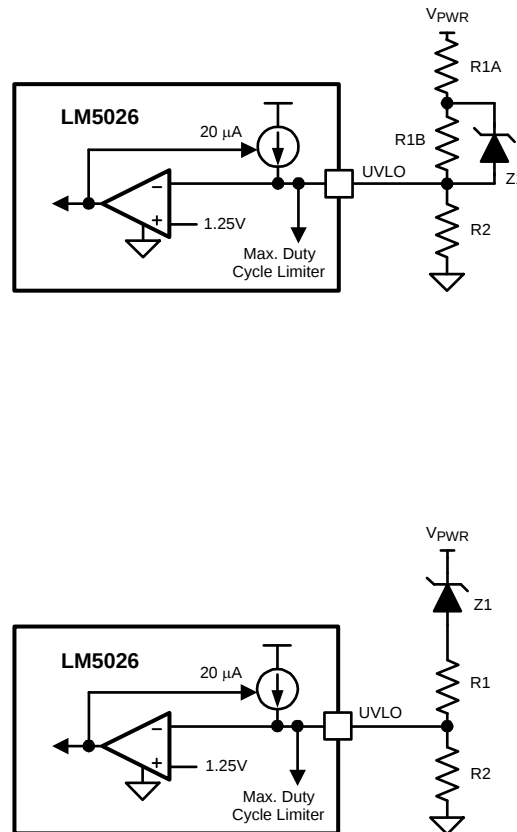


Figure 33. Altering the Slope of Duty Cycle vs. V_{PWR}

Programmable Maximum Duty Cycle Clamp (DCL)

When the UVLO pin is biased at 1.25V (minimum operating level), the maximum duty cycle of OUT_A is limited by the duty cycle of the internal clock signal. The duty cycle of the internal clock can be adjusted by programming a voltage set at the DCL pin. The default maximum duty cycle (80%) can be selected by connecting the DCL pin to the RT pin. The DCL pin should not be left open. A small decoupling capacitor located close to the DCL pin is recommended.

The oscillator frequency set resistance (R_T) must be determined first before programming the maximum duty cycle. Following the selection of the total R_T resistance, the ratio of the R_T resistors can be designed to set the desired maximum duty cycle. As the UVLO pin voltage increases from 1.25V, the maximum duty cycle is reduced by the voltage dependent duty cycle limiter previously as described and illustrated in [Figure 22](#).

Printed Circuit Board Layout

The LM5026 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, DCL, UVLO, TIME, SYNC and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board tracks.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of each transformer should be connected via a dedicated PC board track to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistor should be used. In this case, all the noise sensitive low current ground tracks should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point). The gate drive outputs of the LM5026 should have short direct paths to the power MOSFETs in order to minimize inductance in the PC board traces.

The two ground pins (AGND, PGND) must be connected together with a short direct connection to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM5026 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

Application Circuit Example

The following schematic shows an example of an LM5026 controlled 100W active clamp forward power converter. The input voltage range (V_{PWR}) is 36V to 78V, and the output voltage is 3.3V. The output current capability is 30 Amps. Current sense transformer T2 provides information to the CS pin for current mode control and current limit protection. The error amplifiers and reference U3 and U4 provide voltage feedback via optocoupler U2. Synchronous rectifiers Q3-Q6 minimize rectification losses in the secondary. An auxiliary winding on inductor L2 provides power to the LM5026 VCC pin when the output is in regulation. The input voltage UVLO levels are $\approx 34V$ for increasing V_{PWR} , and $\approx 32V$ for decreasing V_{PWR} . The circuit can be shut down by forcing the ON/OFF input (J2) below 1.25V. An external synchronizing frequency can be applied to the SYNC input (J11) or like converters can be self-synchronized by connections of (J3). The regulator output is current limited at $\approx 32A$.



REVISION HISTORY

Changes from Revision C (April 2013) to Revision D

Page

- Changed layout of National Data Sheet to TI format [23](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5026MT	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 125	LM5026 MT	
LM5026MT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5026 MT	Samples
LM5026MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-1-260C-UNLIM	-40 to 125	LM5026 MT	Samples
LM5026SD/NOPB	ACTIVE	WSO	NHQ	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5026SD	Samples
LM5026SDX/NOPB	ACTIVE	WSO	NHQ	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5026SD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5026MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM5026SD/NOPB	WSO	NHQ	16	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM5026SDX/NOPB	WSO	NHQ	16	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

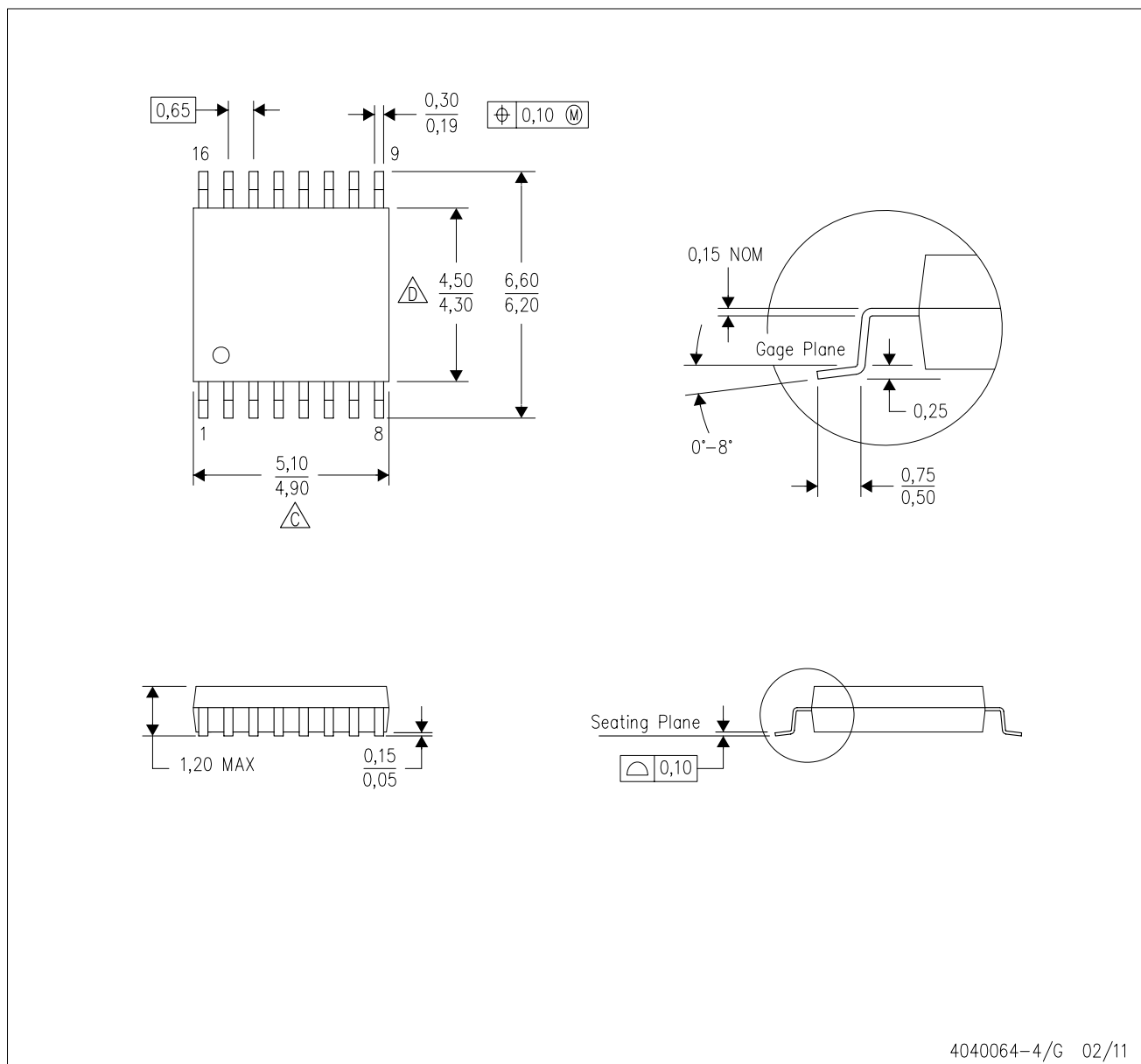


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5026MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5026SD/NOPB	WSO	NHQ	16	1000	210.0	185.0	35.0
LM5026SDX/NOPB	WSO	NHQ	16	4500	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



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