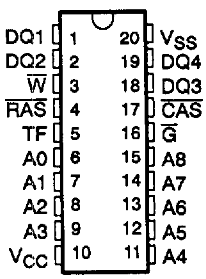
- **Organization . . . 262144 Words × 4 Bits**
- **Single 5-V Supply (10% Tolerance)**
- **Processed to MIL-STD-833, Class B**
- **Performance Ranges:**

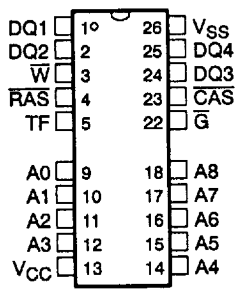
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44C256-80	80 ns	20 ns	40 ns	150 ns
SMJ44C256-10	100 ns	25 ns	45 ns	190 ns
SMJ44C256-12	120 ns	30 ns	55 ns	220 ns
SMJ44C256-15	150 ns	40 ns	70 ns	260 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period 512-Cycle Refresh in 8 ms (Max)**
- **All Inputs and Clocks are TTL Compatible**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Packaging Offered:**
  - **20-Pin 300-Mil Ceramic DIP (JD Suffix)**
  - **20-Lead Ceramic Surface-Mount Package (HJ Suffix)**
  - **20-Pin Ceramic Flat Pack (HK Suffix)**
  - **20-Terminal Leadless Ceramic Surface-Mount Package (FQ Suffix)**
  - **20-Terminal Low-Profile Leadless Ceramic Surface-Mount Package (HL Suffix)**
  - **20-Pin Ceramic Zig Zag In-Line Package (SV Suffix)**
- **Operating Free-Air Temperature Range – 55°C to 125°C**

JD PACKAGE (TOP VIEW)

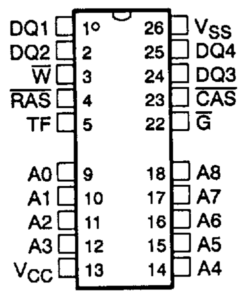


HJ PACKAGE (TOP VIEW)

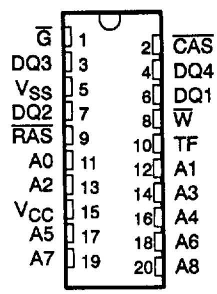


PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{G}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
TF	Test Function
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

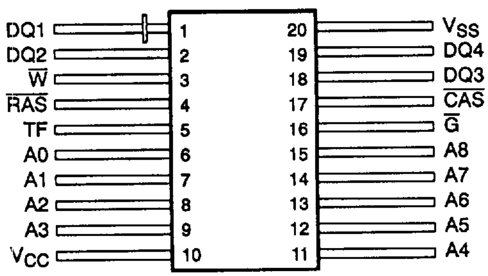
FQ/HL PACKAGES (TOP VIEW)



SV PACKAGE (TOP VIEW)



HK PACKAGE (TOP VIEW)



EPIC is a trademark of Texas Instruments Incorporated.

description

The SMJ44C256 series is a set of high-speed, 1 048 576-bit dynamic random access memories (DRAMs), organized as 262 144 words of four bits each. These devices employ EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power.

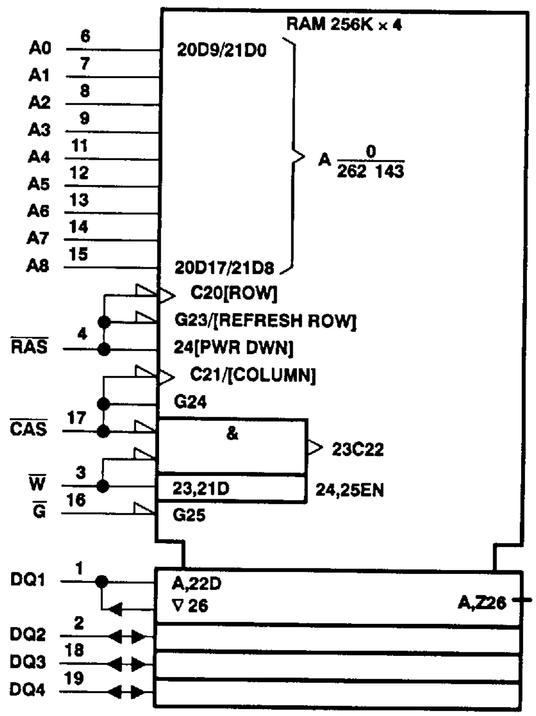
These devices feature maximum RAS access times of 80 ns, 100 ns,120 ns, and 150 ns. Maximum power dissipation is as low as 305 mW operating and 16.5 mW standby on 150-ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and an input voltage undershoot of –1 V can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54/174 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ44C256 is offered in 20-pin ceramic dual-in-line packages (JD suffix) and 20/26-terminal ceramic leadless carriers (FQ/HL suffixes), 20/26-pin leaded carrier (HJ suffix), a 20-pin flatpack (HK suffix), and a 20-pin ceramic zig-zag in-line package (SV suffix). They are specified for operation from –55°C to125°C.

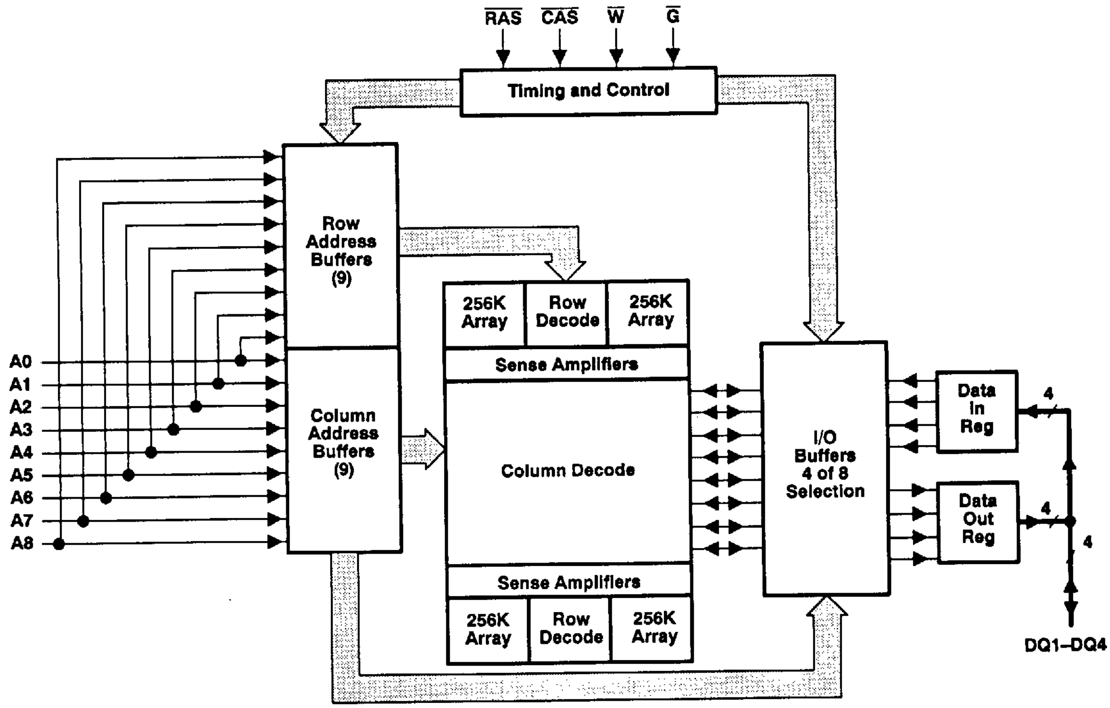
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the JD package.

EPIC is a trademark of Texas Instruments Incorporated.

functional block diagram



operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The column address latches to the first $\overline{CAS}$ falling edge. This feature allows the SMJ44C256 to operate at a wider data bandwidth than conventional page mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ maximum (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by $\overline{RAS}$. Nine column-address bits are set up on pins A0 through A8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the SMJ44C256, $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early-write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to the high-impedance state prior to applying data to the I/O lines.

data out (DQ1–DQ4)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{G}$ and $\overline{CAS}$ to be brought low for the output buffers, to go into the low-impedance state. Once in the low-impedance state, they remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 8 ms to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

CBR refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization (refresh) cycles is required after power-up to the full V_{CC} level.

test function pin

During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . 0 V to 7 V
Voltage range on any pin (see Note 1) . . . . – 1 V to 7 V
Short-circuit output current . . . . 50 mA
Continuous total power dissipation . . . . 1 W
Operating free-air temperature range, T_A . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55			°C
T_C	Case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	μA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, $t_{c(rdW)}$ = minimum		80		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only, or CBR)	V_{CC} = 5.5 V, $t_{c(rdW)}$ = minimum, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		75		65		55		50	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, $t_{c(P)}$ = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35		30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		HL/JD/FQ		HJ		HK		SV		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		6		7		8		9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7		7		8		8	pF
$C_{i(W)}$	Input capacitance, write-enable input		7		7		7		7	pF
C_O	Output capacitance		7		9		10		8	pF

NOTE 3: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30		40	ns
$t_{a(CA)}$	Access time from column-address	t_{AA}		40		45		55		70	ns
$t_{a(RL)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120		150	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		20		25		30		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high column precharge	t_{CPA}		40		50		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}		20		25		30		35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}		20		25		30		35	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{G}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read (see Note 6)	t_{RC}	150		190		220		260		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	150		190		220		260		ns
$t_{c(rdW)}$	Cycle time,read-write/read-modify-write	t_{RWC}	225		270		305		355		ns
$t_{c(P)}$	Cycle time, page-mode read or write (see Note 7)	t_{PC}	50		55		65		80		ns
$t_{c(PM)}$	Cycle time, page-mode read-modify-write	t_{PRWC}	115		135		150		175		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	40	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		80		90		100		ns
$t_{w(RL)}$	Pulse duration, nonpage mode $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	150	10 000	ns
$t_{w(RL)P}$	Pulse duration, page mode $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	150	100 000	ns
$t_{w(WL)}$	Pulse duration, write low	t_{WP}	15		15		20		25		ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	5		5		5		5		ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To assure $t_{c(P)}$ min, $t_{su(CA)}$ should be $\geq t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating temperature (continued) (see Note 5)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	t_{CWL}	20		25		30		40		ns
$t_{su(WRH)}$	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	t_{RWL}	20		25		30		40		ns
$t_{h(CA)}$	Hold time, column address after $\overline{CAS}$ low (see Note 10)	t_{CAH}	15		20		20		25		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	15		15		15		15		ns
$t_{h(RLCA)}$	Hold time, column address after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		100		ns
$t_{h(D)}$	Hold time, data after $\overline{CAS}$ low (see Note 10)	t_{DH}	15		20		25		30		ns
$t_{h(RLD)}$	Hold time, data after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		110		ns
$t_{h(WLGL)}$	Hold time, $\overline{G}$ high after $\overline{W}$ low	t_{GH}	20		25		30		40		ns
$t_{h(CHrd)}$	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	t_{RRH}	10		10		10		10		ns
$t_{h(CLW)}$	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		30		ns
$t_{h(RLW)}$	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 12)	t_{WCR}	65		75		90		105		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 15)	t_{CWD}	60		70		80		90		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	t_{RCD}	30	60	30	75	30	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 13)	t_{RAD}	20	40	20	55	20	65	25	80	ns

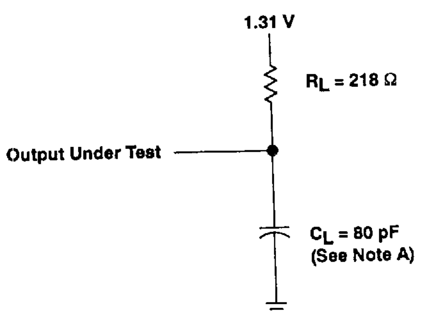
NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early-write operation only
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Maximum value specified only to assure access time.
14. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
15. Read-modify-write operation only

timing requirements over recommended ranges of supply voltage and operating temperature (continued) (see Note 5)

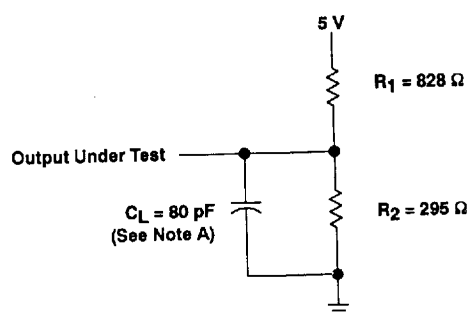
PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	40		45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	40		45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	t_{RWD}	130		150		170		200		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 15)	t_{AWD}	80		95		105		120		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	20		25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		30		40		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time (see Note 17)	t_T									ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
15. Read-modify-write operation only
16. CBR refresh only
17. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

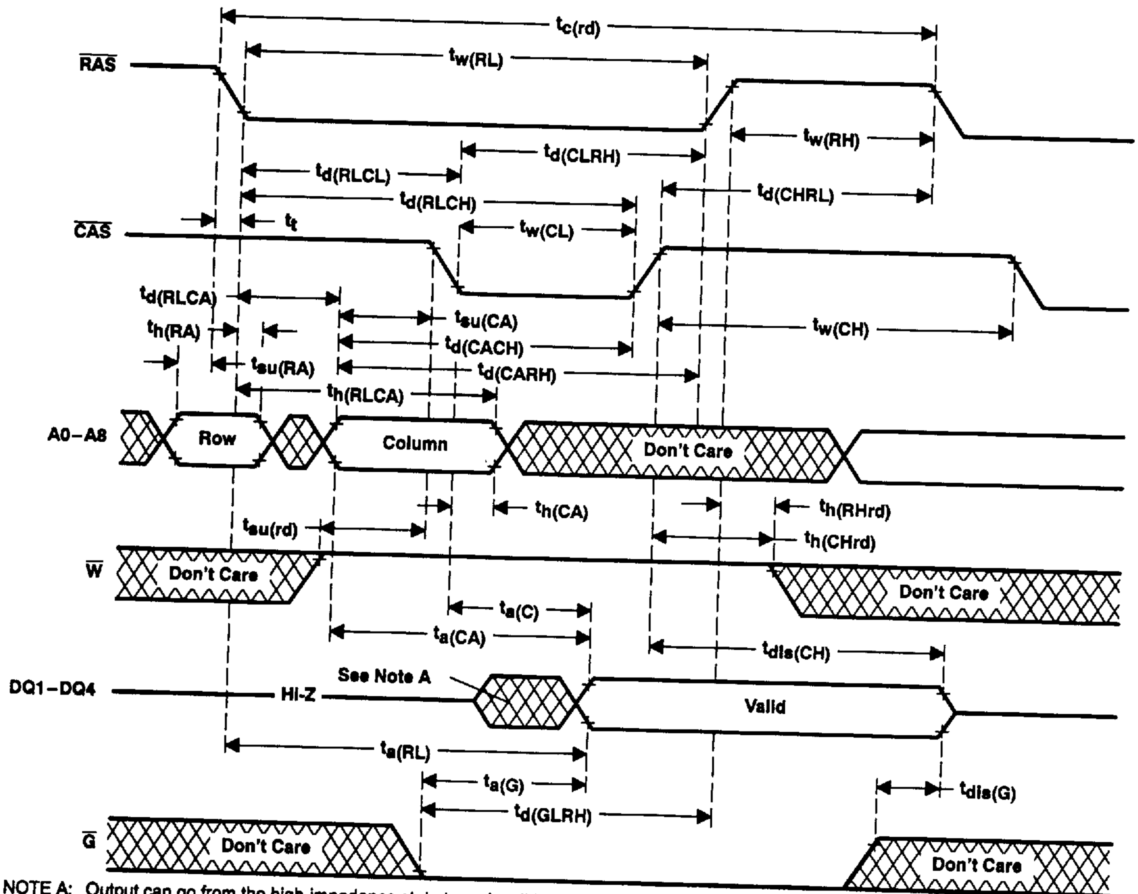


(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

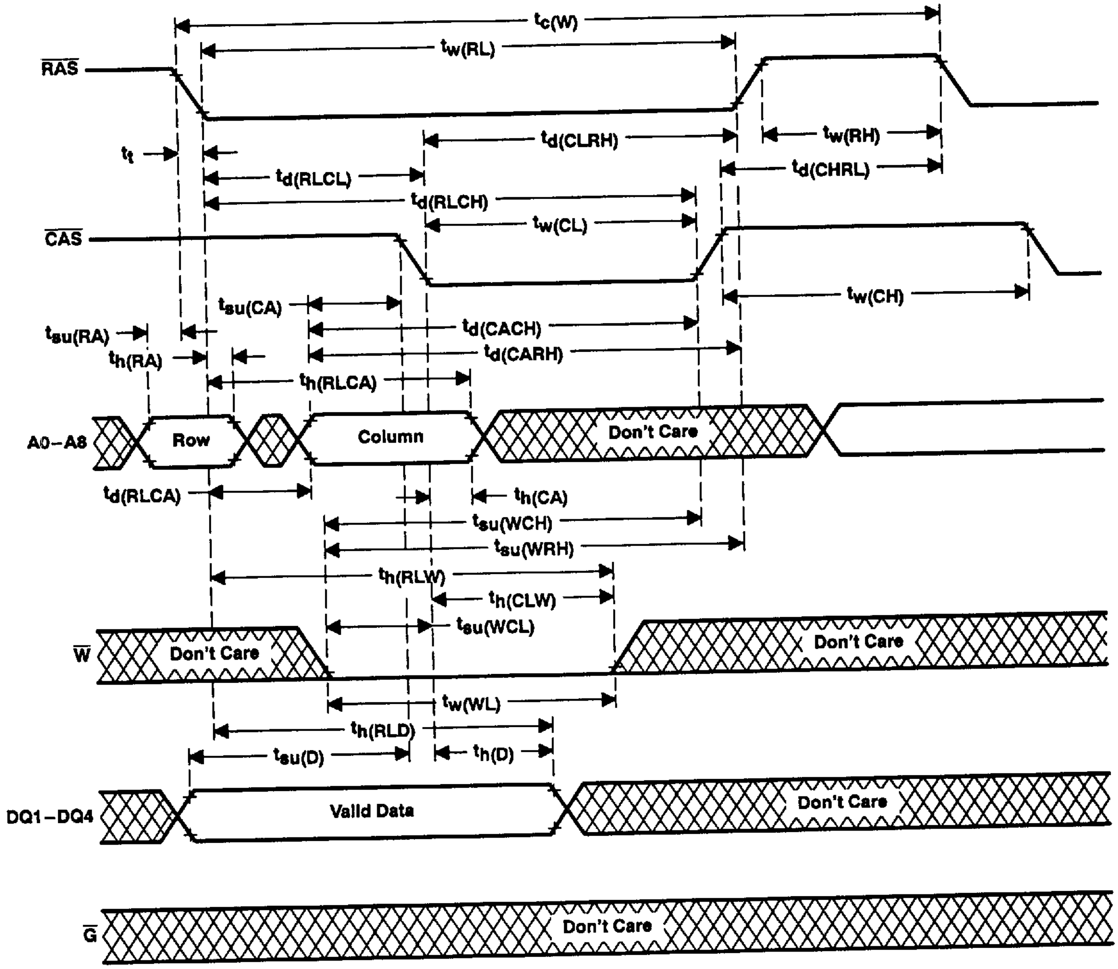


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

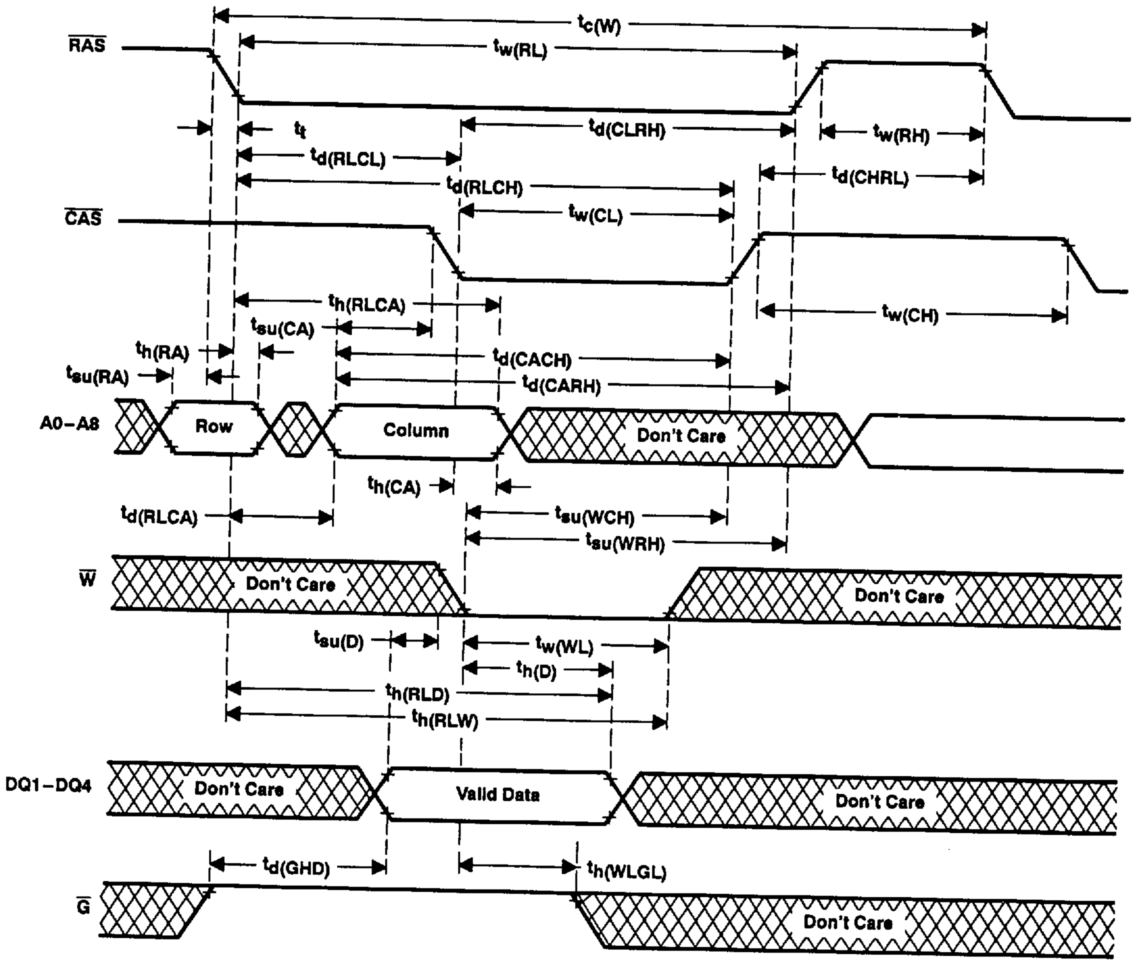
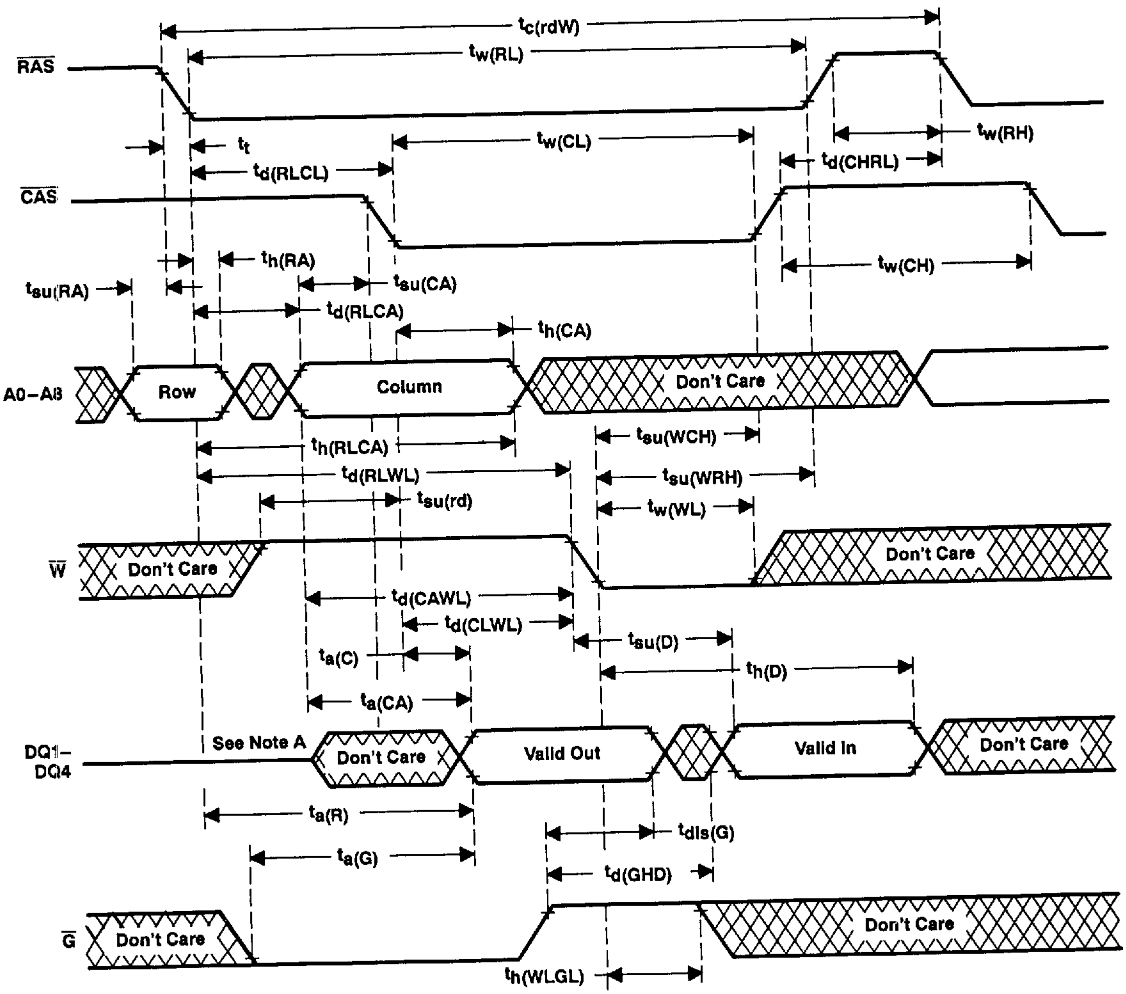


Figure 4. Write-Cycle Timing

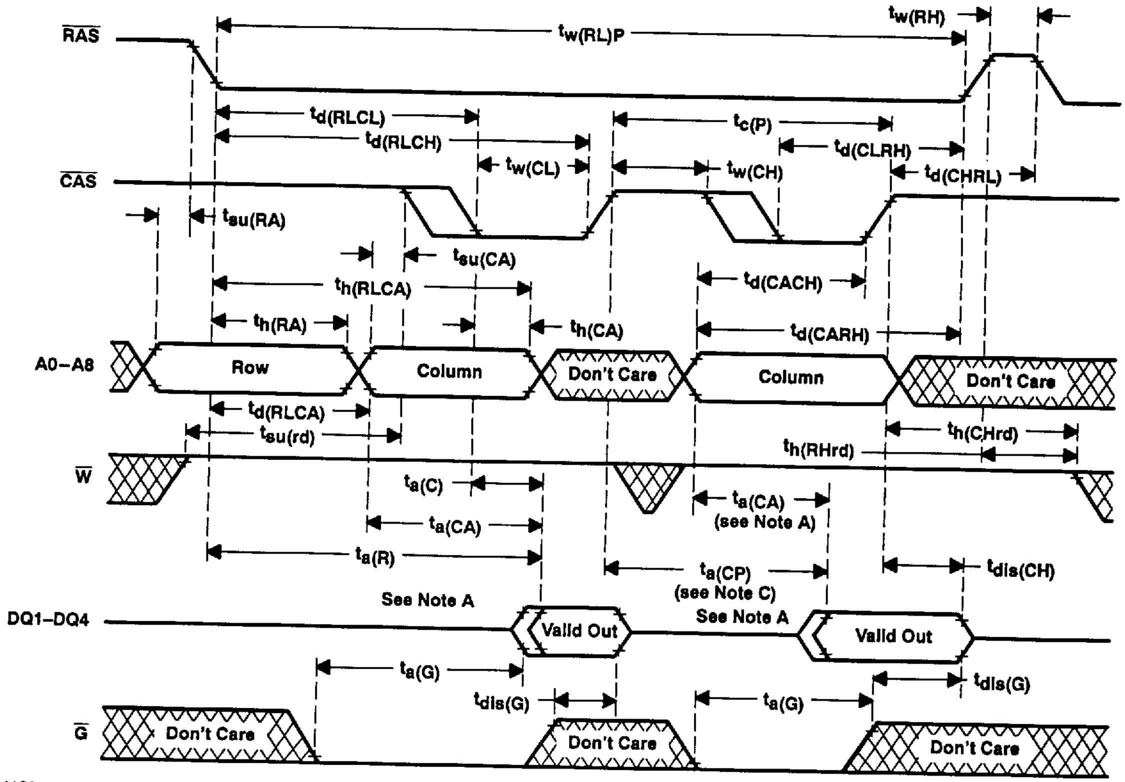
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-/Read-Modify-Write-Cycle Timing

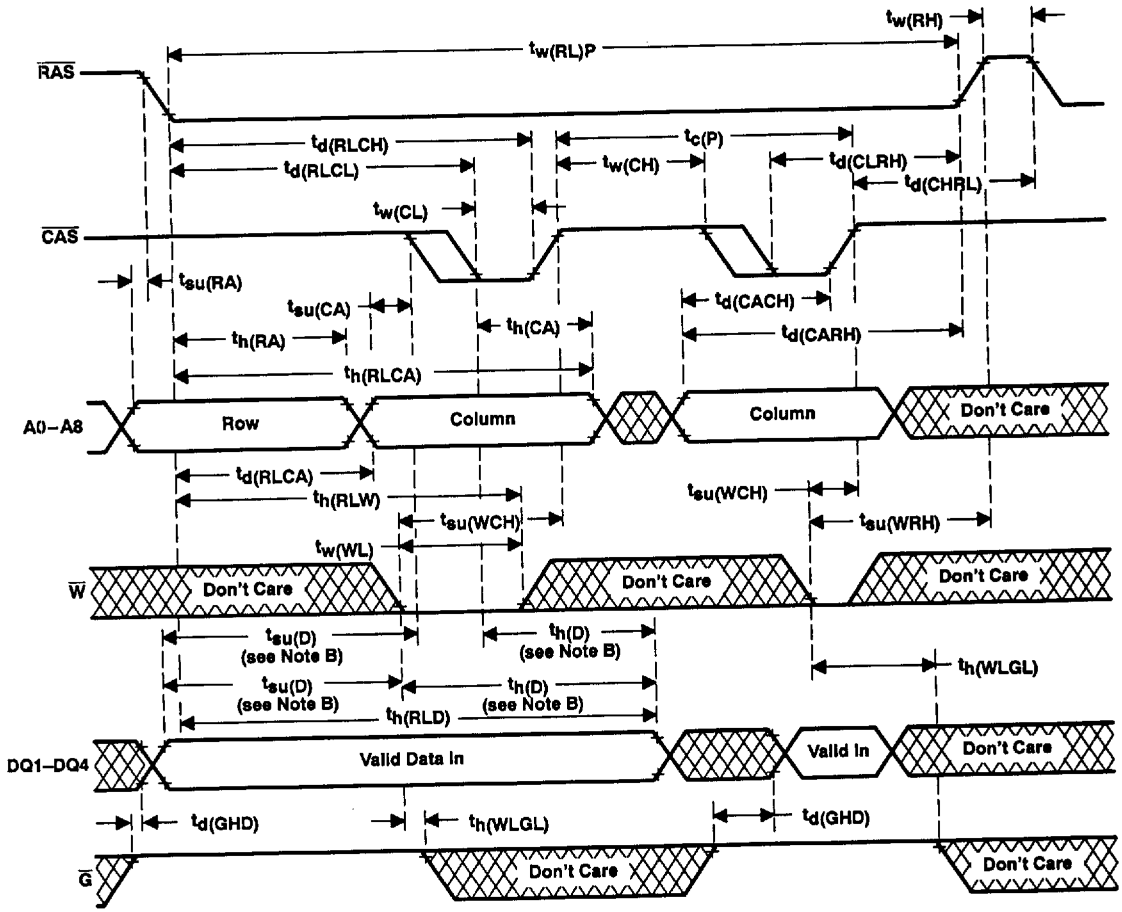
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A write-cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is $t_{a(CP)}$- or $t_{a(CA)}$-dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

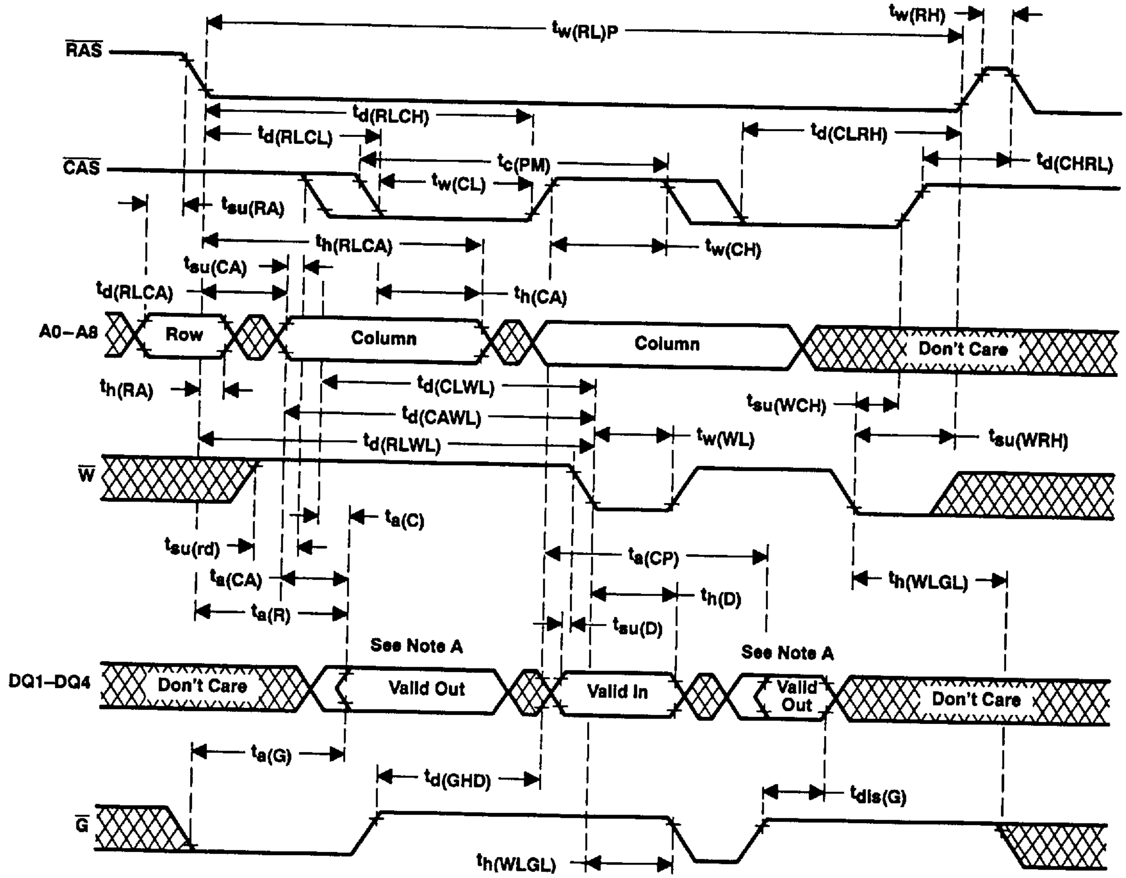


NOTES: A. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

B. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing (see Note A)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing (see Note B)

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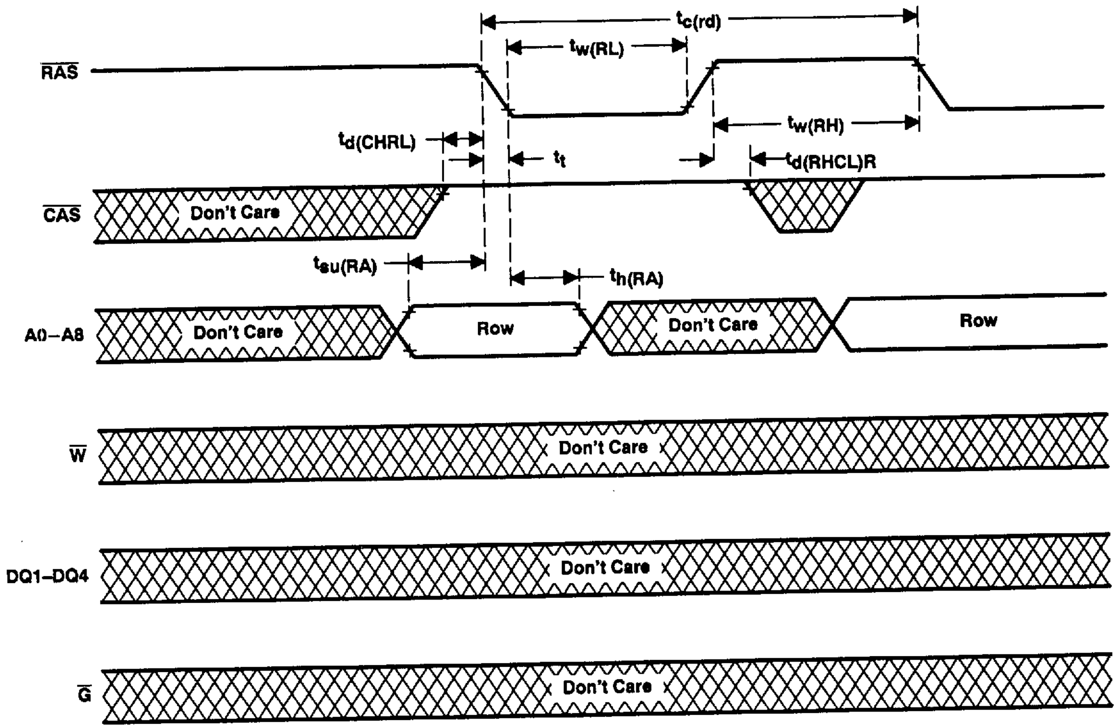

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

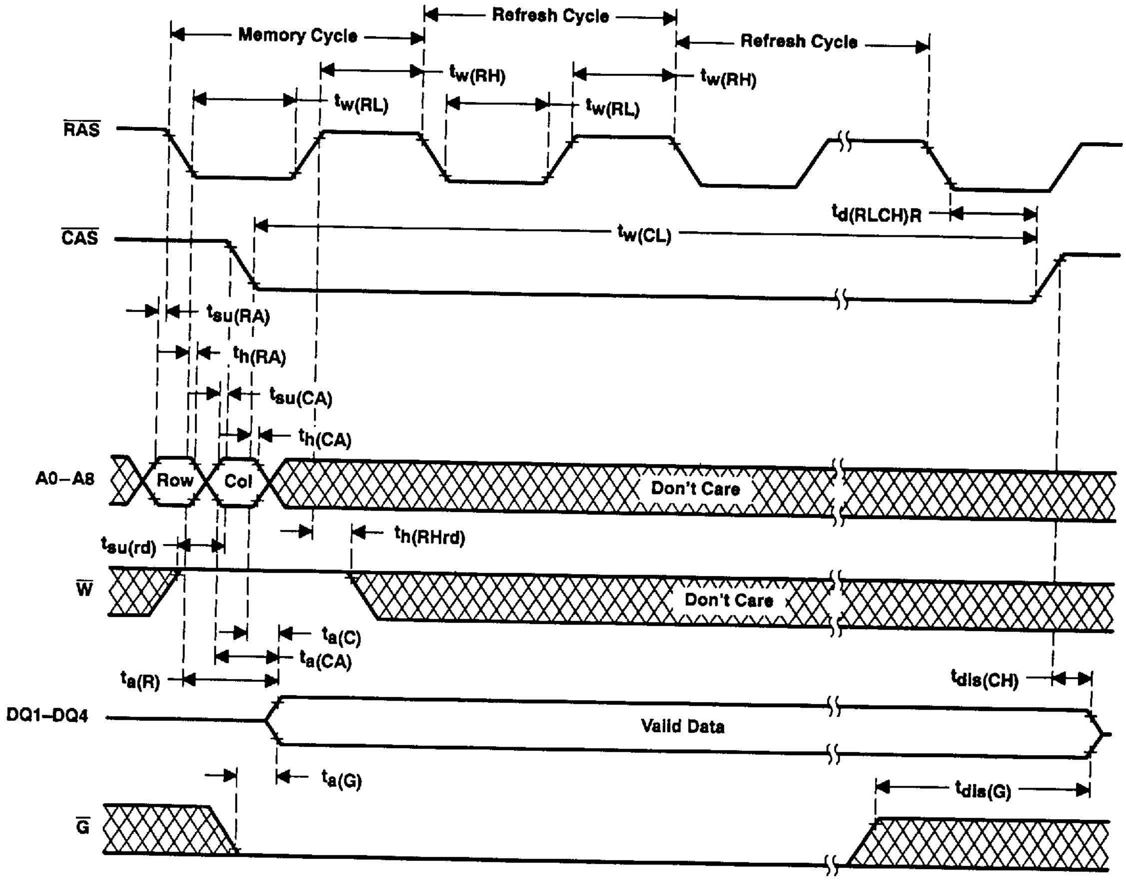

Figure 10. Hidden-Refresh-Cycle (Enhanced Page Mode) Timing

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PARAMETER MEASUREMENT INFORMATION

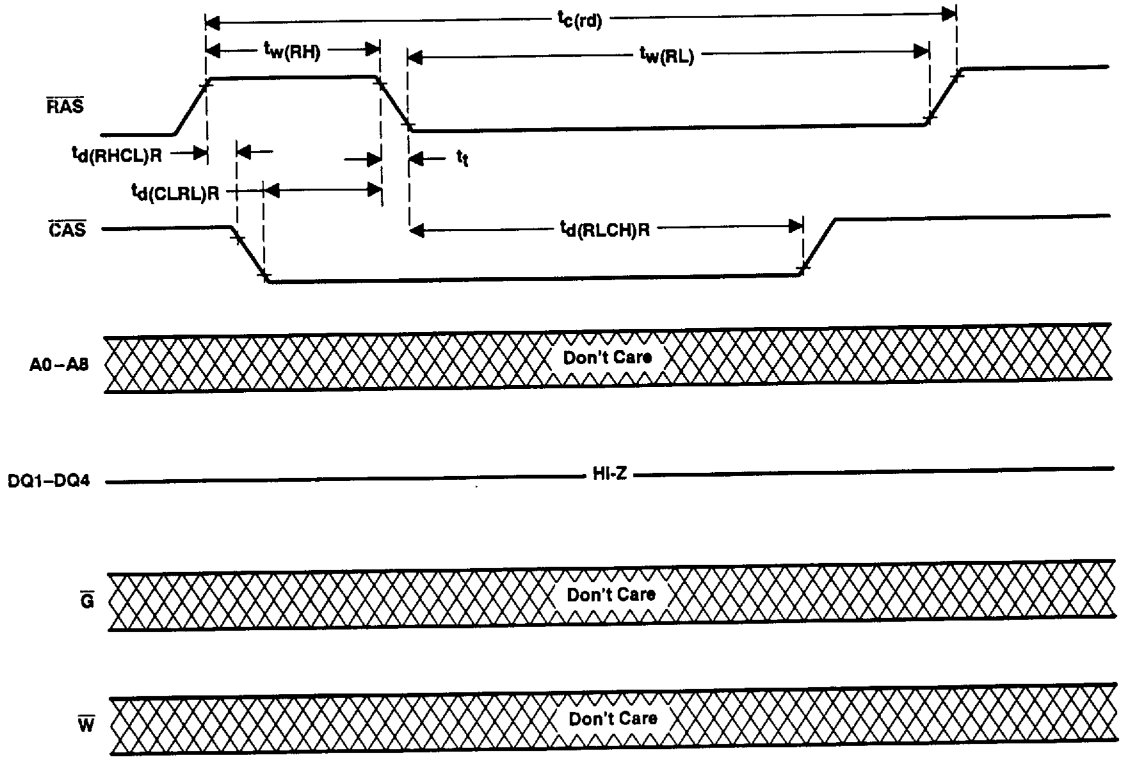

Figure 11. Automatic CBR Refresh-Cycle Timing