

54F194,74F194

54F194 4-Bit Bidirectional Universal Shift Register



Literature Number: SNOS171A

54F/74F194 4-Bit Bidirectional Universal Shift Register

General Description

The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

Features

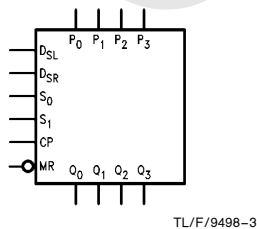
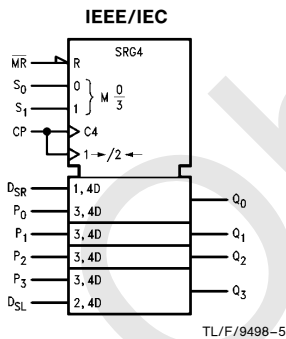
- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

Commercial	Military	Package Number	Package Description
74F194PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F194DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F194SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F194SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F194FM (Note 2)	W16A	16-Lead Cerpack
	54F194LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

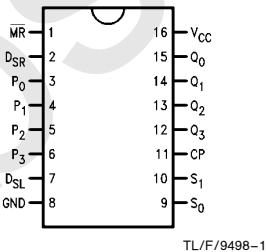
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

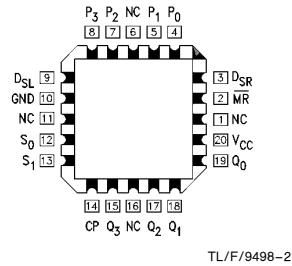


Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



Pin Assignment
for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
S ₀ , S ₁	Mode Control Inputs	1.0/1.0	20 μA/ -0.6 mA
P ₀ -P ₃	Parallel Data Inputs	1.0/1.0	20 μA/ -0.6 mA
D _{SR}	Serial Data Input (Shift Right)	1.0/1.0	20 μA/ -0.6 mA
D _{SL}	Serial Data Input (Shift Left)	1.0/1.0	20 μA/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
\overline{MR}	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
Q ₀ -Q ₃	Parallel Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S₀, S₁) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P₀-P₃) and Serial data (D_{SR}, D_{SL})

inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset (\overline{MR}) overrides all other inputs and forces the outputs LOW.

Mode Select Table

Operating Mode	Inputs						Outputs			
	\overline{MR}	S ₁	S ₀	D _{SR}	D _{SL}	P _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	H	h	l	X	l	X	q ₁	q ₂	q ₃	L
	H	h	l	X	h	X	q ₁	q ₂	q ₃	H
Shift Right	H	l	h	l	X	X	L	q ₀	q ₁	q ₂
	H	l	h	h	X	X	H	q ₀	q ₁	q ₂
Parallel Load	H	h	h	X	X	p _n	p ₀	p ₁	p ₂	p ₃

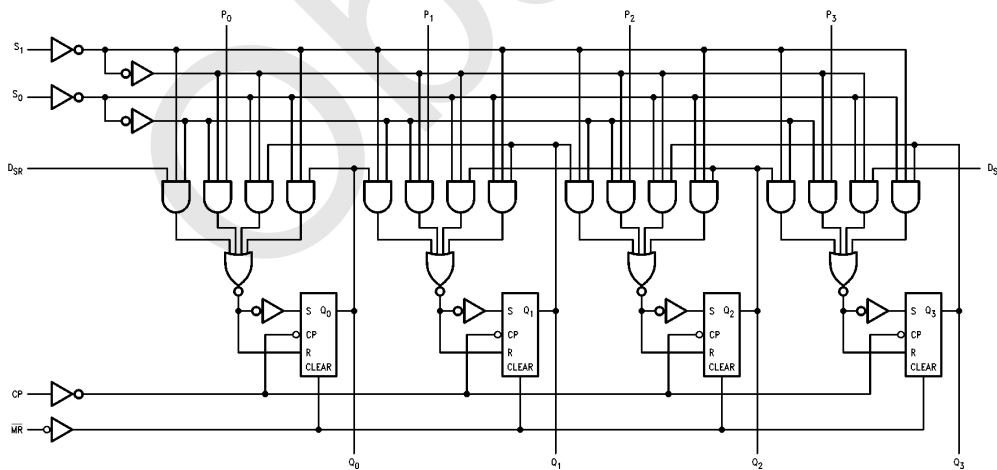
H (h) = High Voltage Level

L (l) = Low Voltage Level

p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

X = Immaterial

Logic Diagram



TL/F/9498-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				
		74F 5% V _{CC}	2.7				
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			
I _{IH}	Input HIGH Current	54F		20.0	μA	Max	V _{IN} = 2.7V
		74F		5.0			
I _{BVI}	Input HIGH Breakdown Test	54F		100	μA	Max	V _{IN} = 7.0V
		74F		7.0			
I _{CEX}	Output HIGH Leakage Current	54F		250	μA	Max	V _{OUT} = V _{CC}
		74F		50			
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current			-60	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		33	46	mA	Max	

AC Electrical Characteristics

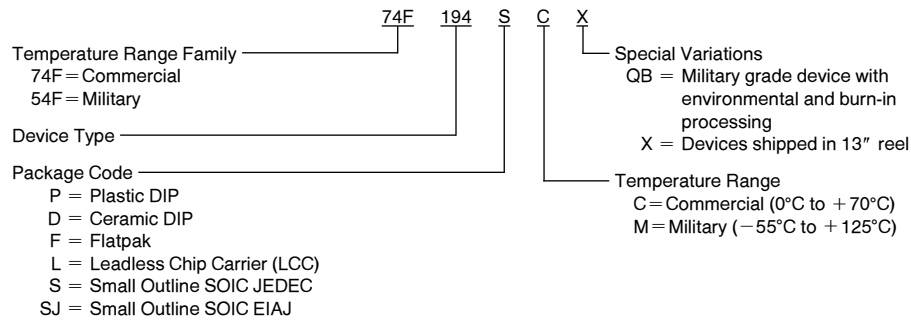
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Shift Frequency	105	150		90		90		MHz
t _{PLH}	Propagation Delay CP to Q _n	3.5	5.2	7.0	3.0	8.5	3.5	8.0	ns
t _{PHL}	Propagation Delay MR to Q _n	3.5	5.5	7.0	3.0	8.5	3.5	8.0	
t _{PHL}	Propagation Delay MR to Q _n	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns

AC Operating Requirements

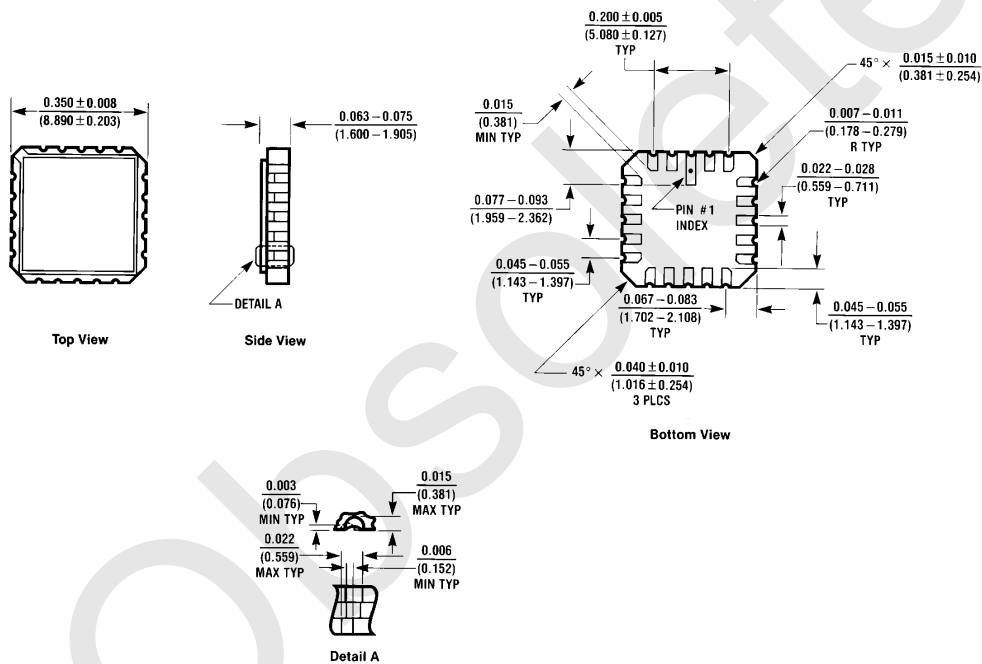
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW P _n or D _{SR} or D _{SL} to CP	4.0		6.0		4.0		ns
t _s (L)		4.0		4.0		4.0		
t _h (H)	Hold Time, HIGH or LOW P _n or D _{SR} or D _{SL} to CP	1.0		1.5		1.0		ns
t _h (L)		0		1.0		1.0		
t _s (H)	Setup Time, HIGH or LOW S _n to CP	10.0		10.5		11.0		ns
t _s (L)		8.0		8.0		8.0		
t _h (H)	Hold Time, HIGH or LOW S _n to CP	0		0		0		ns
t _h (L)		0		0		0		
t _w (H)	CP Pulse Width, HIGH	5.0		5.5		5.5		ns
t _w (L)	MR Pulse Width, LOW	5.0		5.0		5.0		ns
t _{rec}	Recovery Time MR to CP	9.0		9.0		11.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



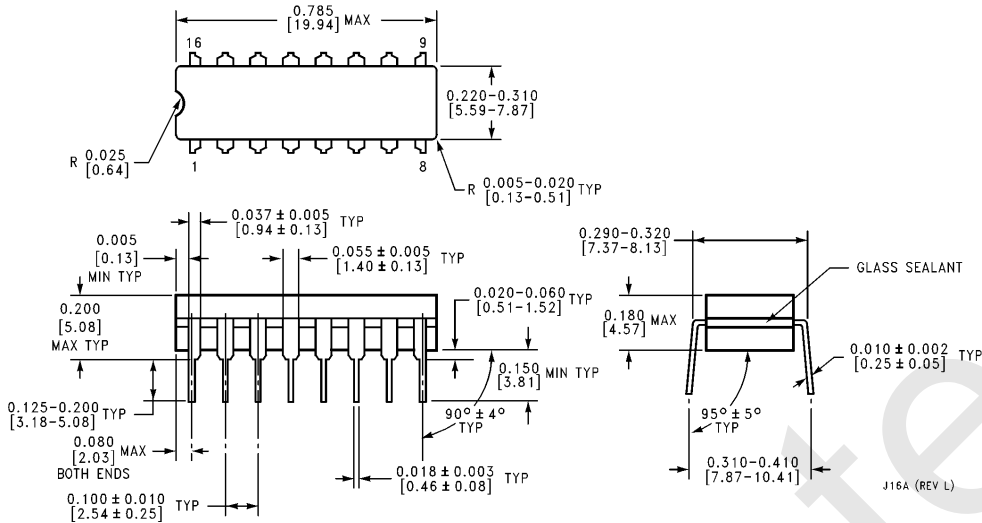
Physical Dimensions inches (millimeters)



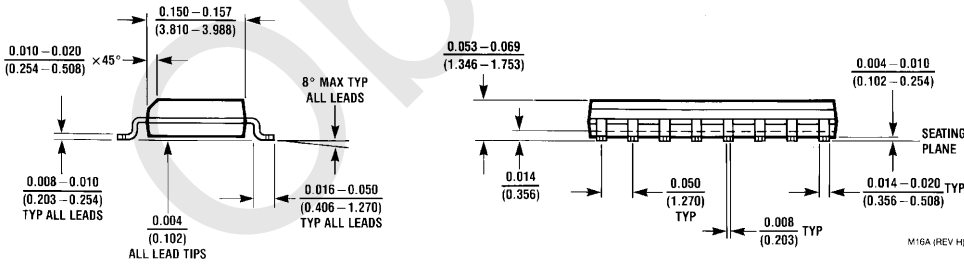
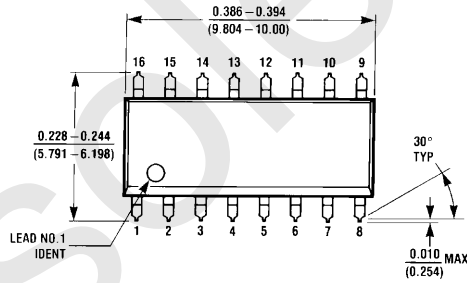
**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

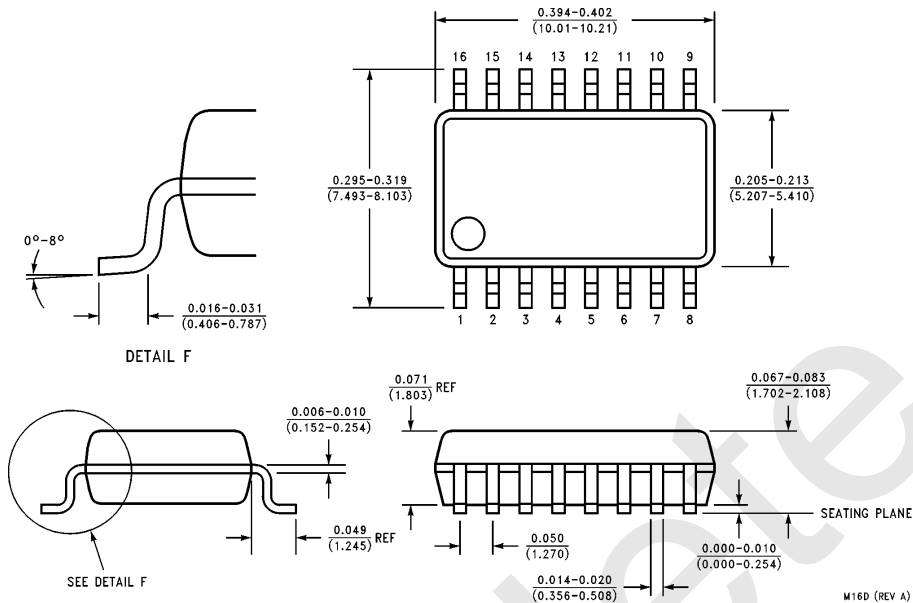


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



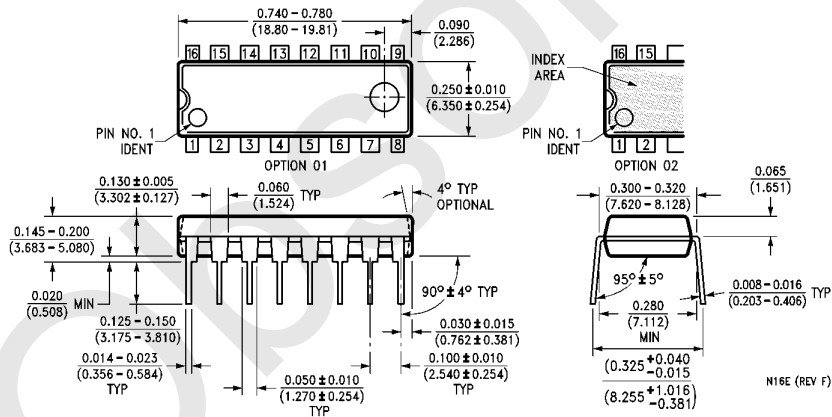
16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

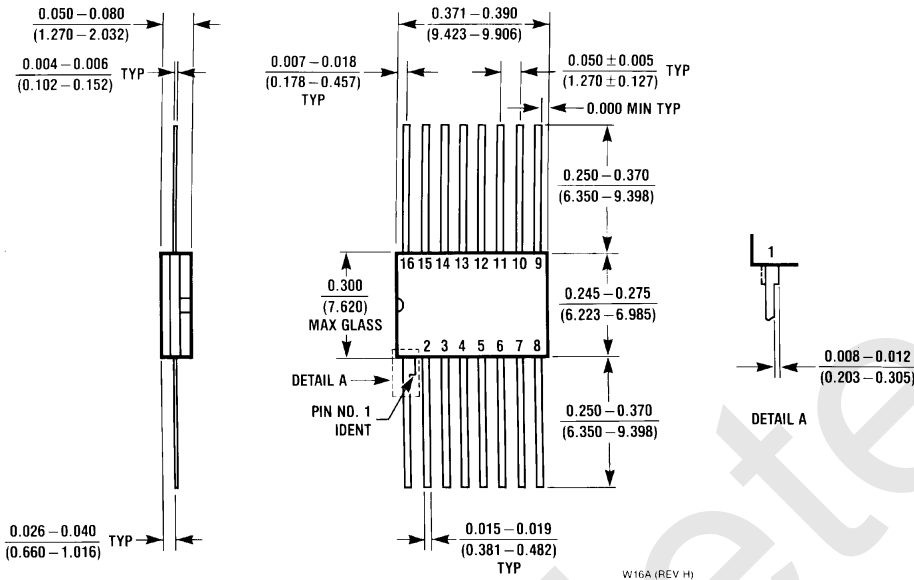
M16D (REV A)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

N16E (REV F)

Physical Dimensions inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**

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