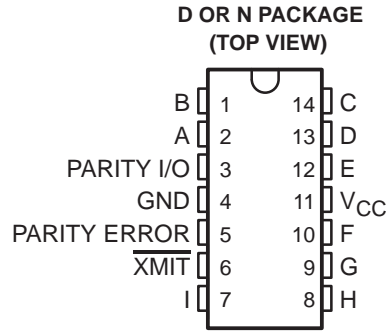


**74AC11286**  
**9-BIT PARITY GENERATOR/CHECKER**  
**WITH BUS DRIVER PARITY I/O PORTS**

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- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs



**description**

The 74AC11286 universal 9-bit parity generator/checker features a local output for parity checking and a bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The  $\overline{XMIT}$  control input is implemented specifically to accommodate cascading. When the  $\overline{XMIT}$  is low, the parity tree is disabled and the PARITY ERROR output will remain at a high logic level regardless of the input levels. When  $\overline{XMIT}$  is high, the parity tree is enabled. The PARITY ERROR output will indicate a parity error when either an even number of inputs (A through I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power up or power down to prevent bus glitches.

The 74AC11286 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{XMIT}$ INPUT	PARITY I/O	PARITY ERROR OUTPUT
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level                      l — low input level  
H — high output level                    L — low output level

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

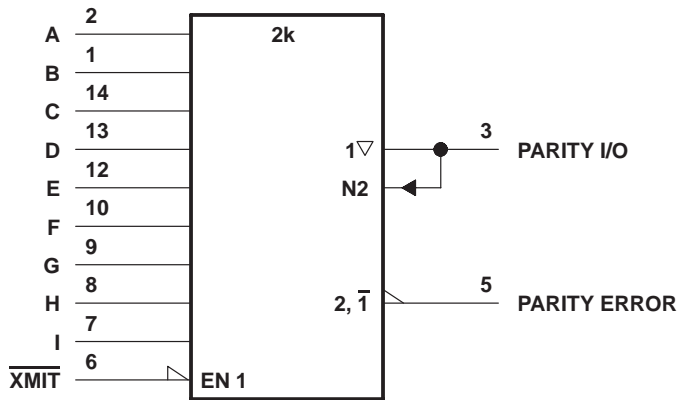
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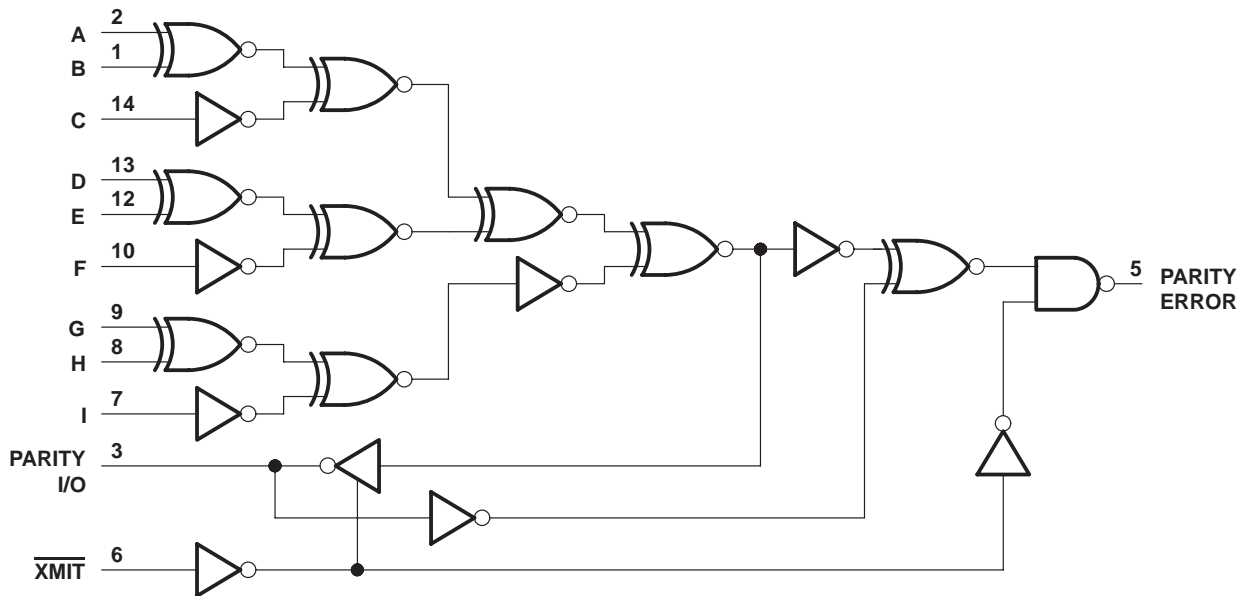
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**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



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74AC11286  
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**recommended operating conditions**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 4.5 V		1.35	
		V <sub>CC</sub> = 5.5 V		1.65	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		-4	mA
		V <sub>CC</sub> = 4.5 V		-24	
		V <sub>CC</sub> = 5.5 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12	mA
		V <sub>CC</sub> = 4.5 V		24	
		V <sub>CC</sub> = 5.5 V		24	
Δt/Δv	Input transition rise or fall rate	0		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9		2.9	V		
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V			3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V		0.1	0.1	V		
		4.5 V		0.1	0.1			
		5.5 V		0.1	0.1			
	I <sub>OL</sub> = 12 mA	3 V		0.36	0.44			
		4.5 V		0.36	0.44			
		5.5 V		0.36	0.44			
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V			1.65				
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.5	± 5	μA		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1	± 1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8	80	μA		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3.5		pF		
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		8.5		pF		

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



# 9-BIT PARITY GENERATOR/CHECKER WITH BUS DRIVER PARITY I/O PORTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ , (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	Any A thru I	PARITY I/O	2.6	10	11.7	2.6	13.1	ns
$t_{PHL}$			3.8	11.6	14.5	3.8	16.1	
$t_{PLH}$	Any A thru I	PARITY ERROR	3	8.5	13.1	3	14.7	ns
$t_{PHL}$			4	10.9	16	4	17.8	
$t_{PLH}$	PARITY I/O	PARITY ERROR	2.2	5.9	7.6	2.2	8.4	ns
$t_{PHL}$			3.4	7.9	10.2	3.4	11.1	
$t_{PZH}$	$\overline{XMIT}$	PARITY I/O	1.8	4.9	6.4	1.8	7	ns
$t_{PZL}$			3.5	9.7	12.8	3.5	13.6	
$t_{PHZ}$	$\overline{XMIT}$	PARITY I/O	3.2	5.4	6.6	3.2	7	ns
$t_{PLZ}$			3.2	5.4	6.7	3.2	7.2	

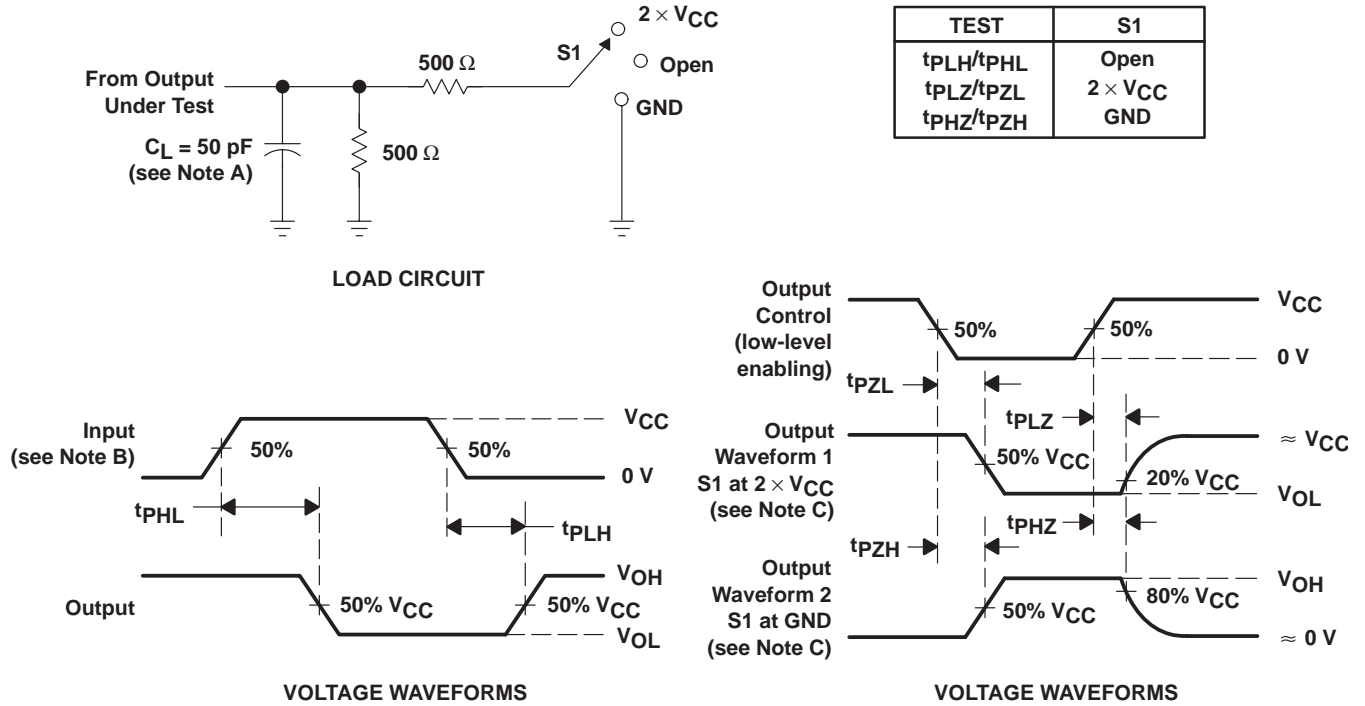
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ , (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	Any A thru I	PARITY I/O	2	5.5	8	2	9	ns
$t_{PHL}$			3.1	6.9	9.1	3.1	10.7	
$t_{PLH}$	Any A thru I	PARITY ERROR	2.5	5.2	8.9	2.5	10	ns
$t_{PHL}$			3.3	6.5	10.7	3.3	12	
$t_{PLH}$	PARITY I/O	PARITY ERROR	1.9	3.9	5.6	1.9	6.2	ns
$t_{PHL}$			2.9	5	7.2	2.9	7.9	
$t_{PZH}$	$\overline{XMIT}$	PARITY I/O	1.4	3.3	4.9	1.4	5.3	ns
$t_{PZL}$			3	5.4	8.3	3	8.9	
$t_{PHZ}$	$\overline{XMIT}$	PARITY I/O	3.1	4.8	6.1	3.1	6.5	ns
$t_{PLZ}$			3	4.6	6	3	6.3	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled	53	pF
		Outputs disabled	46	

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AC11286D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
74AC11286DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
74AC11286N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.





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