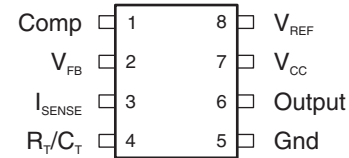


## RAD-TOLERANT CLASS V, CURRENT-MODE PWM CONTROLLER

### FEATURES

- QML-V Qualified, SMD 5962-86704
- Rad-Tolerant: 30 kRad (Si) TID <sup>(1)</sup>
- Optimized for Offline and DC-to-DC Converters
- Low Start-Up Current (<0.5 mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double-Pulse Suppression
- High-Current Totem-Pole Output
- Internally Trimmed Bandgap Reference
- 500-kHz Operation
- Low  $R_O$  Error Amplifier

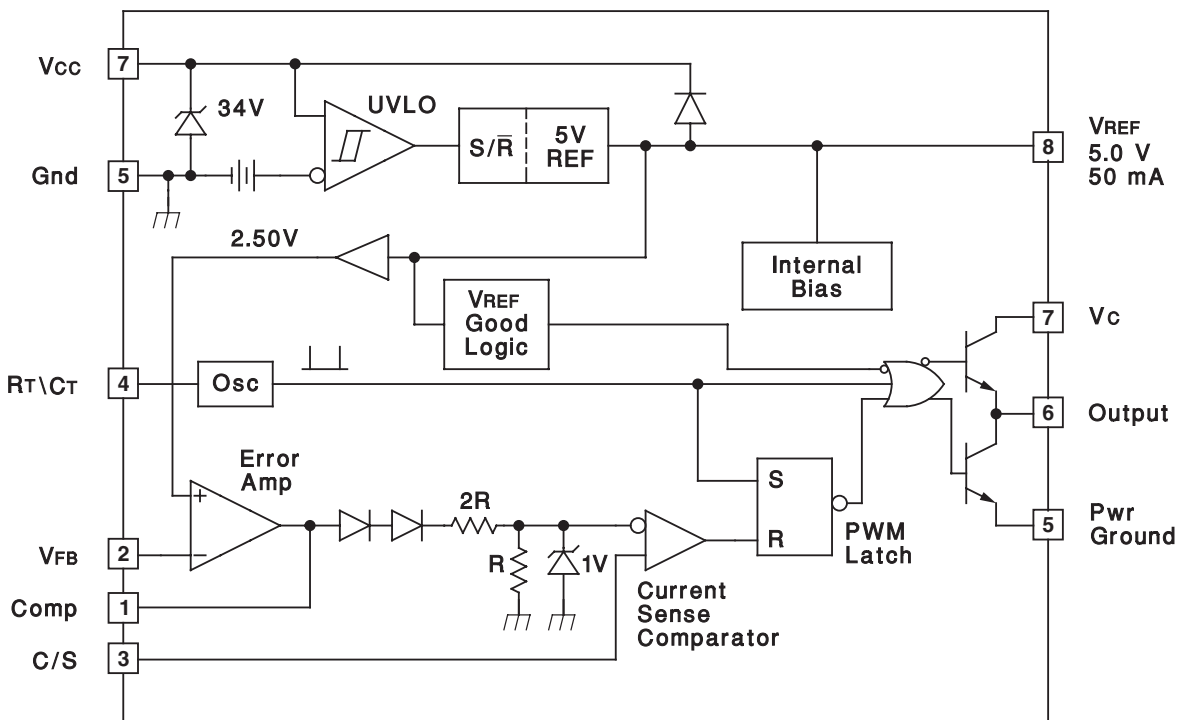
(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

**JG PACKAGE  
(TOP VIEW)**


### DESCRIPTION

The UC1843A control IC is a pin-for-pin compatible improved version of the UC1843. Providing the necessary features to control current-mode switched-mode power supplies, this device has the following improved features. Start up current is guaranteed to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During undervoltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for  $V_{CC}$  over 5 V.

### BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – JG	5962-8670409VPA	UC1843A-SP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

V <sub>CC</sub>	Supply voltage, low-impedance source	30 V
	Supply current	Self limiting
I <sub>O</sub>	Output current	±1 A
	Output energy (capacitive load)	5 μJ
V <sub>I</sub>	Input voltage (V <sub>FB</sub> , I <sub>SENSE</sub> )	–0.3 V to 6.3 V
	Error amplifier output sink current	10 mA
P <sub>D</sub>	Power dissipation (T <sub>A</sub> = 25°C)	1 W
T <sub>stg</sub>	Storage temperature range	–65°C to 150°C
T <sub>lead</sub>	Lead temperature (soldering, 10 seconds)	300°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (T<sub>A</sub> = T<sub>J</sub> = –55°C to 125°C), unless otherwise noted.

	MIN	MAX	UNIT
V <sub>CC</sub> Supply voltage	12	25	V
Sink/source output current (continuous or time average)	0	200	mA
Reference load current	0	20	mA

**ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 15 V, R<sub>T</sub> = 10 kΩ, C<sub>T</sub> = 3.3 nF, T<sub>A</sub> = T<sub>J</sub> = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Reference Section</b>					
Output voltage	T <sub>J</sub> = 25°C, I <sub>O</sub> = 1 mA	4.94	5	5.06	V
Line regulation	V <sub>CC</sub> = 12 V to 25 V		6	20	mV
Load regulation	I <sub>L</sub> = 1 mA to 20 mA		6	25	mV
Total output variation	Over line, load, and temperature	4.9		5.1	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T <sub>J</sub> = 25°C		50		μV
Short-circuit output current		–30	–100	–180	mA
<b>Oscillator Section</b>					
Initial accuracy	T <sub>J</sub> = 25°C	47	52	57	kHz
Voltage stability	V <sub>CC</sub> = 12 V to 25 V		0.2	1	%
Temperature stability	T <sub>J</sub> = –55°C to 125°C		5		%
Amplitude	V <sub>RT/CT</sub> peak to peak		1.7		V
Discharge current <sup>(1)</sup>	T <sub>J</sub> = 25°C, V <sub>RT/CT</sub> = 2 V	7.8	8.3	8.8	mA
	V <sub>RT/CT</sub> = 2 V	7.5		8.8	

- (1) This parameter is measured with R<sub>T</sub> = 10 kΩ to V<sub>REF</sub>. This contributes approximately 300 μA of current to the measurement. The total current flowing into the R<sub>T</sub>/C<sub>T</sub> pin will be approximately 300 μA higher than the measured value.

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{CC} = 15\text{ V}$ ,  $R_T = 10\text{ k}\Omega$ ,  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

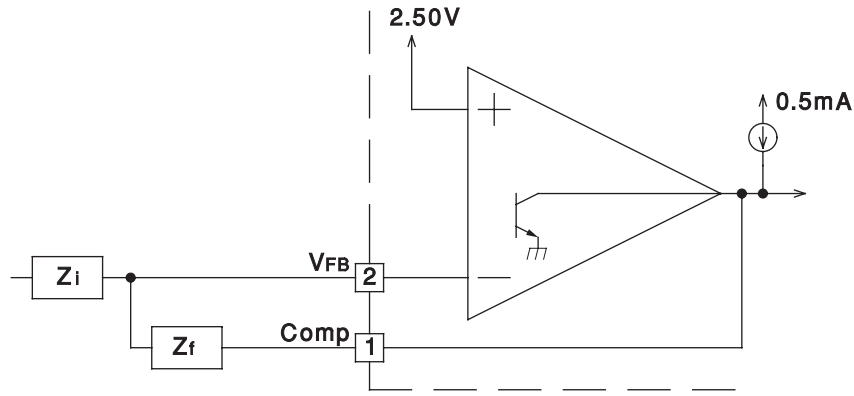
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Error Amp Section</b>					
Input voltage	$V_{Comp} = 2.5\text{ V}$	2.45	2.50	2.55	mV
Input bias current			-0.3	-1	$\mu\text{A}$
Open-loop voltage gain	$V_O = 2\text{ V}$ to $4\text{ V}$	65	90		dB
Unity-gain bandwidth	$T_J = 25^\circ\text{C}^{(2)}$	0.7	1		MHz
PSRR	$V_{CC} = 12\text{ V}$ to $25\text{ V}$	60	70		dB
Output sink current	$V_{FB} = 2.7\text{ V}$ , $V_{Comp} = 1.1\text{ V}$	2	6		mA
Output source current	$V_{FB} = 2.3\text{ V}$ , $V_{Comp} = 5\text{ V}$	-0.5	-0.8		mA
High-level output voltage	$V_{FB} = 2.3\text{ V}$ , $R_L = 15\text{ k}\Omega$ to ground	5	6		V
Low-level output voltage	$V_{FB} = 2.7\text{ V}$ , $R_L = 15\text{ k}\Omega$ to $V_{REF}$		0.7	1.1	V
<b>Current Sense Section</b>					
Gain <sup>(3)(4)</sup>		2.85	3	3.15	V/V
Maximum input signal	$V_{Comp} = 5\text{ V}^{(3)}$	0.9	1	1.1	V
PSRR	$V_{CC} = 12\text{ V}$ to $25\text{ V}^{(3)}$		70		dB
Input bias current			-2	-10	$\mu\text{A}$
Delay to output	$V_{ISENSE} = 0$ to $2\text{ V}^{(2)}$		150	300	ns
<b>Output Section</b>					
Output low-level voltage	$I_{SINK} = 20\text{ mA}$		0.1	0.4	V
	$I_{SINK} = 200\text{ mA}$		1.5	2.2	V
Output high-level voltage	$I_{SOURCE} = 20\text{ mA}$	13	13.5		V
	$I_{SOURCE} = 200\text{ mA}$	12	13.0		V
Rise time	$C_L = 1\text{ nF}$ , $T_J = 25^\circ\text{C}^{(2)}$		50	150	ns
Fall time	$C_L = 1\text{ nF}$ , $T_J = 25^\circ\text{C}^{(2)}$		50	150	ns
UVLO saturation	$V_{CC} = 5\text{ V}$ , $I_{SINK} = 10\text{ mA}$		0.7	1.2	V
<b>Undervoltage Lockout Section</b>					
Start threshold		7.8	8.4	9	V
Minimum operation voltage after turn-on		7	7.6	8.2	V
<b>PWM Section</b>					
Maximum duty cycle		94	96	100	%
Minimum duty cycle				0	%
<b>Total Standby Current</b>					
Start-up current			0.3	0.5	mA
Operating supply current	$V_{FB} = V_{ISENSE} = 0\text{ V}$		11	17	mA
$V_{CC}$ zener voltage	$I_{CC} = 25\text{ mA}$	30	34		V

(2) Parameters ensured by design and/or characterization, if not production tested.

(3) Parameter measured at trip point of latch with  $V_{FB} = 0\text{ V}$ .

(4) Gain defined as:  $G = \Delta V_{Comp} / \Delta V_{ISENSE}$ ;  $V_{ISENSE} = 0$  to  $0.8\text{ V}$ .

APPLICATION INFORMATION



Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Figure 1. Error Amplifier Configuration

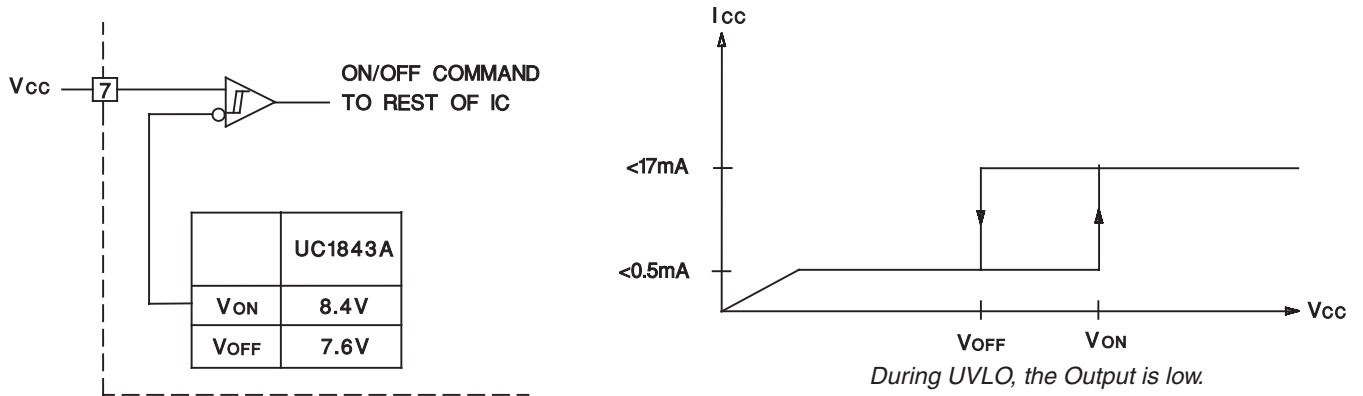
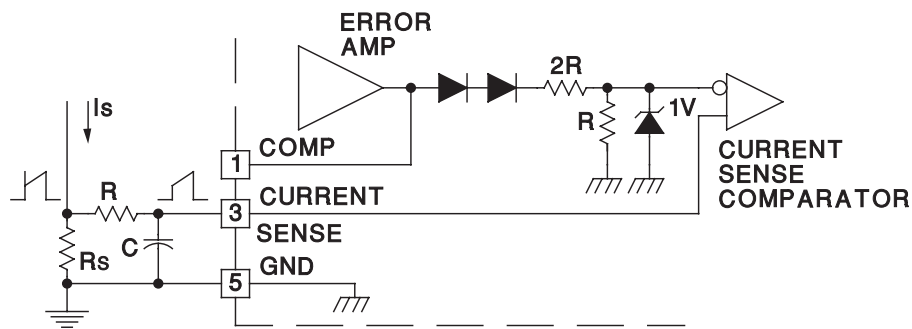


Figure 2. Undervoltage Lockout



Peak Current (Is) is Determined By The Formula

$$I_{SMAX} = \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 3. Current-Sense Circuit

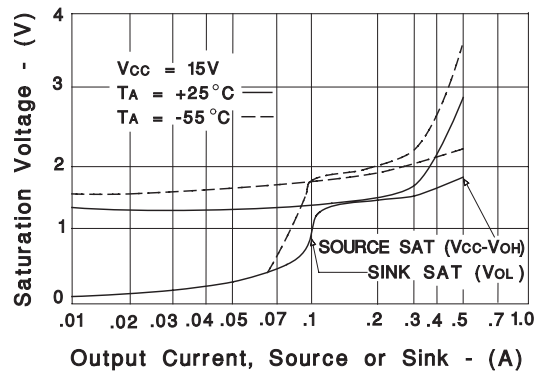


Figure 4. Output Saturation Characteristics

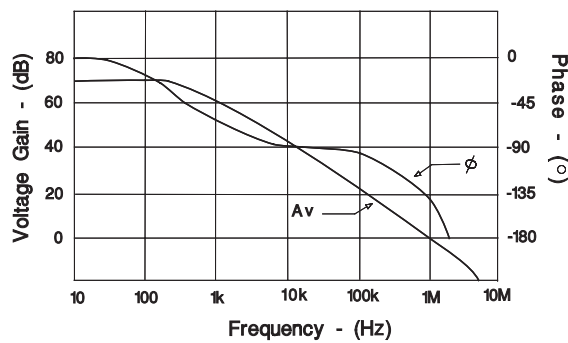
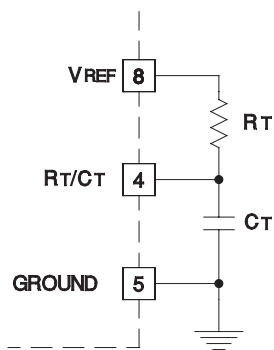


Figure 5. Error Amplifier Open-Loop Frequency Response

Oscillator Frequency vs Timing Resistance

Maximum Duty Cycle vs Timing Resistor



For  $RT > 5k$   $f \approx \frac{1.72}{RTCT}$

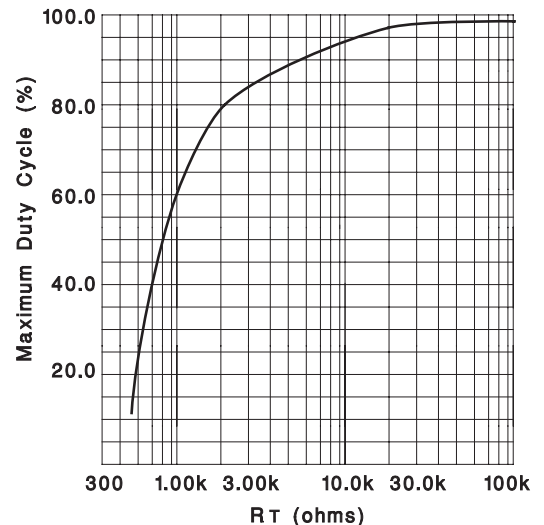
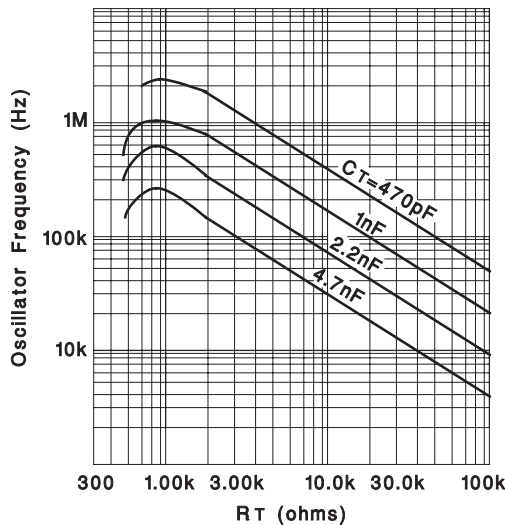
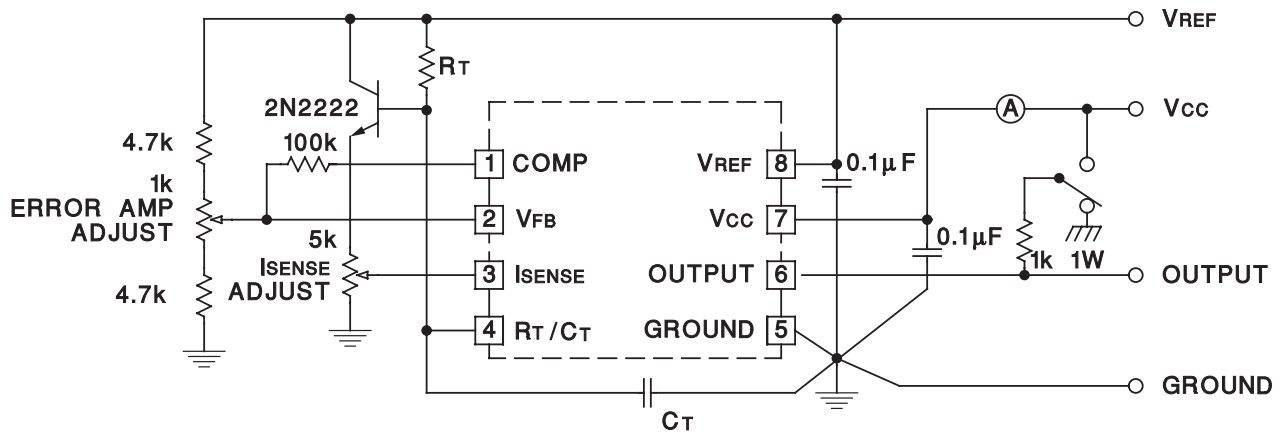


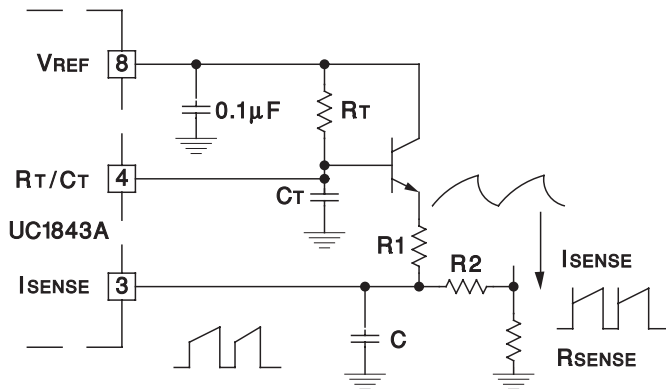
Figure 6. Oscillation Section



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point

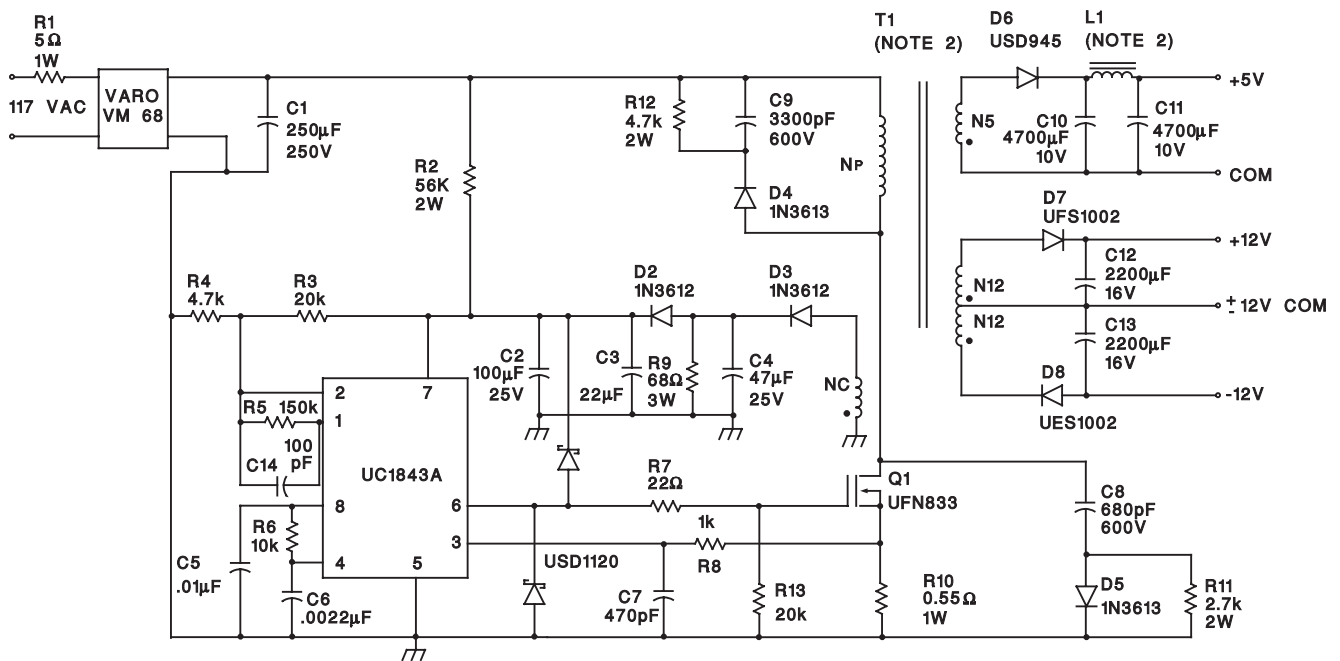
ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 7. Open-Loop Laboratory Test Fixture



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 8. Slope Compensation



Power Supply Specifications

- |                         |                                |
|-------------------------|--------------------------------|
| 1. Input Voltage        | 95VAC to 130VA<br>(50 Hz/60Hz) |
| 2. Line Isolation       | 3750V                          |
| 3. Switching Frequency  | 40kHz                          |
| 4. Efficiency Full Load | 70%                            |

5. Output Voltage:
- |                                 |                               |
|---------------------------------|-------------------------------|
| A. +5V ± 5%; 1A to 4A load      | Ripple voltage: 50mV P-P Max  |
| B. +12V ± 3%; 0.1A to 0.3A load | Ripple voltage: 100mV P-P Max |
| C. -12V ± 3%; 0.1A to 0.3A load | Ripple voltage: 100mV P-P Max |

Figure 9. Offline Flyback Regulator

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8670406VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-8670406VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8670409VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1843AJQMLV	ACTIVE	CDIP	JG	8		TBD	Call TI	Call TI
UC1843ALQMLV	ACTIVE	LCCC	FK	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF UC1843A-SP :**

- Catalog: [UC1843A](#)
- Enhanced Product: [UC1843A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

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