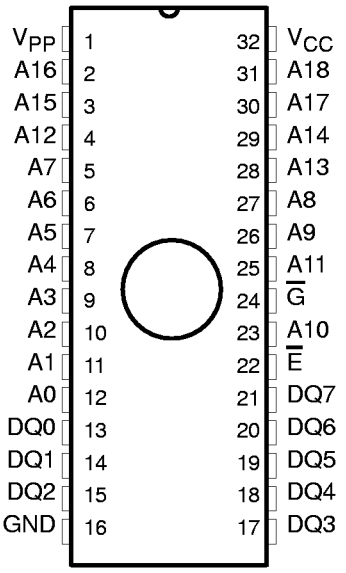
- **Organization . . . 524288 by 8 Bits**
- **Single 5-V Power Supply**
- **Industry Standard 32-Pin Dual-In-line Package**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

'27C040-10	100 ns
'27C040-12	120 ns
'27C040-15	150 ns

- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV DC Assured Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 385 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **Military Operating Temperature Range**
  – 55°C to 125°C

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A18	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply†

† Only in program mode

description

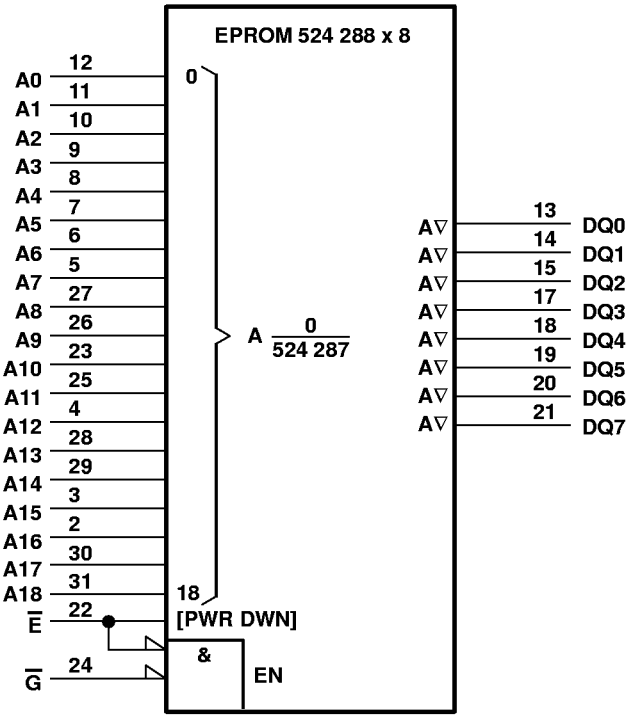
The SMJ27C040 is a set of 4194304-bit, ultraviolet-light erasable, electrically programmable read-only memories (EPROMs).

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits. Each output can drive one Series 54. TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus.

The SMJ27C040 is offered in a 32-pin 600-mil dual-in-line ceramic package (J suffix) rated for operation from – 55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

operation

The seven modes of operation are listed in Table 1. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V)§ on A9 for signature mode.

Table 1. Operation Modes

	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	DQ0–DQ7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	Hi-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	Hi-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	Hi-Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Signature Mode	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_{IH}‡	V_{IL}	MFG Code 97
						V_{IH}	Device Code 50

‡ X can be V_{IL} or V_{IH}.
§ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more SMJ27C040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins. Output data is accessed at pins Q0–Q7.

latchup immunity

Latchup immunity on the SMJ27C040 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 70 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The SMJ27C040 and TMS27PC040 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ1 through DQ8. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{G}$ high, then $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the SMJ27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown in Table 2.

Table 2. Signature Modes

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

† $\overline{E}$ = $\overline{G}$ = V_{IL}, A1–A8 = V_{IL}, A9 = V_H, A10–A18 = V_{IL}, V_{PP} = V_{CC}.

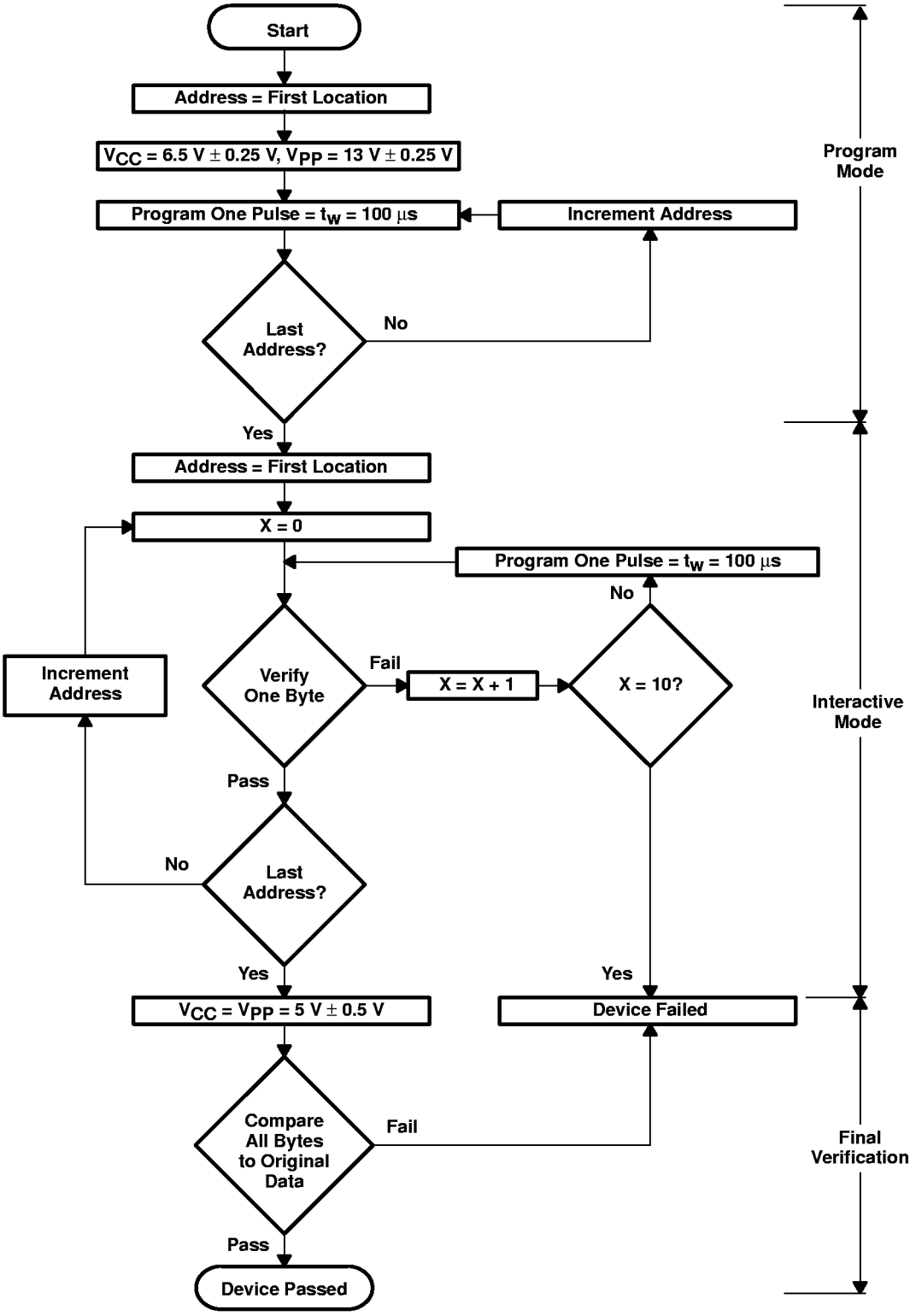


Figure 1. SNAP! Pulse Programming Flow Chart

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13 V
Output voltage range, with respect to V_{SS} (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	8	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		V_{CC} – 0.6		V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.2		V_{CC}+0.5	
V_{IL}	Low-level input voltage		TTL	– 0.5		0.8	V
			CMOS	– 0.5		0.2	
T_A	Operating free-air temperature			– 55			°C
T_C	Operating case temperature					125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 400 µA	2.4		V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		V_{PP} = 12.75 V, T_A – 25°C		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V t_{cycle} = minimum cycle time, outputs open (see Note 5)		50	mA

NOTES: 4. This parameter is only sampled and not 100% tested.
5. Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (V_{CC} = V_{PP} = 5 V ± 0.5 V)†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	8	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Capacitance is sampled only at initial design and after any major change.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 7 and 8)

PARAMETER		TEST CONDITIONS (SEE NOTE 6 AND 7)	'27C040-10		'27C040-12		'27C040-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 2) Input $t_r \le 20$ ns Input $t_f \le 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first (see Note 8)		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first (see Note 8)		0		0		0		ns

NOTES: 6. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Figure 2)
7. Common test conditions apply for t_{dis} except during programming.
8. Value calculated from 0.5-V delta to measured output level. This parameter is only sampled and not 100% tested.

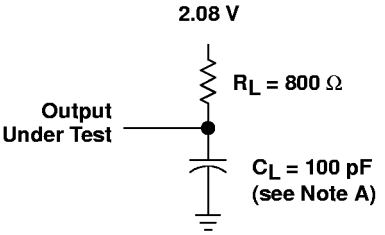
switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

timing requirements for programming

			MIN	TYP	MAX	UNIT
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

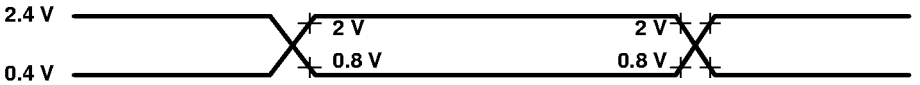


Figure 2. Output Load Circuit and Input/Output Wave Forms

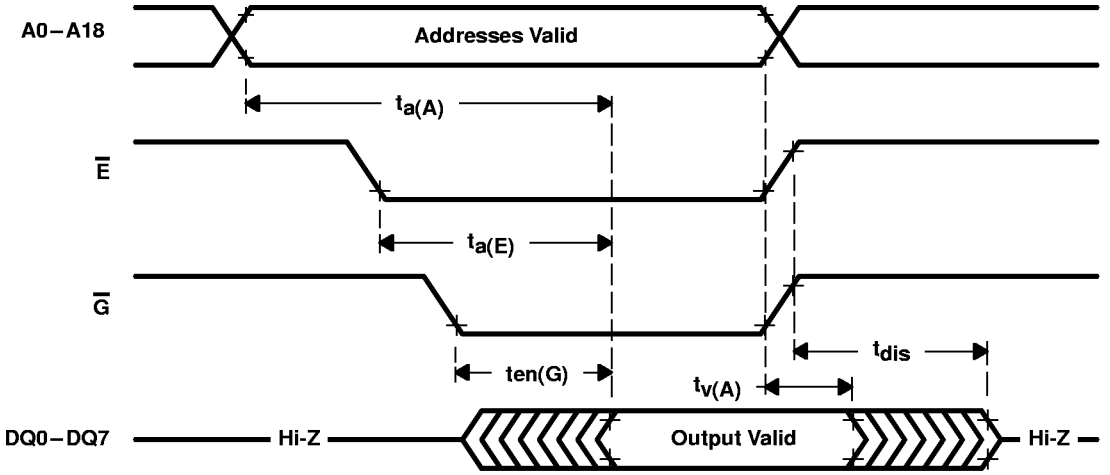
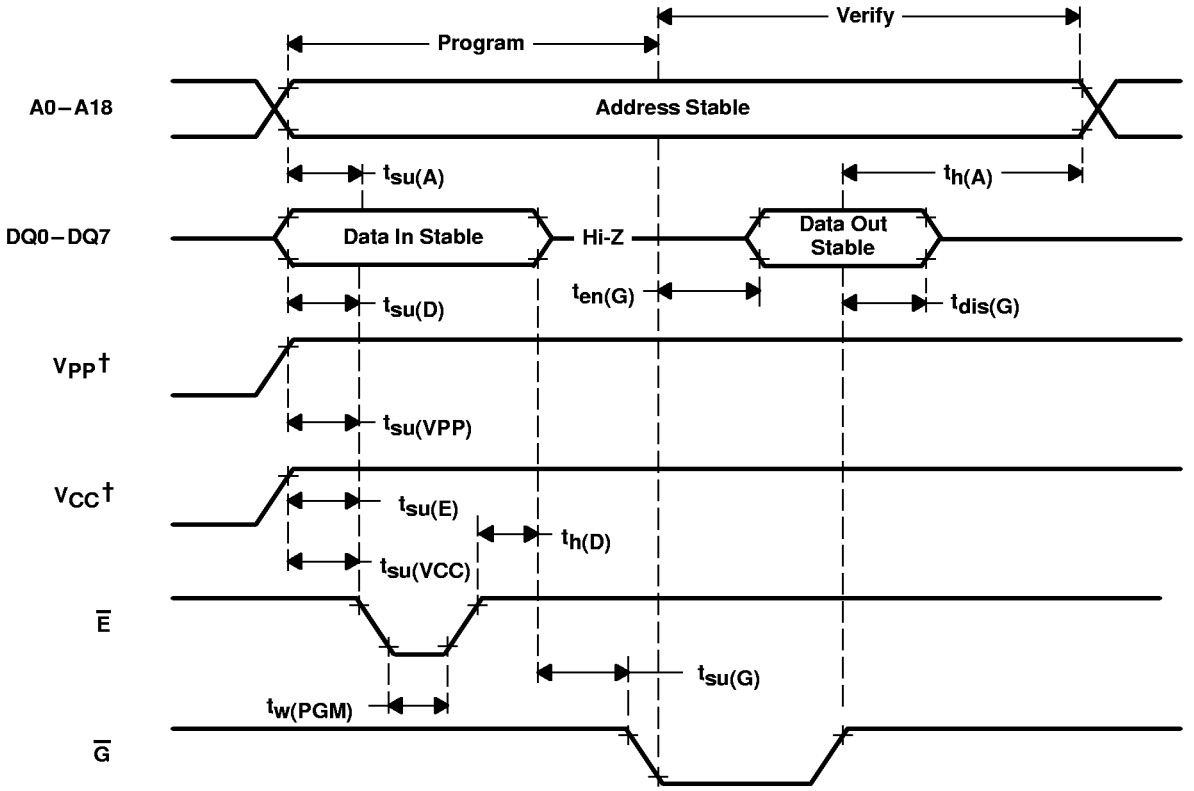


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

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