

- Functionally Equivalent to AM29827 and AM29828
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or busses carrying parity.

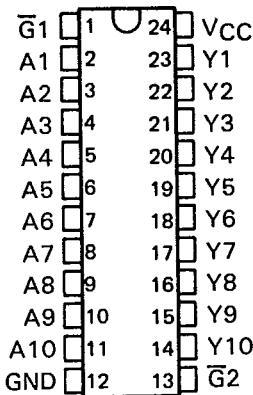
The three-state control gate is a 2-input NOR such that if either \bar{G}_1 or \bar{G}_2 is high, all ten outputs are in the high-impedance state.

The SN74ALS29827 provides true data and the SN74ALS29828 provides inverted data at the outputs.

The SN74' family is characterized for operation from 0°C to 70°C.

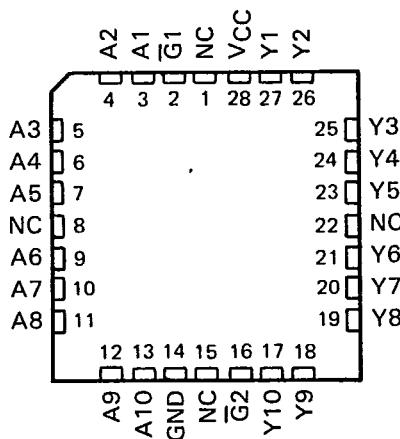
DW OR NT PACKAGE

(TOP VIEW)



FN PACKAGE

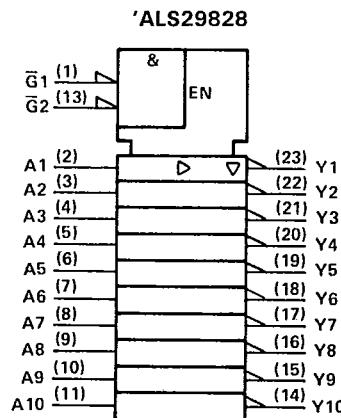
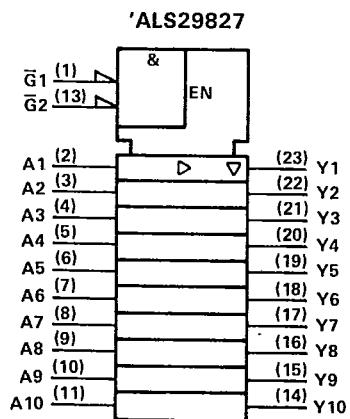
(TOP VIEW)



SN74ALS29827, SN74ALS29828
10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

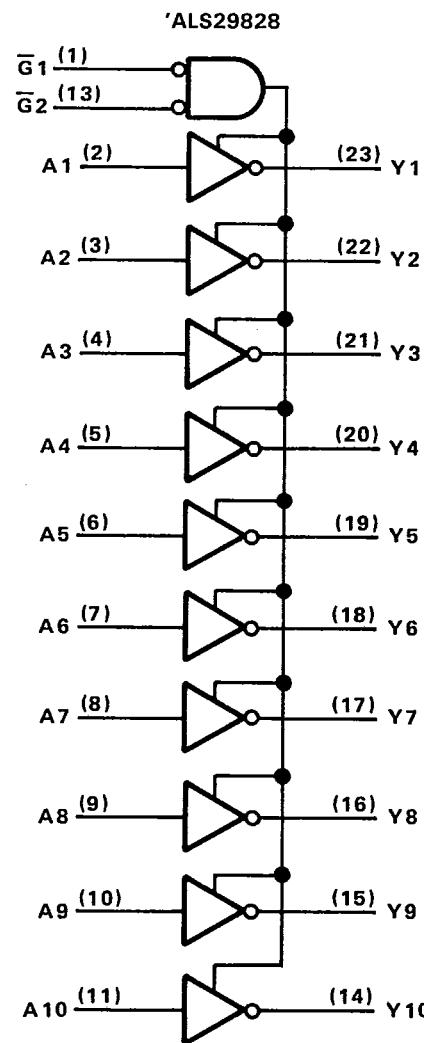
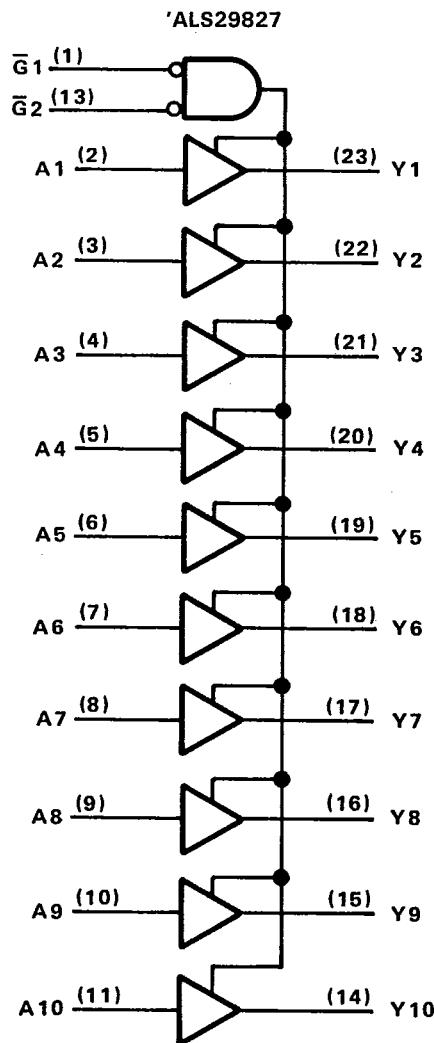
TEXAS INSTR {LOGIC} 86 DE 8961723 0073934 0 7-52.09

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



Pin numbers shown are DW and NT packages.

8961723 TEXAS INSTR (LOGIC)

86D 73935 D T-52-09

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			-24	mA
I _{OL}	Low-level output current			48	mA
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V, I _I = -18 mA			-1.2	V
V _{OH}	V _{CC} = 4.75 V, I _{OH} = -15 mA	2.4			V
	V _{CC} = 4.75 V, I _{OH} = -24 mA	2			
V _{OL}	V _{CC} = 4.75 V, I _{OL} = 48 mA		0.35	0.5	V
I _{OZH}	V _{CC} = 5.25 V, V _O = 2.4 V			20	μA
I _{OZL}	V _{CC} = 5.25 V, V _O = 0.4 V			-20	μA
I _I	V _{CC} = 5.25 V, V _I = 5.5 V		0.1		mA
I _{IH}	V _{CC} = 5.25 V, V _I = 2.7 V			20	μA
I _{IL}	V _{CC} = 5.25 V, V _I = 0.4 V			-0.1	mA
I _{OS[‡]}	V _{CC} = 5.25 V, V _O = 0 V	-75		-250	mA
I _{CC}	'ALS29827	V _{CC} = 5.25 V	25	40	mA
	'ALS29828	V _{CC} = 5.25 V	25	40	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.[‡] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74ALS29827, SN74ALS29828 TEXAS INSTR {LOGIC} 86 DE 8961723 0073936 3
10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

8961723 TEXAS INSTR (LOGIC)

86D 73936 D **T-52-09**

SN74ALS29827 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C			V _{CC} = 4.75 V to 5.25 V, T _A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 300 pF	8	11			15	ns
t _{PHL}				10.8	13.2			15	
t _{PLH}			C _L = 50 pF	4.8	6			8	
t _{PHL}				5.2	6.2			8	
t _{PZH}	G	Y	C _L = 300 pF	11	17			20	ns
t _{PZL}				18	21			23	
t _{PZH}			C _L = 50 pF	6.5	12			15	
t _{PZL}				9.5	12			15	
t _{PHZ}	G	Y	C _L = 50 pF	11.2	16			17	ns
t _{PLZ}				4.5	9			12	
t _{PHZ}			C _L = 5 pF	3.5	8			9	
t _{PLZ}				3.5	8			9	

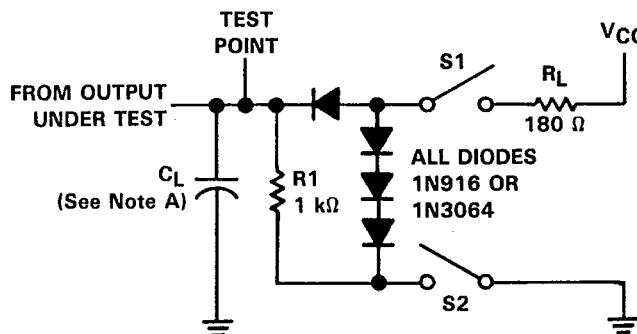
SN74ALS29828 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25°C			V _{CC} = 4.75 V to 5.25 V, T _A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 300 pF	7.3	10			14	ns
t _{PHL}				8.5	12.9			14	
t _{PLH}			C _L = 50 pF	4	5.2			7	
t _{PHL}				3	5.9			7.5	
t _{PZH}	G	Y	C _L = 300 pF	13	17			20	ns
t _{PZL}				16	21			23	
t _{PZH}			C _L = 50 pF	6.5	12			15	
t _{PZL}				9.5	12			15	
t _{PHZ}	G	Y	C _L = 50 pF	10	16			17	ns
t _{PLZ}				4	9			12	
t _{PHZ}			C _L = 5 pF	4.5	8			9	
t _{PLZ}				4.5	8			9	

8961723 TEXAS INSTR (LOGIC)

86D 73937 D T-52-09

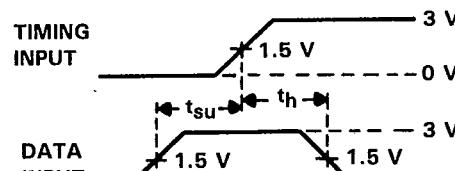
PARAMETER MEASUREMENT INFORMATION



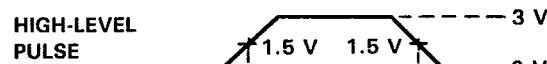
SWITCH POSITION TABLE

TEST	S1	S2
tPLH	Closed	Closed
tPHL	Closed	Closed
tPZH	Open	Closed
tPZL	Closed	Open
tPHZ	Closed	Closed
tPLZ	Closed	Closed

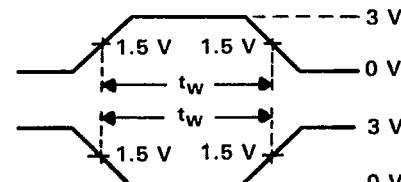
LOAD CIRCUIT



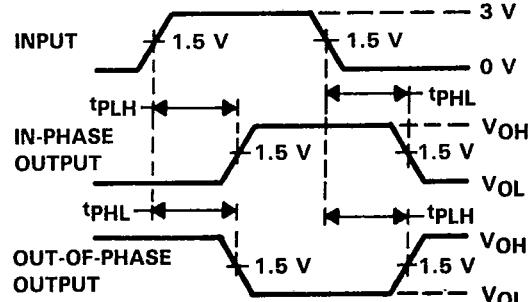
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



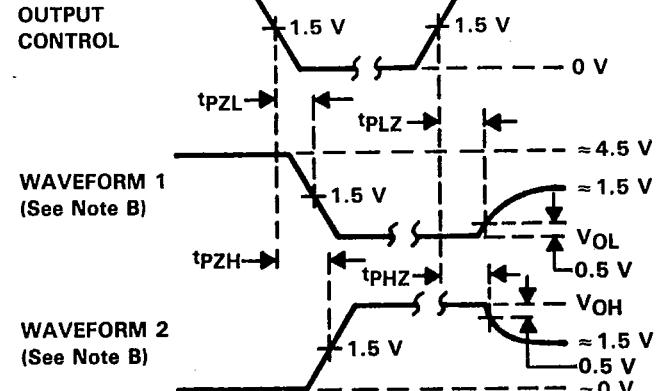
LOW-LEVEL PULSE



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

FIGURE 1