TMS27C400 4 194 304-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC400 4 194 304-BIT PROGRAMMABLE READ-ONLY MEMORY

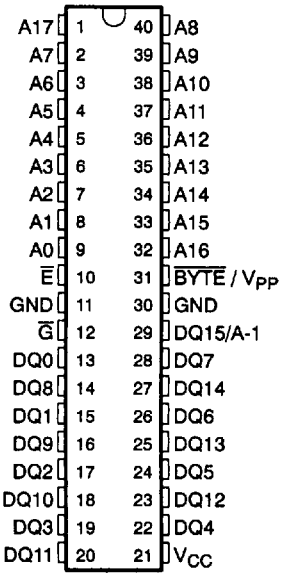
SMLS400A–OCTOBER 1992–REVISED JANUARY 1993

- Word-Wide (256K × 16) or Byte-Wide (512K × 8) Configurable
- 4-Megabit Mask ROM Compatible
  - 40-Lead CERDIP Package
  - 40-Lead PDIP Package
- Single 5-V Power Supply
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

  V_{CC} ± 10%

  '27C/PC400-10 100 ns
  '27C/PC400-12 120 ns
  '27C/PC400-15 150 ns
- Very High Speed SNAP! Pulse Programming
- Power-Saving CMOS Technology
- 3-State Output Buffers
- 400-mV Guaranteed DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Lines
- No Pullup Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - Active . . . 275 mW Worst Case
  - Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges

TMS27C400
J AND N PACKAGES
(TOP VIEW)



PIN NOMENCLATURE	
A0–A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
DQ0–DQ14	Inputs (Programming)/Outputs
DQ15/A-1	Input (Programming). Output (Word-Wide Read Mode), Byte Select (Byte-Wide Read Mode)
$\overline{BYTE}$	Word/Byte Enable
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply (Program Mode Only)

description

The TMS27C400 is a 4 194 304-bit ultraviolet-light erasable, electrically programmable read-only memory, organized as 262 144 words of 16 bits each. A byte enable switch allows the device to be addressed as a 524 288 × 8-bit device. The TMS27C400 is pinout and functionally compatible with 40-pin 4-megabit Mask ROMs.

The TMS27PC400 is a 4 194 304-bit, one-time electrically programmable (OTP) read-only memory, organized as 262 144 words of 16 bits each. A byte enable switch allows the device to be addressed as a 524 288 × 8-bit device. The TMS27PC400 is pinout and functionally compatible with 4-megabit Mask ROMs in a 40-pin dual-in-line plastic package (N suffix).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

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The TMS27C400 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C400 is also offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (JL and JE suffixes). The TMS27C400 is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC400 OTP PROM is offered in a 40-pin dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC400 is also offered with two choices of temperature ranges, 0°C to 70°C and – 40°C to 85°C (NL and NE suffixes). The TMS27PC400 is also offered with 168 hour burn-in on both temperature ranges (NL4 and NE4 suffixes). (See table below.)

	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C400-xx	JL	JE	JL4	JE4
TMS27PC400-xx	NL	NE	NL4	NE4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The following table lists modes of operation for the TMS27C400 and TMS27PC400. The read mode requires a single 5-V supply. All inputs are TTL level except V_{CC}, $\overline{BYTE}$ / V_{PP} during programming (13 V for SNAP! Pulse), and A9 for signature modes (12 V).

MODE	$\overline{E}$	$\overline{G}$	$\overline{BYTE}$ / V_{PP}	V_{CC}	A9	A0	DQ15/A-1	DQ8–DQ14	DQ0–DQ7
Read (Word)	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	X	DQ15	DQ8–DQ14	DQ0–DQ7
Read (Upper Byte)	V_{IL}	V_{IL}	V_{IL}	V_{CC}	X	X	V_{IH}	HI-Z	DQ8–DQ15
Read (Lower Byte)	V_{IL}	V_{IL}	V_{IL}	V_{CC}	X	X	V_{IL}	HI-Z	DQ0–DQ7
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	X	X	HI-Z	HI-Z	HI-Z
Standby	V_{IH}	X†	X	V_{CC}	X	X	HI-Z	HI-Z	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In	Data In	Data In
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z	HI-Z	HI-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	0B	00H	97H
Signature Mode (Dev)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IH}	0B	00H	54H

† All X's can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C400s or TMS27PC400s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

word-wide mode

With $\overline{BYTE}$ / V_{PP} at V_{IH}, outputs DQ8–DQ15 present the upper eight bits of data for the address selected, and outputs DQ0–DQ7 present the lower eight bits of data when $\overline{E}$ and $\overline{G}$ are appropriately enabled.

byte-wide mode

With $\overline{BYTE}/V_{PP}$ at V_{IL}, outputs DQ8–DQ14 are disabled. Two selectable bytes of data determined by the logic state on DQ15/A-1 will appear on outputs DQ0–DQ7. When DQ15/A-1=V_{IH}, the upper byte or eight bits of data will appear on outputs DQ0–DQ7. When DQ15/A-1=V_{IL}, the lower byte or eight bits of data will appear on outputs DQ0–DQ7.

latchup immunity

Latchup immunity on the TMS27C400 and TMS27PC400 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C400)

Before programming, theTMS27C400 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C400, the window should be covered with an opaque label.

initializing (TMS27PC400)

The one-time programmable TMS27PC400 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C400 and TMS27PC400 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is $\overline{BYTE}$ / V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, and $\overline{G}$ = V_{IH}. Once the initial location is selected, the data is presented in parallel (16 bits) on pins DQ0–DQ15. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at $\overline{BYTE}$ / V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, and $\overline{G}$ = V_{IL}. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with V_{CC} = $\overline{BYTE}$ / V_{PP} = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with $\overline{BYTE}$ / V_{PP} = 13 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 39) is forced to 12 V. Two identifier bytes are accessed by toggling A0. A0 low selects the manufacturer's code (0097 HEX), and A0 high selects the device code (0054 HEX), as shown by the table below. All other addresses must be held low.

IDENTIFIER	A0	DQ8-DQ15	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer's Code	V_{IL}	All 0	H	L	L	H	L	H	H	H	0097
Device Code	V_{IH}	All 0	L	H	L	H	L	H	L	L	0054

NOTE: $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A17 = V_{IL}, $\overline{BYTE}$ / V_{PP} = V_{CC}.

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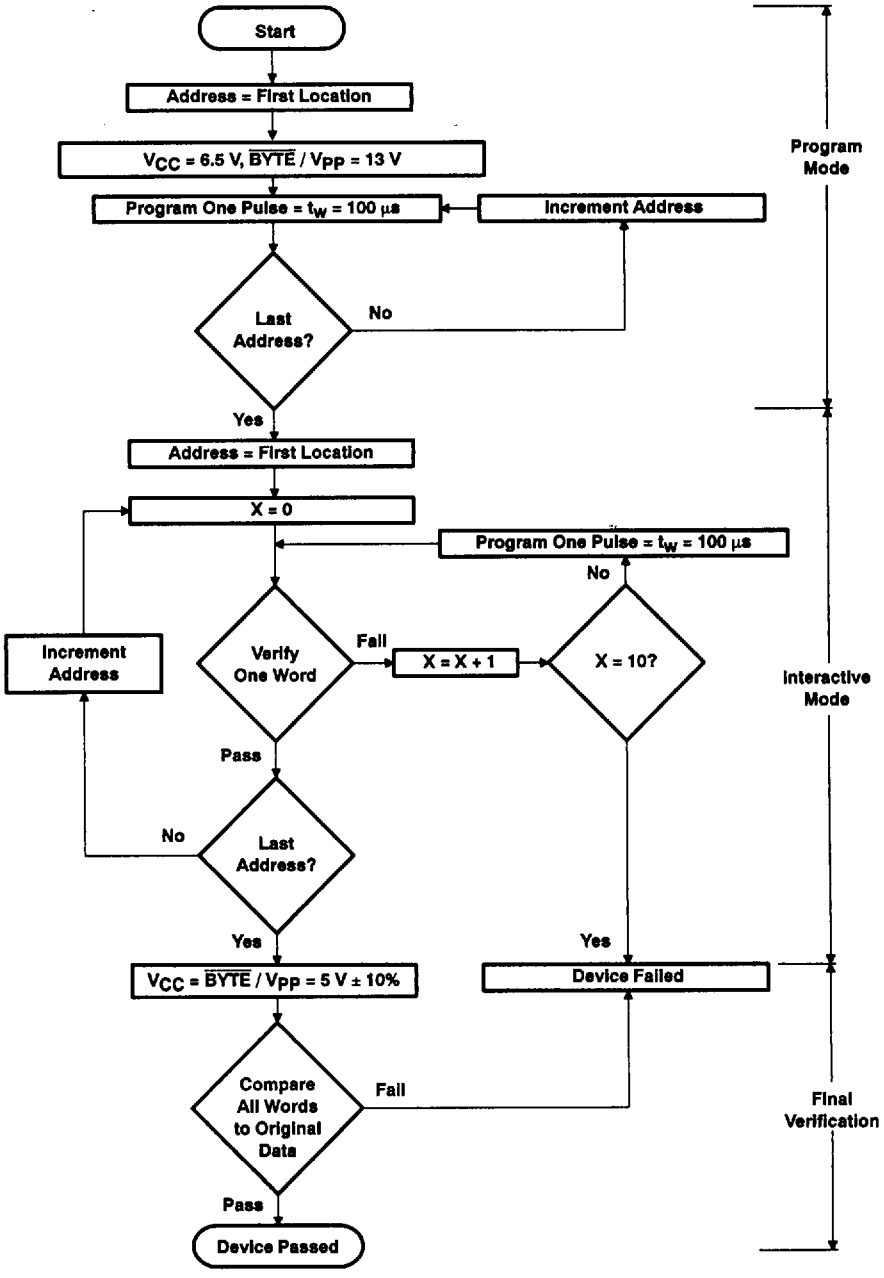
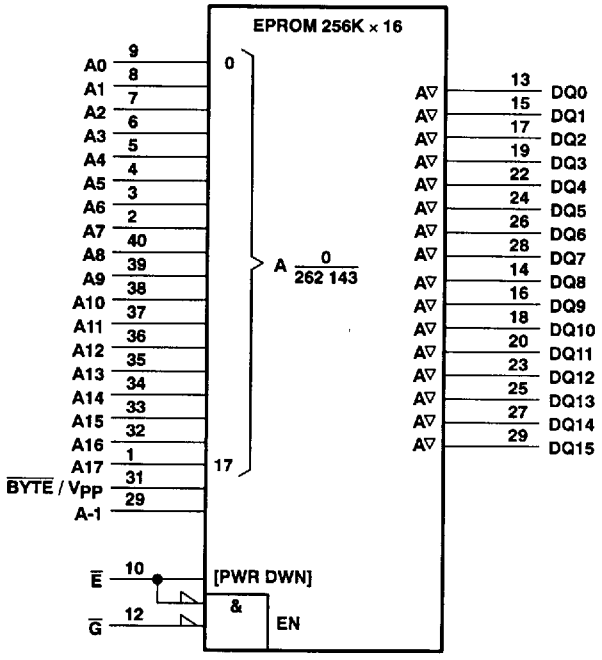


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, $\overline{BYTE}$ / V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C400__JL and JL4, '27PC400__NL and NL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C400__JE and JE4, '27PC400__NE and NE4) ..... − 40°C to 85°C
Storage temperature range ..... −65°C to 125°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				TMS27C/PC400-10 TMS27C/PC400-12 TMS27C/PC400-15			UNIT
				MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse Programming algorithm		6.25	6.5	6.75	
BYTE/ V_{PP}	Supply voltage	Read mode (WORD) Read mode (BYTE) (see Note 3)		V_{IH} −0.5		V_{CC} + 0.5 V_{IL}	V
		SNAP! Pulse Programming algorithm		12.75	13	13.25	
V_{IH}	High-level input voltage		TTL	2		V_{CC}+ 0.5	V
			CMOS	V_{CC} − 0.2		V_{CC}+ 0.5	
V_{IL}	Low-level input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature		'27C400_ _JL, JL4 '27PC400_ _NL, NL4	0		70	°C
			'27C400_ _JE, JE4 '27PC400_ _NE, NE4	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as $\overline{BYTE}$/ V_{PP} and removed after or at the same time as $\overline{BYTE}$ / V_{PP}. The device must not be inserted into or removed from the board when $\overline{BYTE}$ / V_{PP} or V_{CC} is applied.

3. $\overline{BYTE}$ / V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming $\overline{BYTE}$ / V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = − 2.5 mA	2.4		V
			I_{OH} = − 20 µA	V_{CC} − 0.1		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 µA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	$\overline{BYTE}$ / V_{PP} operating current		$\overline{BYTE}$ / V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$\overline{BYTE}$ / V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL} t_{cycles} = 5 MHz outputs open		50	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0		4	8	pF
C_O	Output capacitance	V_O = 0		8	12	pF
$C_{BYTE / VPP}$	$\overline{BYTE}$/ V_{PP} capacitance	$\overline{BYTE}$ / V_{PP} = 0		18	25	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

		TEST CONDITIONS (SEE NOTES 4, 5, & 6)	'27C/PC400-10		'27C/PC400-12		'27C/PC400-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns,		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
5. Common test conditions apply for t_{dis} except during programming.
6. $t_{a(A)}$ includes access time from DQ15/A-1 in Byte Wide Read Mode.

switching characteristics for programming: V_{CC} = 6.5 V and $\overline{BYTE}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and $\overline{BYTE}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	$\overline{BYTE}$ / V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

PARAMETER MEASUREMENT INFORMATION

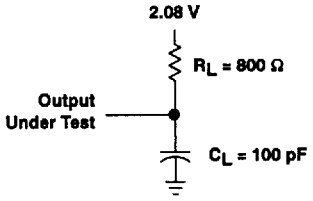
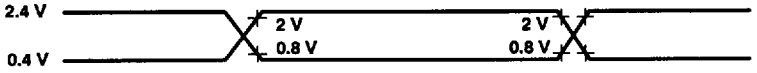


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

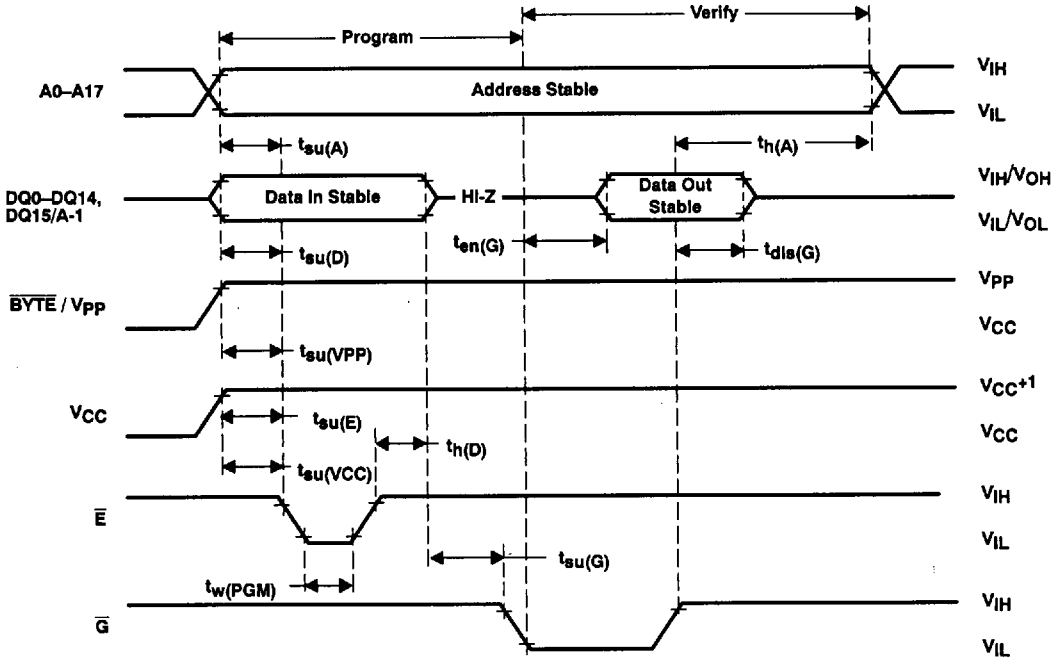
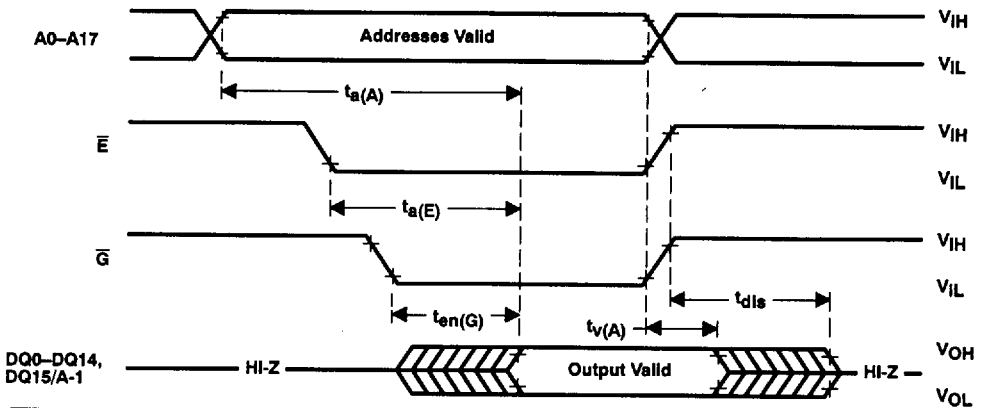


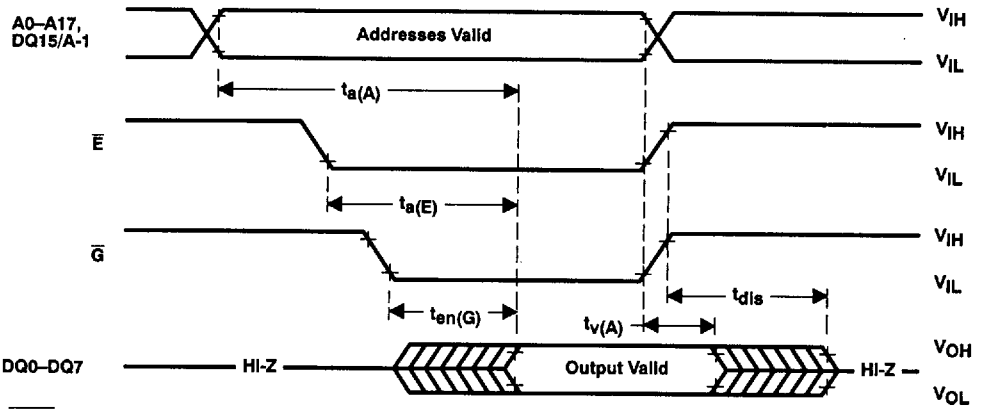
Figure 3. Program Cycle Timing (Snap! Pulse Programming)

PARAMETER MEASUREMENT INFORMATION



NOTE: $\overline{BYTE}$ / V_{PP} = V_{IH}

Figure 4. Read Cycle Timing: Word-Wide Read Mode



NOTE: $\overline{BYTE}$ / V_{PP} = V_{IL}
DQ8–DQ14 = HI-Z

Figure 5. Read Cycle Timing: Byte-Wide Read Mode

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