PRODUCT PREVIEW

TMX44C256, TMX44C257, TMX44C259
262,144-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORIES

NOVEMBER 1985

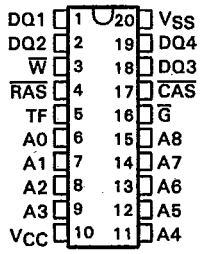
T-46-23-17

- 262,144 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- Pinout to Proposed JEDEC Standard
- Performance Ranges:

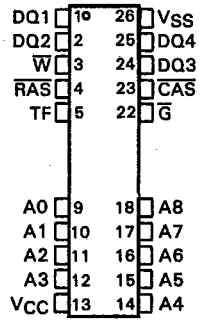
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMX44C25_-10	100 ns	50 ns	200 ns
TMX44C25_-12	120 ns	60 ns	230 ns
TMX44C25_-15	150 ns	75 ns	260 ns

- Multiple Operations Options:
  TMX44C256 — Page Mode/Enhanced Page Mode
  TMX44C257 — Static Column Mode
  TMX44C259 — 256 X 4 Bit Nibble Mode (Serial Mode)
- Long Refresh Period
  512-Cycle Refresh in 8 ms (Max)
- Three-State Unlatched Output
- Lower Power Dissipation
- New Scaled-CMOS Technology
- Low Standby Power with CMOS-Level Inputs
- High-Reliability Plastic 20-Pin 300-Mil-Wide DIP or Surface-Mount Packages

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

description

The Megabit DRAM devices are high-speed, 1,048,576-bit dynamic random-access memories organized as 262,144 words of four bits each. They employ state-of-the-art TIC-MOS (Scaled CMOS) technology for high performance, reliability and lower power at a low cost.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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