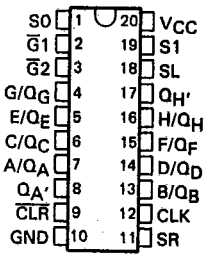
# SN54F323, SN74F323
# 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

D2932, MARCH 1987—REVISED JANUARY 1989

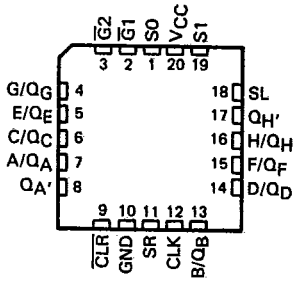
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can be Cascaded for N-Bit Word Lengths
- Synchronous Clear
- Applications:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54F323 . . . J PACKAGE
SN74F323 . . . DW OR N PACKAGE
(TOP VIEW)

T-46-09-05




SN54F323 . . . FK PACKAGE
(TOP VIEW)




## description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs synchronously when $\overline{CLR}$ is low. Taking either of the output controls $\overline{G1}$ or $\overline{G2}$ high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54F323 is characterized for operation over the full military range of −55°C to 125°C. The SN74F323 is characterized for operation from 0°C to 70°C.





TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54F323, SN74F323
# 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

**FUNCTION TABLE**

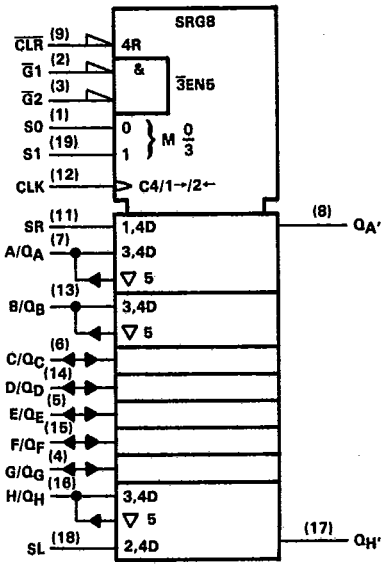
| MODE | INPUTS | | | | | | | I/O PORTS | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | S1 | S0 | OUTPUT CONTROL $\overline{G1}$† | OUTPUT CONTROL $\overline{G2}$† | CLK | SL | SR | A/$Q_A$ | B/$Q_B$ | C/$Q_C$ | D/$Q_D$ | E/$Q_E$ | F/$Q_F$ | G/$Q_G$ | H/$Q_H$ | $Q_{A'}$ | $Q_{H'}$ |
| Clear | L | X | L | L | L | ↑ | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | L | X | L | L | ↑ | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | H | H | X | X | ↑ | X | X | X | X | X | X | X | X | X | X | L | L |
| Hold | H | L | L | L | L | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| | H | X | X | L | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | H | $Q_{Gn}$ |
| | H | L | H | L | L | ↑ | X | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | L | $Q_{Gn}$ |
| Shift Left | H | H | L | L | L | ↑ | H | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | H | $Q_{Bn}$ | H |
| | H | H | L | L | L | ↑ | L | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | L | $Q_{Bn}$ | L |
| Load | H | H | H | X | X | ↑ | X | X | a | b | c | d | e | f | g | h | a | h |

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

2 Data Sheets

## logic symbol‡




‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

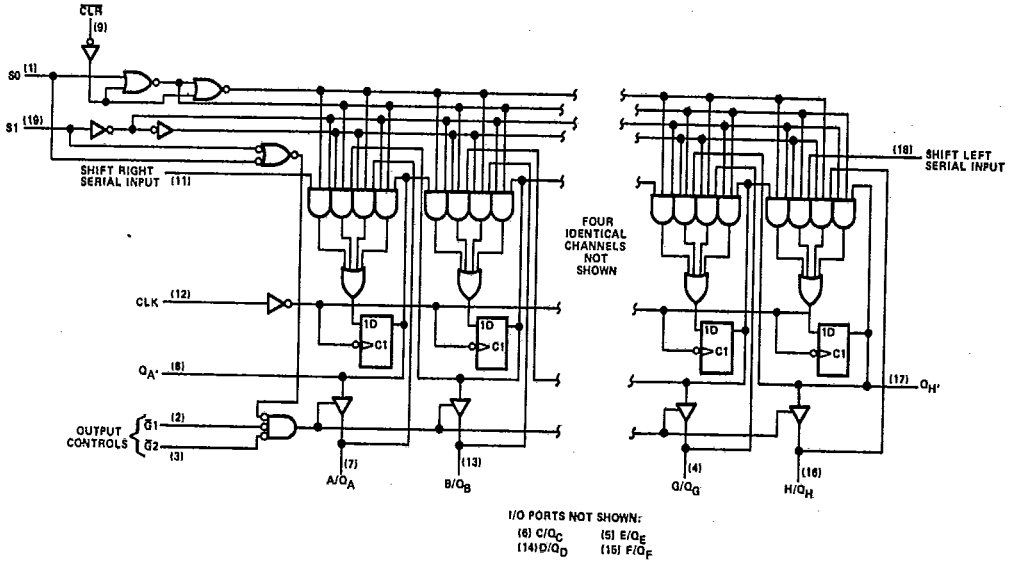


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54F323, SN74F323
# 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

T-46-09-05

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to $V_{CC}$
Current into any output in the low state: ($Q_{A'}$ or $Q_{H'}$) . . . . . 40 mA
SN54F323 ($Q_A$ thru $Q_H$) . . . . . 40 mA
SN74F323 ($Q_A$ thru $Q_H$) . . . . . 48 mA
Operating free-air temperature range: SN54F323 . . . . . −55°C to 125°C
SN74F323 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

**SN54F323, SN74F323**
**8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS**
**WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS**

T-46-09-05



### recommended operating conditions

| | | | SN54F323 | | | SN74F323 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | $Q_{A'}$ or $Q_{H'}$ | | | −1 | | | −1 | mA |
| | | $Q_A$ thru $Q_H$ | | | −3 | | | −3 | |
| $I_{OL}$ | Low-level output current | $Q_{A'}$ or $Q_{H'}$ | | | 20 | | | 20 | mA |
| | | $Q_A$ thru $Q_H$ | | | 20 | | | 24 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |



### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F323 | | | SN74F323 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V,, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| | $Q_A$ thru $Q_H$ | | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | Any output | $V_{CC}$ = 4.75 V | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| | $Q_A$ thru $Q_H$ | | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | A thru H | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | Any other | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$‡ | A thru H | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | |
| | Any other | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | A thru H | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.65 | | | −0.65 | mA |
| | S0 or S1 | | | | | −1.2 | | | −1.2 | |
| | Any other | | | | | −0.6 | | | −0.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = MAX, | See Note 1 | | 68 | 95 | | 68 | 95 | mA |



† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports ($Q_A$ thru $Q_H$), the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ No more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: $I_{CC}$ is measured with $\overline{G}1$, $\overline{G}2$, and CLK at 4.5 V.



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

## timing requirements over recommended operating free-air temperature range (see Note 2)

| PARAMETER | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 'F323 | | SN54F323 | | SN74F323 | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 70 | | | 0 | 70 | MHz |
| $t_{su}$ | Setup time before CLK↑ | S0 or S1 high or low | 8.5 | | | | 8.5 | | ns |
| $t_h$ | Hold time after CLK↑ | S0 or S1 high or low | 0 | | | | 0 | | ns |
| $t_{su}$ | Setup time before CLK↑ | A/$Q_A$ thru H/$Q_H$, SR, or SL high or low | 5 | | | | 5 | | ns |
| $t_h$ | Hold time after CLK↑ | A/$Q_A$ thru H/$Q_H$, SR, or SL high or low | 2 | | | | 2 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ high or low | 10 | | | | 10 | | ns |
| $t_h$ | Hold time after CLK↑ | $\overline{CLR}$ high or low | 0 | | | | 0 | | ns |
| $t_w$ | Pulse duration | CLK high or low | 7 | | | | 7 | | ns |



## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F323 | | | SN54F323 | | SN74F323 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 70 | 100 | | | | 70 | | MHz |
| $t_{PLH}$ | CLK | $Q_{A'}$ or $Q_{H'}$ | 3.2 | 6.6 | 9 | | | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 2.7 | 6.1 | 8.5 | | | 2.7 | 9.5 | |
| $t_{PLH}$ | CLK | $Q_A$ thru $Q_H$ | 3.2 | 6.6 | 9 | | | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 4.2 | 8.1 | 11 | | | 4.2 | 12 | |
| $t_{PZH}$ | $\overline{G}1$ or $\overline{G}2$ | $Q_A$ thru $Q_H$ | 2.7 | 5.6 | 8 | | | 2.7 | 9 | ns |
| $t_{PZL}$ | | | 3.2 | 6.6 | 10 | | | 3.2 | 11 | |
| $t_{PHZ}$ | $\overline{G}1$ or $\overline{G}2$ | $Q_A$ thru $Q_H$ | 1.7 | 4.1 | 6 | | | 1.7 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.6 | 5.5 | | | 1.2 | 6.5 | |



† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.