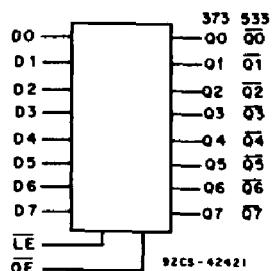


CD54/74AC373, CD54/74AC533

CD54/74ACT373, CD54/74ACT533



Data sheet acquired from Harris Semiconductor
SCHS289



Octal Transparent Latch, 3-State

CD54/74AC/ACT373 - Non-Inverting

CD54/74AC/ACT533 - Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
4.3 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

FUNCTIONAL DIAGRAM

The RCA-CD54/74AC373 and CD54/74AC533 and the CD54/74ACT373 and CD54/74ACT533 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable (LE) is HIGH. When the Latch Enable (LE) goes LOW, the data is latched. The Output Enable (OE) controls the 3-state outputs. When the Output Enable (OE) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT373 and CD74AC/ACT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

The CD54AC/ACT373 and CD54AC/ACT533, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST®/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST® ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

Output Enable	Latch Enable	Data	AC/ACT373 Output	AC/ACT533 Output
L	H	H	H	L
L	H	L	L	H
L	L	I	L	H
L	L	h	H	L
H	X	X	Z	Z

Note:

L = Low voltage level
H = High voltage level
I = Low voltage level one set-up time prior to the high to low latch enable transition
h = Don't Care

z = High impedance state
h = High voltage level one set-up time prior to the high to low latch enable transition.
X = Don't Care
Z = High Impedance State

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{cc})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{ik} (for $V_i < -0.5$ V or $V_i > V_{cc} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{ok} (for $V_o < -0.5$ V or $V_o > V_{cc} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_o (for $V_o > -0.5$ V or $V_o < V_{cc} + 0.5$ V)	± 50 mA
DC V_{cc} or GROUND CURRENT (I_{cc} or I_{GND})	± 100 mA*

POWER DISSIPATION PER PACKAGE (P_o):

For $T_A = -55$ to $+100^\circ C$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ C$ to 300 mW
For $T_A = -55$ to $+70^\circ C$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ C$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ C$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ C$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 \pm 0.79 mm) from case for 10 s maximum	$+265^\circ C$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ C$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

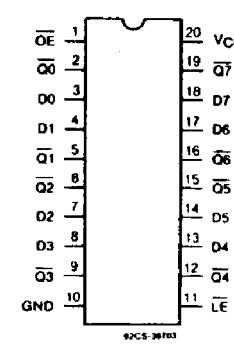
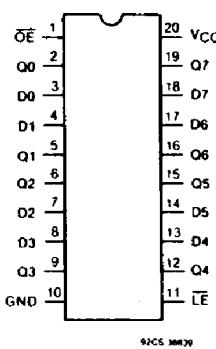
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{cc} *: (For $T_A =$ Full Package-Temperature Range)			
AC Types	1.5	5.5	
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_i , V_o	0	V_{cc}	V
Operating Temperature, T_A	-55	$+125$	$^\circ C$
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V(AC Types) at 3.6 V to 5.5 V(AC Types) at 4.5 V to 5.5 V(ACT Types)	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

9

TERMINAL ASSIGNMENT DIAGRAMS

Technical Data

**CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533**

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS		
			+25		-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V _{IH}		1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	V _{IL}		1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL} #, *	-0.05	1.5	1.4	—	1.4	—	1.4	V	
			-0.05	3	2.9	—	2.9	—	2.9		
			-0.05	4.5	4.4	—	4.4	—	4.4		
			-4	3	2.58	—	2.48	—	2.4		
			-24	4.5	3.94	—	3.8	—	3.7		
			-75	5.5	—	—	3.85	—	—		
			-50	5.5	—	—	—	3.85	—		
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05	1.5	—	0.1	—	0.1	—	V	
			0.05	3	—	0.1	—	0.1	—		
			0.05	4.5	—	0.1	—	0.1	—		
			12	3	—	0.36	—	0.44	—		
			24	4.5	—	0.36	—	0.44	—		
			75	5.5	—	—	—	1.65	—		
			50	5.5	—	—	—	—	1.65		
Input Leakage Current	I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS		
			+25		-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V_{IH}	4.5 to 5.5	2	—	2	—	2	—	V		
Low-Level Input Voltage	V_{IL}	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V		
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL} #, *	-0.05 -24 -75 -50	4.5 3.94 5.5 5.5	4.4 3.8 — —	4.4 3.8 3.85 —	4.4 3.7 — 3.85	— — — —	V		
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL} #, *	0.05 24 75 50	4.5 4.5 5.5 5.5	— — — —	0.1 0.36 — —	0.1 0.44 1.65 —	— — — 1.65	V		
Input Leakage Current	I_I	V_{CC} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} $V_O = V_{CC}$ or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

9

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	ACT373	ACT533
OE	0.87	0.87
Dn	0.5	0.5
LE	0.8	0.8

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

**CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533**

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
LE Pulse Width	t _W	1.5 3.3* 5†	44 4.9 3.5	— — —	50 5.6 4	— — —	ns	
Setup Time Data to LE	t _{SU}	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns	
Hold Time Data to LE	t _H	1.5 3.3 5	33 3.7 2.6	— — —	38 4.2 3	— — —	ns	

*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_W, t_H = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS		
			-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.			
Propagation Delays: Data to Qn 373	t _{PLH} t _{PHL}	1.5 3.3* 5†	— 3.1 2.2	96 10.8 7.7	— 3 2.1	106 11.9 8.5	ns		
533	t _{PLH} t _{PHL}	1.5 3.3 5	— 3.8 2.7	119 13.4 9.5	— 3.7 2.6	131 14.7 10.5	ns		
LE on Qn 373	t _{PLH} t _{PHL}	1.5 3.3 5	— 4.3 3.1	136 15.2 10.9	— 4.2 3	150 16.8 12	ns		
533	t _{PLH} t _{PHL}	1.5 3.3 5	— 4.3 3.1	136 15.3 10.9	— 4.2 3	150 16.8 12	ns		
Output Enable Times	t _{PZL} t _{PZH}	1.5 3.3 5	— 4.1 2.7	119 14.4 9.5	— 4 2.6	131 15.8 10.5	ns		
Output Disable Times	t _{PZL} t _{PZH}	1.5 3.3 5	— 3.7 3	131 13.1 10.5	— 3.6 2.9	144 14.4 11.5	ns		
Power Dissipation Capacitance	C _{PD} §	—	63 Typ.		63 Typ.		pF		
Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} See Fig. 1	5	4 Typ. @ 25°C				V		
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V		
Input Capacitance	C _I	—	—	10	—	10	pF		
3-State Output Capacitance	C _O	—	—	15	—	15	pF		

*3.3 V: min. is @ 3.6 V
max. is @ 3 V†5 V: min. is @ 5.5 V
max. is @ 4.5 V§C_{PD} is used to determine the dynamic power consumption, per latch.

$$P_D = V_{CC}^2 f_i (C_{PD} + C_L) \text{ where } f_i = \text{input frequency}$$

C_L = output load capacitanceV_{CC} = supply voltage

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
LE Pulse Width	t_W	5†	3.6	—	4	—	ns	
Setup Time Data to LE	t_{SU}	5	2	—	2	—	ns	
Hold Time Data to LE	t_H	5	2.7	—	3	—	ns	

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; $t_s, t_r = 3$ ns, $C_L = 50$ pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS		
			-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.			
Propagation Delays: Data to Qn 373	t_{PLH}	5†	2.7	9.5	2.6	10.4	ns		
533	t_{PHL}		3	10.4	2.9	11.4			
LE to Qn 373 533	t_{PLH}	5	3.1	11.4	3	12.5	ns		
	t_{PHL}								
Output Enable Times	t_{PZL}	5	3.5	12.3	3.4	13.5	ns		
Output Disable Times	t_{PZL}	5	3.2	11.4	3.1	12.5	ns		
Power Dissipation Capacitance	$C_{PD\$}$	—	63 Typ.		63 Typ.		pF		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V		
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V		
Input Capacitance	C_I	—	—	10	—	10	pF		
3-State Output Capacitance	C_O	—	—	15	—	15	pF		

9

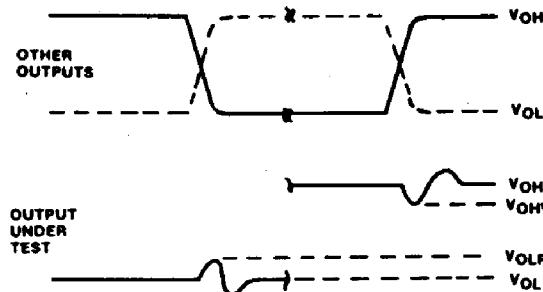
†5 V: min. is @ 5.5 V
max. is @ 4.5 V $\$C_{PD}$ is used to determine the dynamic power consumption, per latch.

$$P_D = V_{CC}^2 f_i (C_{PD\$} + C_L) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

$C_L = \text{output load capacitance}$
 $V_{CC} = \text{supply voltage.}$

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

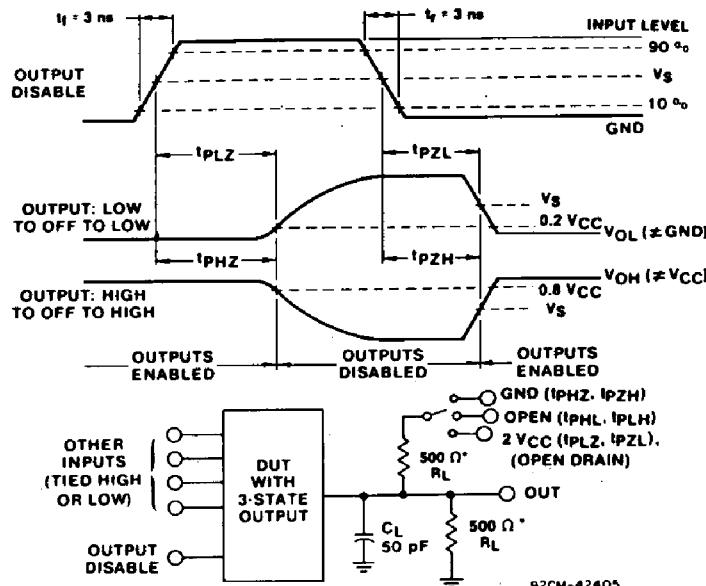
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OH} AND V_{OL} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, $t_L = 3$ ns, $t_H = 3$ ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH $0.1\ \mu F$ CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1\ k\Omega$

92CM-42405

Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.

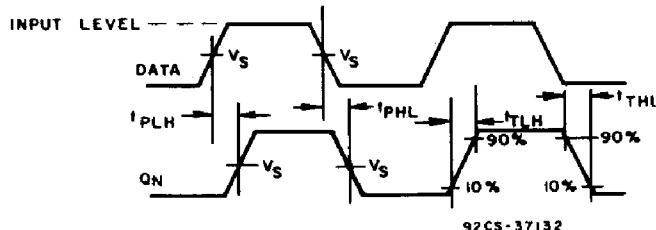
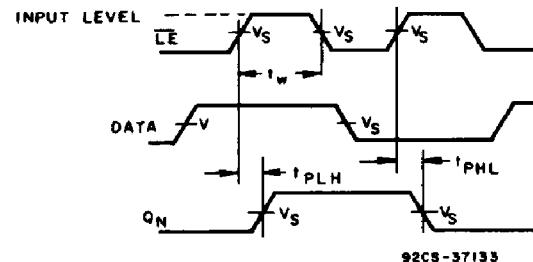
Fig. 3 - Data to Q_n output propagation delays and output transition times.

Fig. 4 - Latch enable propagation delays.

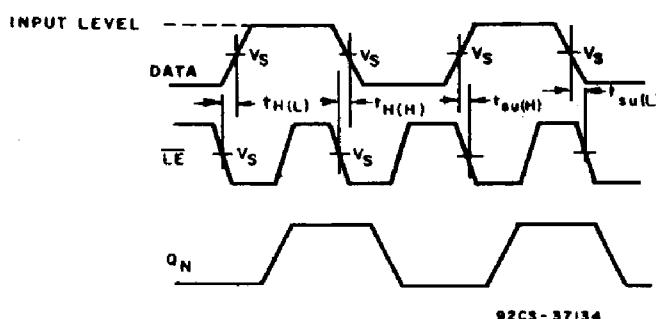


Fig. 5 - Latch enable prerequisite times.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_s	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_s	0.5 V_{CC}	0.5 V_{CC}

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.