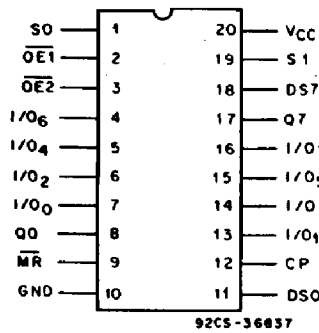




Data sheet acquired from Harris Semiconductor
SCHS288

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323



TERMINAL ASSIGNMENT

8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

CD54/74AC/ACT299 - Asynchronous Reset
CD54/74AC/ACT323 - Synchronous Reset

Type Features:

- Buffered inputs
- Typical propagation delay:
6 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

The RCA CD54/74AC299 and CD54/74AC323 and the CD54/74ACT299 and CD54/74ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices use the RCA ADVANCED CMOS technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DS0, DS7), and the Parallel Data (I/O₀ - I/O₇) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset ($\overline{\text{MR}}$) is an asynchronous active-LOW input. When MR is LOW, the register is cleared regardless of the status of all other inputs. With the CD54/74AC/ACT323, the Master Reset ($\overline{\text{MR}}$) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ($\overline{\text{OE1}}$ and $\overline{\text{OE2}}$) inputs are LOW and S0 or S1 or both are LOW; the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{\text{OE1}}$ and $\overline{\text{OE2}}$.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT299 and CD54AC/ACT323, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

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CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

MODE SELECT — FUNCTION TABLE REGISTER OPERATING MODES

FUNCTION	INPUTS							REGISTER OUTPUTS				
	\overline{MR}	CP	S0	S1	DS0	DS7	I/O _n	Q0	Q1	...	Q6	Q7
Reset (Clear)	L	X*	X	X	X	X	X	L	L	...	L	L
Shift Right	H		h	l	l	X	X	L	q ₀	...	q ₅	q ₆
	H		h	l	h	X	X	H	q ₀	...	q ₅	q ₆
Shift Left	H		l	h	X	l	X	q ₁	q ₂	...	q ₇	L
	H		l	h	X	h	X	q ₁	q ₂	...	q ₇	H
Hold (do nothing)	H		l	l	X	X	X	q ₀	q ₁	...	q ₆	q ₇
Parallel Load	H		h	h	X	X	l	L	L	...	L	L
	H		h	h	X	X	h	H	H	...	H	H

*On CD54/74AC/ACT323, CP must be in transition from the LOW-to-HIGH state to Reset (Clear).

MODE SELECT — FUNCTION TABLE 3-STATE I/O PORT OPERATING MODE

FUNCTION	INPUTS				Q _n (Register)	I/O ₀ ... I/O ₇
	$\overline{OE1}$	$\overline{OE2}$	S0	S1		
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Q _n = I/O _n	I/O _n = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = Input voltage high level.

h = Input voltage high one set-up time prior clock transition.

L = Input voltage low level.

l = Input voltage low one set-up time prior clock transition.

q_n = Lower case letters indicate the state of the referenced output one set-up time prior clock transition.

X = Voltage level on logic status don't care.

Z = Output in high-impedance state.

= Low-to-high clock transition.

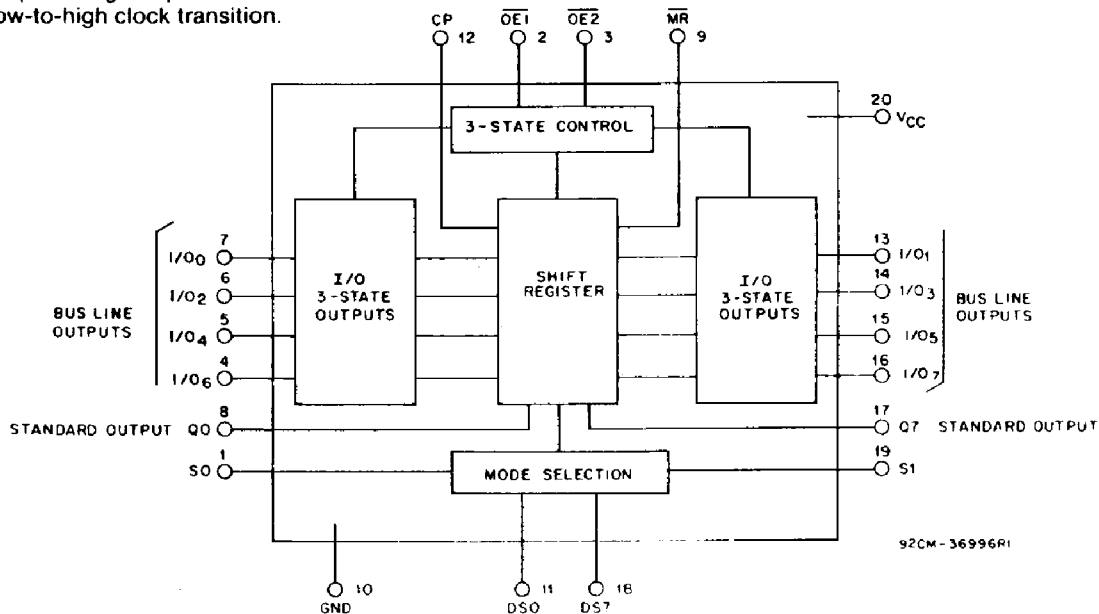


Fig. 1 - Functional diagram.

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_o (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	± 50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{STG})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, V_i, V_o	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V	
Low-Level Input Voltage	V _{IL}		1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V	
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
Input Leakage Current	I _I	V _{CC} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
			50	5.5	—	—	—	—	—	1.65	
3-Stage Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{cc} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OIH}	V _{IH} or V _{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OOL}	V _{IH} or V _{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{cc} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O V _{cc} or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I _{cc}	V _{cc} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{cc}	V _{cc} -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

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#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	299	323
S1, S0, OE1, OE2	0.83	0.83
I/O ₀ - I/O ₇ , CP, DS0, DS7	0.67	0.67
MR	1.33	0.67

*Unit load is ΔI_{cc} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0, to CP	t _{su}	1.5	99	—	113	—	ns
		3.3*	11.1	—	12.6	—	
		5†	7.9	—	9	—	
Hold Time S1, S0 to CP	t _h	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Setup Time (I/O)n, DS0, DS7 to CP	t _{su}	1.5	49	—	56	—	ns
		3.3	5.5	—	6.3	—	
		5	3.9	—	4.5	—	
Hold Time (I/O)n, DS0, DS7 to CP	t _{su}	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Setup Time MR to CP (323)	t _{su}	1.5	61	—	69	—	ns
		3.3	6.8	—	7.8	—	
		5	4.8	—	5.5	—	
Hold Time MR to CP (323)	t _h	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Maximum CP Frequency	f _{max}	1.5	9	—	8	—	MHz
		3.3	78	—	68	—	
		5	108	—	95	—	
CP Pulse Width	t _w	1.5	57	—	65	—	ns
		3.3	6.4	—	7.3	—	
		5	4.6	—	5.2	—	
MR Pulse Width	t _w	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
Recovery Time MR to CP 299	t _{rec}	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	

*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

Technical Data

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH}	1.5	—	147	—	162	ns
	t_{PHL}	3.3*	4.7	16.5	4.5	18.1	
		5†	3.3	11.7	3.2	12.9	
CP to (I/O)n	t_{PLH}	1.5	—	154	—	169	ns
	t_{PHL}	3.3	4.9	17.2	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
MR to Q0, Q7 (299 only)	t_{PLH}	1.5	—	127	—	140	ns
	t_{PHL}	3.3	4	14.3	3.9	15.7	
		5	2.9	10.2	2.8	11.2	
MR to (I/O)n	t_{PLH}	1.5	—	158	—	174	ns
	t_{PHL}	3.3	5	17.7	4.9	19.5	
		5	3.6	12.6	3.5	13.9	
Enable and Disable Times	t_{PZL}	1.5	—	169	—	186	ns
	t_{PZH}	3.3	5.8	20.4	5.6	22.4	
	t_{PLZ}	5	3.8	13.5	3.7	14.9	
	t_{PHZ}						
Power Dissipation Capacitance	$C_{PD}\S$	—	280 Typ.		280 Typ.		pF
Input Capacitance	C_i	—	—	10	—	10	pF
3-State Output Capacitance	C_o	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption, per function.

$$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0 to CP	t_{su}	5*	7.9	—	9	—	ns
Hold Time S1, S0 to CP	t_H	5	0	—	0	—	ns
Setup Time (I/O)n, DS0, DS7 to CP	t_{su}	5	3.9	—	4.5	—	ns
Hold Time (I/O)n, DS0, DS7 to CP	t_H	5	0	—	0	—	ns
Setup Time MR to CP (323)	t_{su}	5*	4.8	—	5.5	—	ns
Hold Time MR to CP (323)	t_H	5	0	—	0	—	ns
Maximum CP Frequency	f_{max}	5	103	—	90	—	MHz
CP Pulse Width	t_w	5	4.8	—	5.5	—	ns
MR Pulse Width	t_w	5	4.4	—	5	—	ns
Recovery Time MR to CP (299)	t_{rec}	5	4.4	—	5	—	ns

*5 V: min. is @ 4.5 V

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CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH} t_{PHL}	5*	3.3	11.7	3.2	12.9	ns
CP to (I/O)n	t_{PLH} t_{PHL}	5	3.7	13.2	3.6	14.5	ns
\overline{MR} to Q0, Q7 (299 only)	t_{PLH} t_{PHL}	5	3.1	11.1	3.1	12.2	ns
\overline{MR} to (I/O)n	t_{PLH} t_{PHL}	5	4.8	16.9	4.7	18.6	ns
Enable and Disable Times	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.8	13.5	3.7	14.9	ns
Power Dissipation Capacitance	$C_{PD}\S$	---	280 Typ.		280 Typ.		pF
Input Capacitance	C_i	---	---	10	---	10	pF
3-State Output Capacitance	C_o	---	---	15	---	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

$\S C_{PD}$ is used to determine the dynamic power consumption, per function.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$$

where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

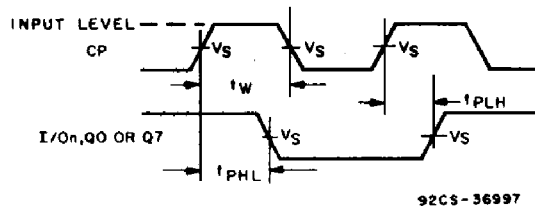


Fig. 2 - Clock prerequisite and propagation delays.

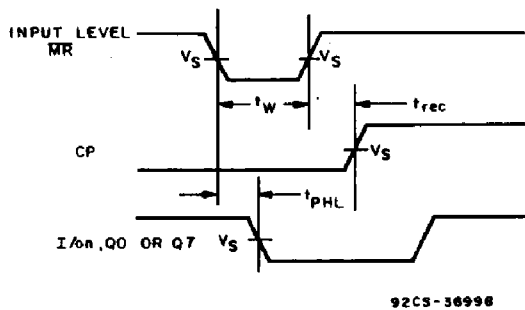


Fig. 3 - Master Reset prerequisite and propagation delays.

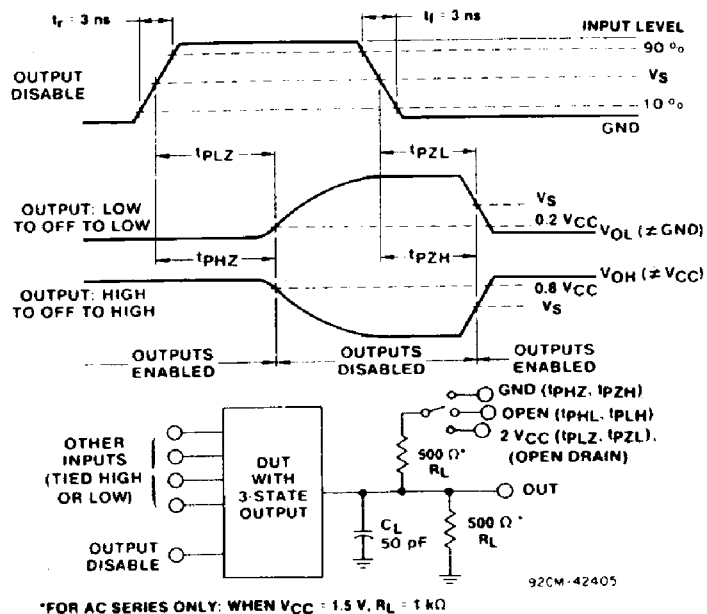


Fig. 4 - Three-state propagation delay times and test circuit.

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

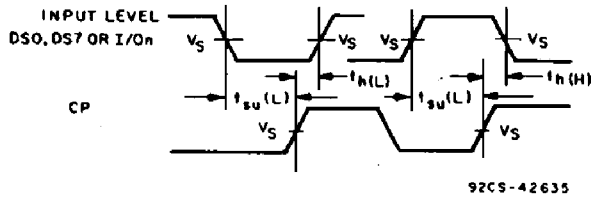
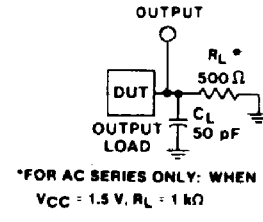


Fig. 5 - Data prerequisite times.



*FOR AC SERIES ONLY: WHEN
 $V_{CC} = 1.5 V, R_L = 1 k\Omega$

Fig. 6 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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